ePIC SVT design and R&D

Nikki Apadula

UC EIC Consortium meeting

August 22, 2023

ePIC SVT DSC

SVT DSC Leader: Ernst Sichtermann

SVT DSC Technical Coordinator: Laura Gonella

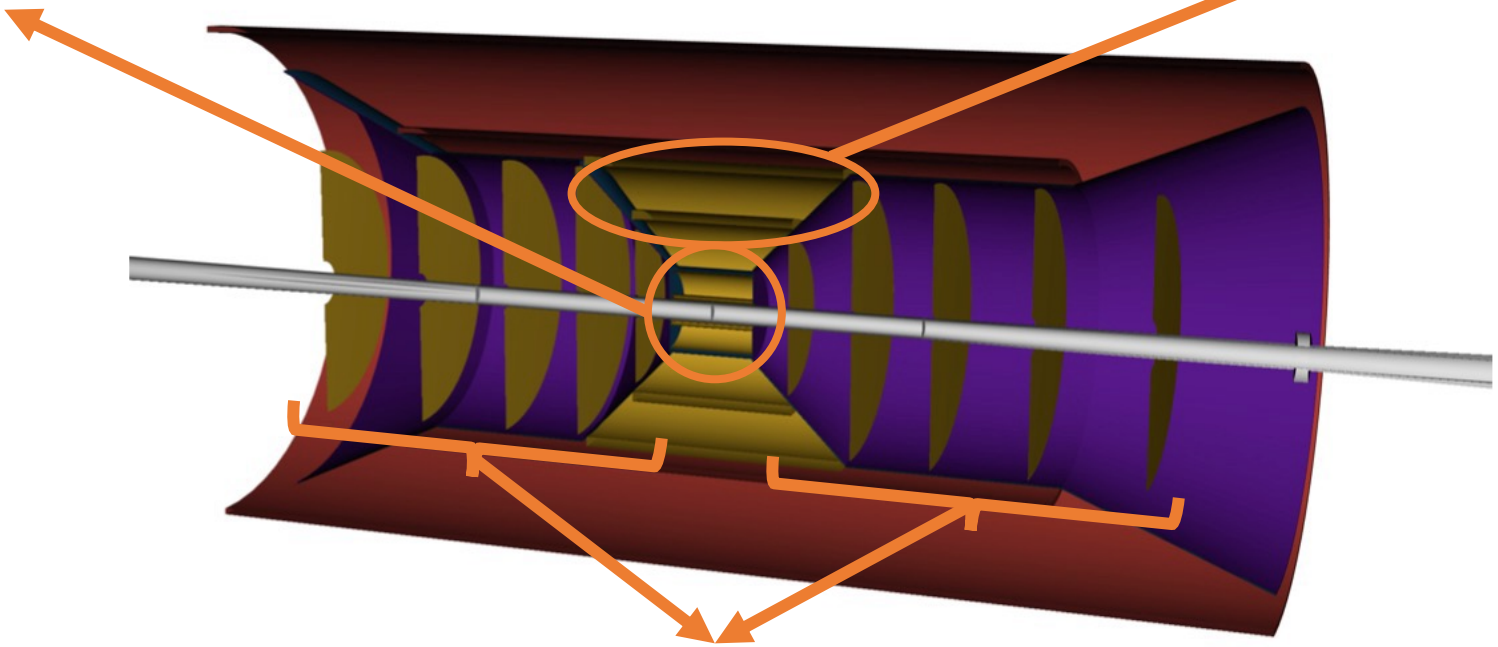
WP structure coming soon

[ePIC Collaboration Meeting July 2023]

SVT configuration

Inner Barrel (IB)
- 2 curved vertex layers
- 1 curved dual purpose layer

Outer Barrel (OB)
- 1 stave-based sagitta layer
- 1 stave-based outer layer



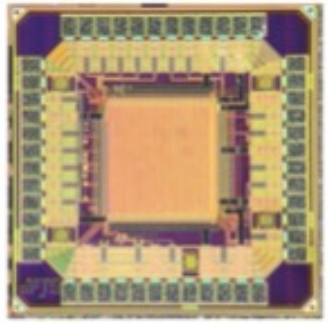
Electron/Hadron Endcaps (EE/HE)
- 5 discs on either side of IP

~8.5 m^2 silicon

Sensor

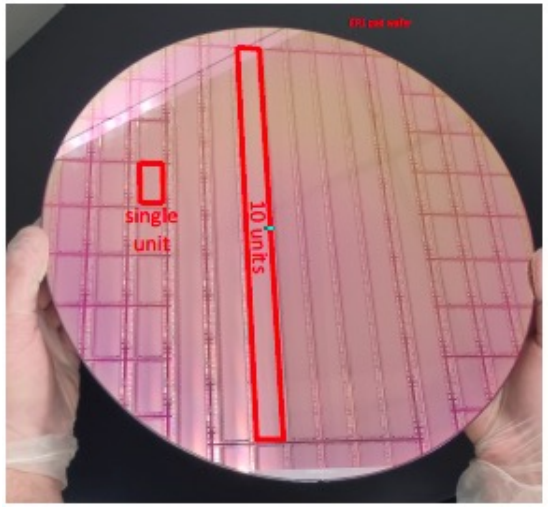
- Monolithic Active Pixel Sensor (MAPS) in 65 nm CMOS technology
  - Developed with ALICE ITS3
  - IB: ITS3 wafer scale sensor
  - OB/HE/EE: EIC Large Area Sensor (LAS)

DPTS



Digital Pixel Test Structure

- MLR1 (Q4 2020) ✓ **complete**
  - Verification of 65 nm technology
- ER1 (Q4 2022) **in progress (MOSS & MOST sensors)**
  - Learning stitching and first yield numbers
- ER2 (Q1 2024)
  - Sensor design to fulfill ITS3 requirements
- ER3 (Q2 2025)
  - Final ITS3 design/production



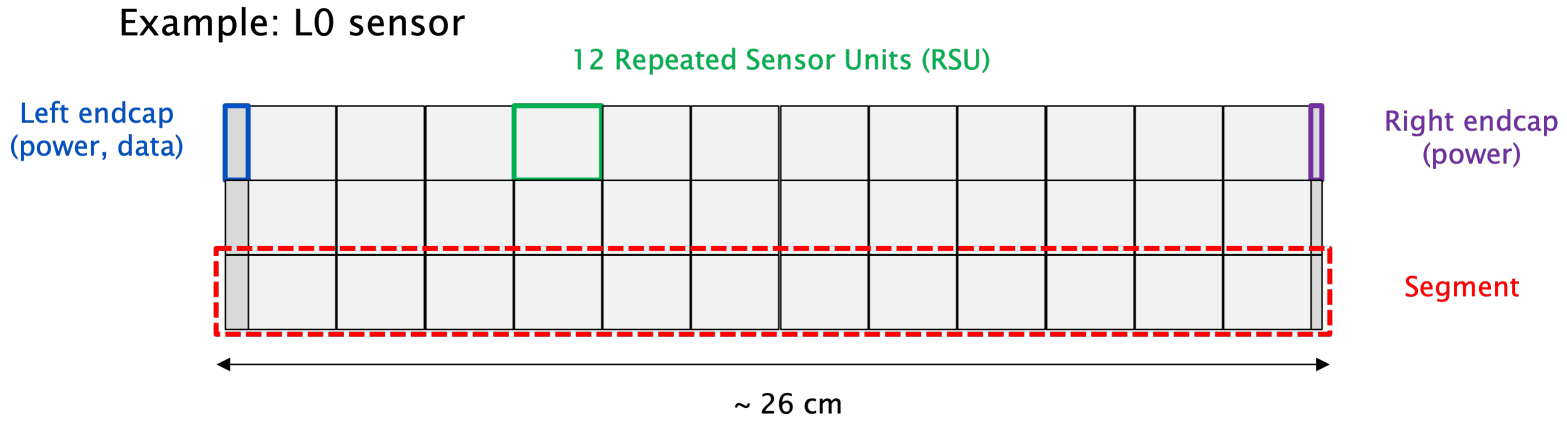
EIC LAS based on ER2 & ER3

Sensor structure

ER2 design evolving
Final RSU size TBD

ITS3 & ePIC SVT IB

L0: 3 segments
L1: 4 segments
L2: 5 segments



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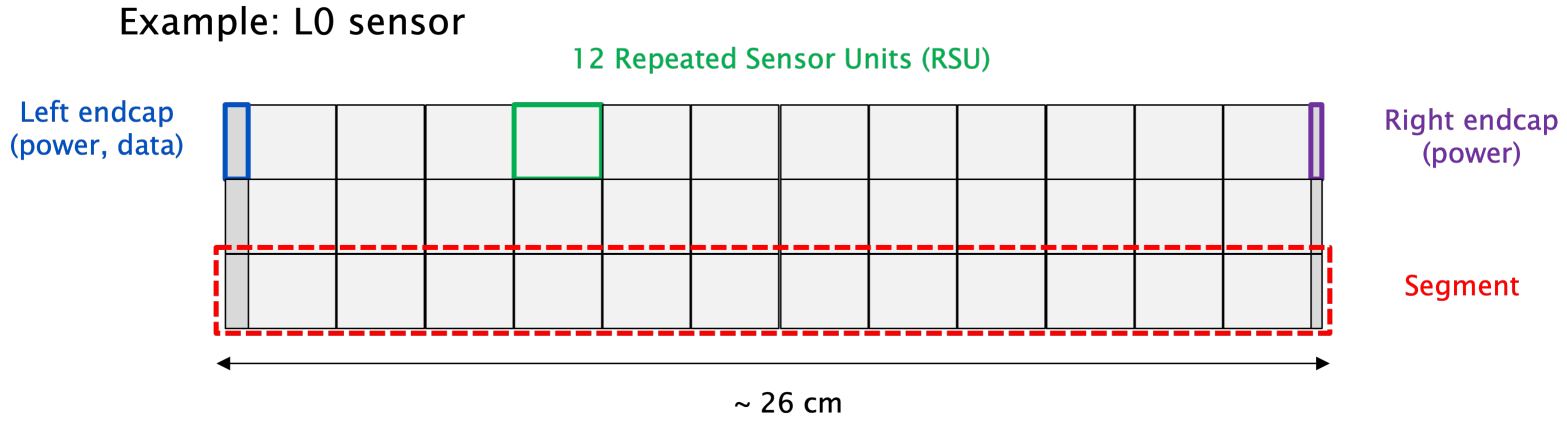
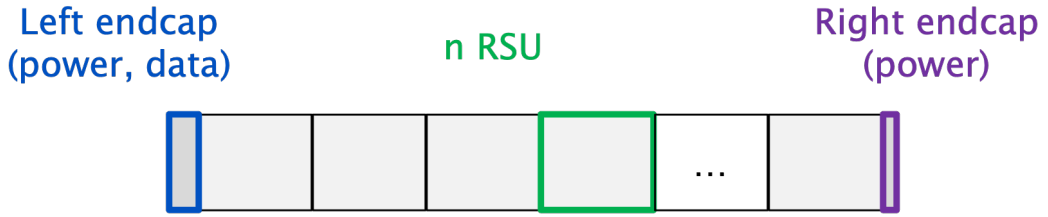


EIC LAS

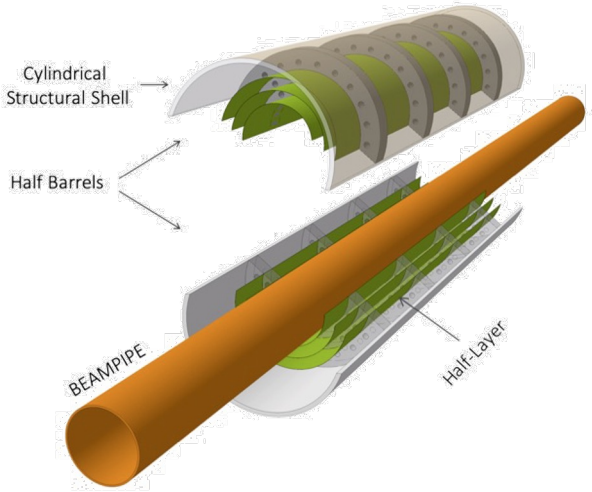


EIC LAS

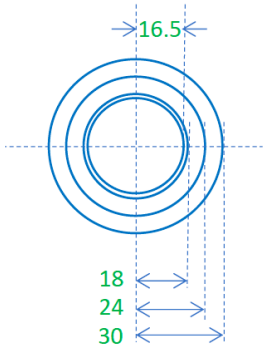
- Single segment
- Variable # RSU
- Right endcap not needed if n ≤ 6

Inner barrel

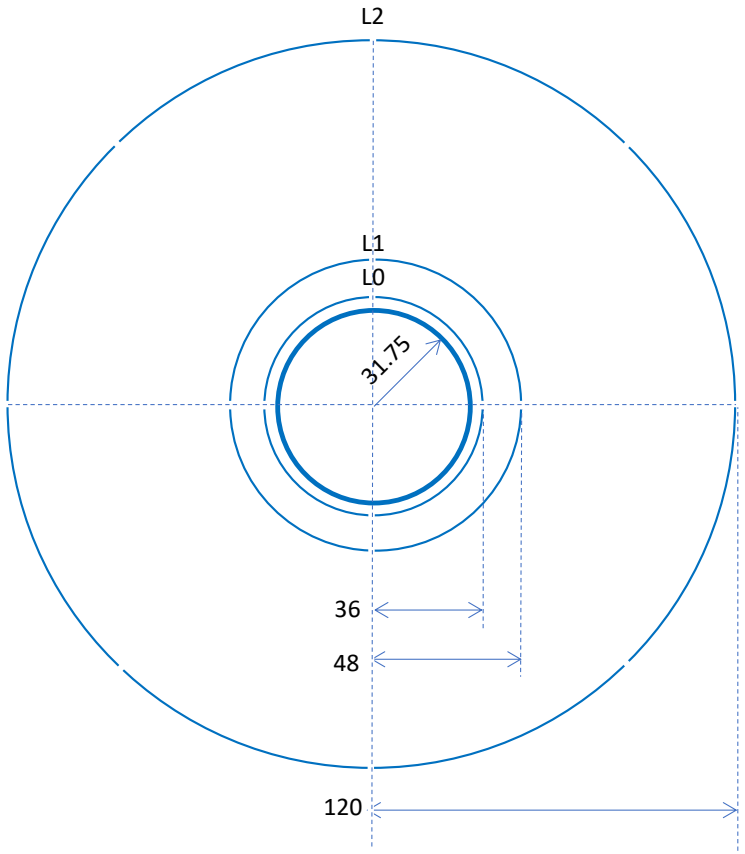
- 3 layers of thin, bent, wafer-scale silicon sensors
- Minimal mechanical support, air cooling, no services in active area
  - ALICE ITS3 adapted to ePIC radii



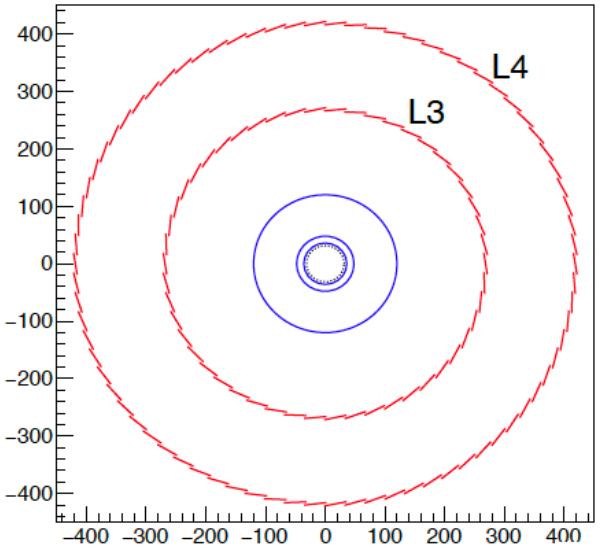
ALICE ITS3

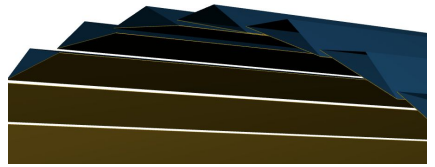


Option for ePIC Inner Barrel

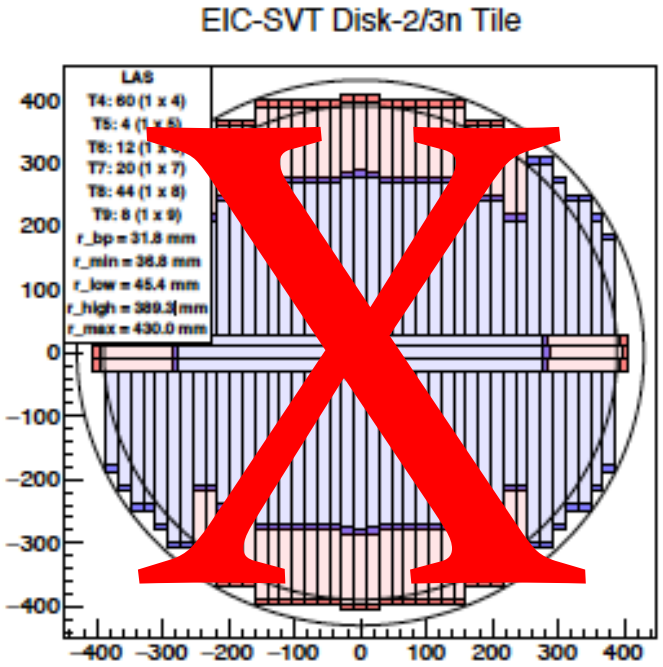


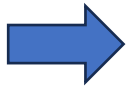
Outer barrel & discs





- Large Area Sensor (LAS)
  - Optimized for high yield, low cost, large area coverage
  - **2-3 variations only**
- OB
  - Stave-based design
- EE/HE
  - Sensor tiling
- Material budget challenging!
  - 0.24% X/X0 in discs





New variations exist, more to come

SVT R&D

2024															
Project:	**eRD101**	**eRD102**	**eRD103**	**eRD104**	**eRD105**	**eRD106**	**eRD107**	**eRD108**	**eRD109**	**eRD110**	**eRD111**	**eRD112**	**eRD113**	**eRD114**	**eRD115**
Title:	mRICH	dRICH	hpDIRC	Silicon Service reduction	SciGlass	Forward ECal	Forward HCal	Cylindrical MPGD	ASIC/Electronics	Photosensors	Si-Vertex	AC-LGAD	Si-Sensor Development and Characterization	pfRICH	Imaging Cal
Contact:	X. He (GSU)	E. Cisbani (INFN-RM1), M.Contalbrigo (U. Ferrara), A. Vossen (Duke)	G. Kalicy (CUA), J. Schwiening (GSI)	L. Gonella (B'ham)	T. Horn and .L. Pegg (CUA)	H.Z. Huang (UCLA), O. Tsai (UCLA)	Friederike Bock (ORNL)	K. Gnanvo (UVA)	Fernando Barbosa (JLab)	Y. Ilieva (SC), C. Zorn (JLab), J. Xie (ANL), A. Kiselev (BNL), Pietro Antonioli (INFN)	Nicole Apadula (LBNL)	Zh. Ye (UIC)	Grzegorz Deptuch (BNL)	A. Kiselev (BNL)	Maria Zurek (ANL), Sylvester Joosten (ANL), Zisis Papandreou (ANL)
Proposal/ Progress Report:	v1 (pdf)	v1 (pdf)	v1 (pdf)	v1 (pdf)	-	v1 (pdf)	v1 (pdf),	v1 (pdf)	v1 (pdf), v2 (pdf)	v1 (pdf)	v1 (pdf)	v1 (pdf)	v1 (pdf)	v1 (pdf)	v1 (pdf)

eRD104: Powering & Readout

eRD111: Everything else

- modules/FPC
- Stave & Disc design
- Global mechanics
- Cooling

eRD113: Sensor development & characterization
(see talks from Barak & Oscar)

Generic R&D

FY23: Embedded silicon, aluminum flex

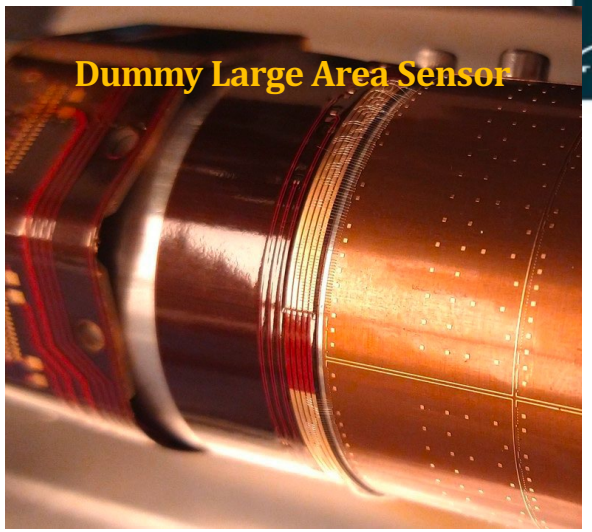
Powering & readout

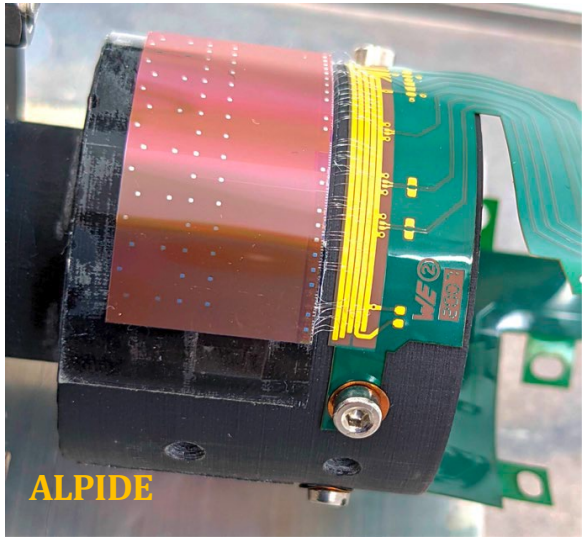
- Serial powering: EIC LAS powered in series by constant current
  - Regulators convert the input current into (analog & digital) voltage
- Shunt-LDO
  - Concept developed for ATLAS & CMS serial powering
  - External to LAS
- Multiplexing strategy for LAS
  - Multiple 10 Gbps links for ITS3, not necessary for ePIC
- External (commercial FPGA) & internal (integrated on sensor) options under consideration

Modules/Connections

- INFN: Previous EICSC presentation
- Single-reticle sensors & large-size MAPS
  - Bending, thinning, interconnection
- Bending & wire-bonding have been successfully exercised at ITS3 vertex radii
- First electrical tests of ITS3 FPC in Bari

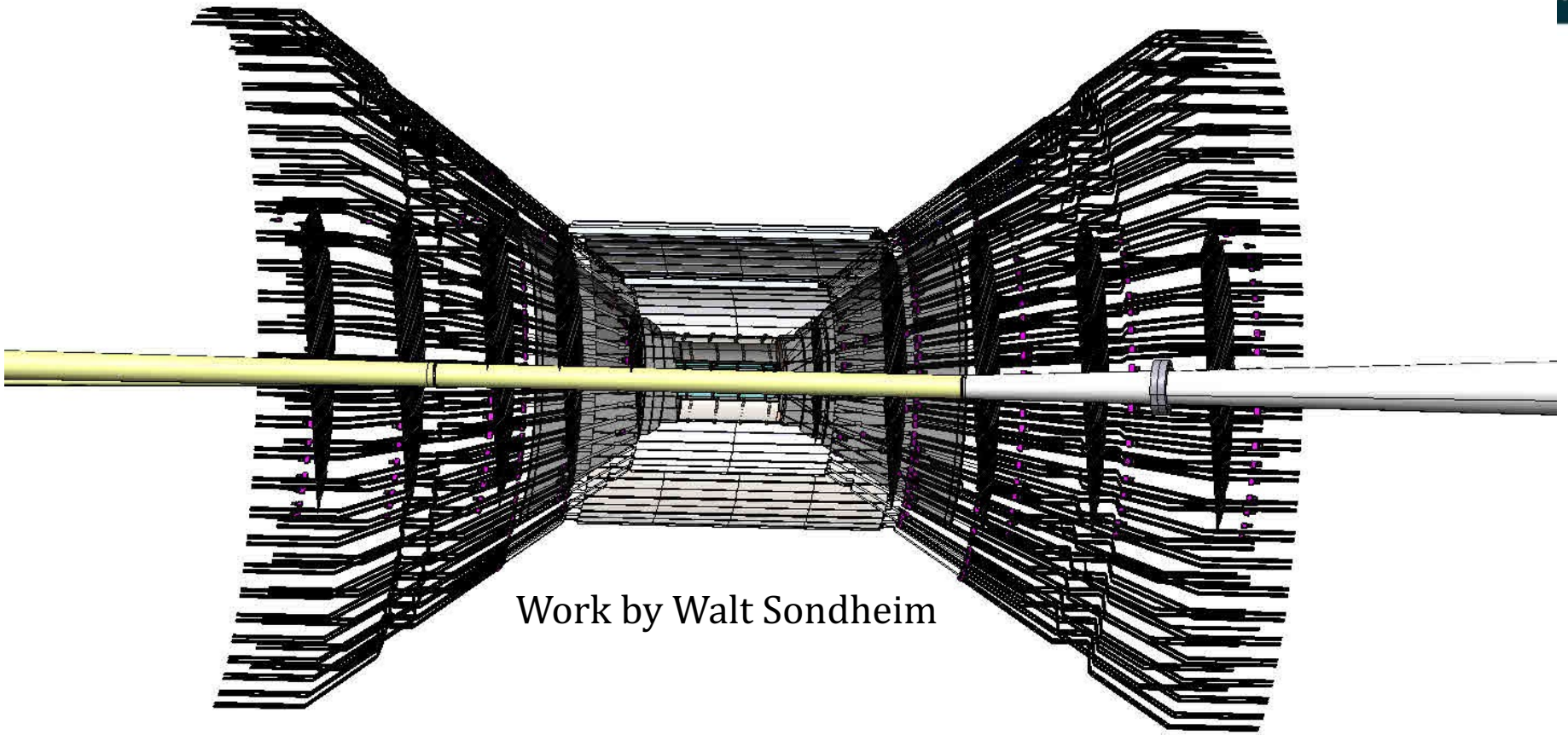
- **OB/HE/EE FPC likely different from IB**





https://doi.org/10.1016/j.nima.2021.166280

CAD Model

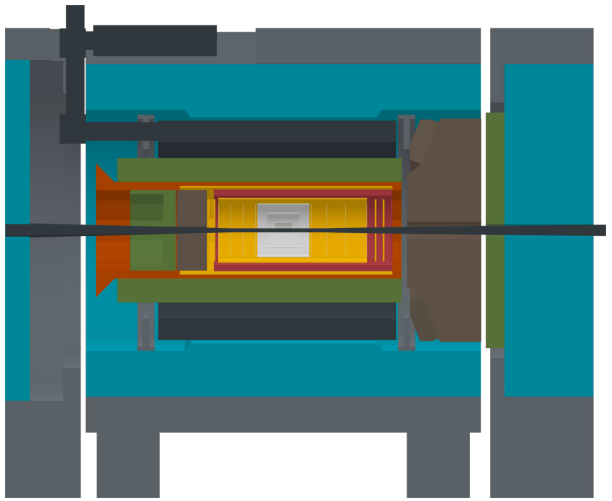


Work by Walt Sondheim

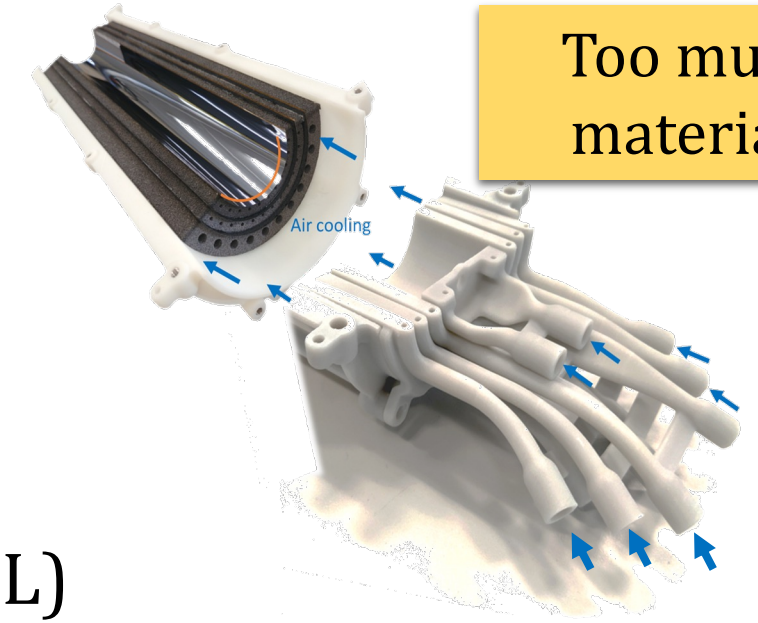
- EICSC 1/30/23
- SVT mechanics meeting

Global mechanics/support

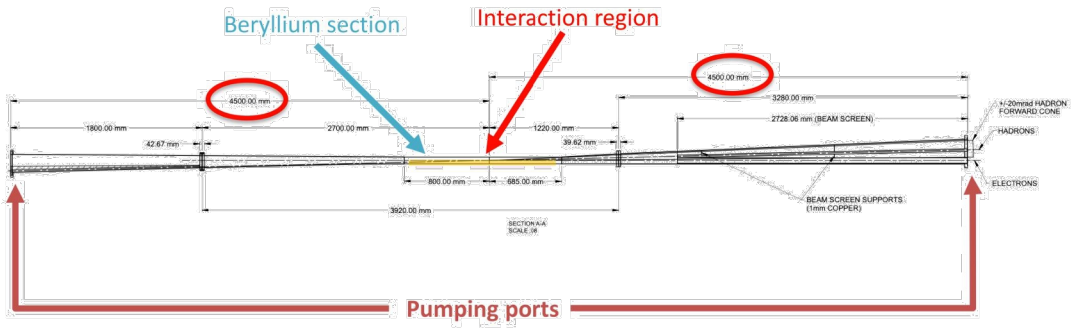
- SVT mechanics meeting 3/29/23
  - Initial discussion with interested groups & project engineers
- ePIC engineering workshop 5/10 – 5/12/23
  - 3 day workshop at BNL
  - Brainstorming/conversation about assembly sequence, conceptual support design, & more
- A lot of work on service estimates
  - Low voltage, bias, cables defined
  - Update on data links, cooling

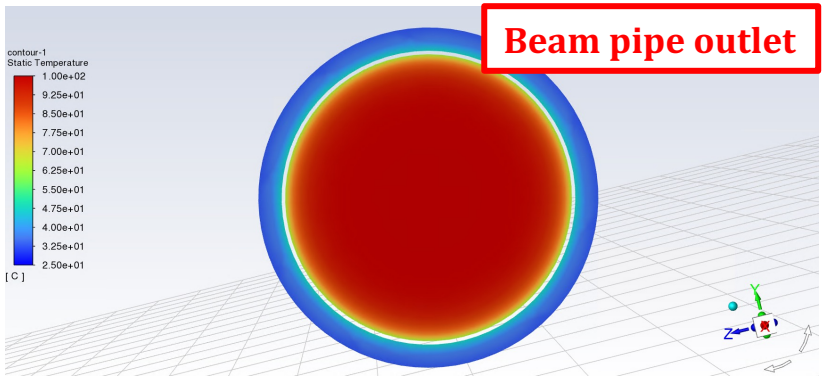


Cooling: IB

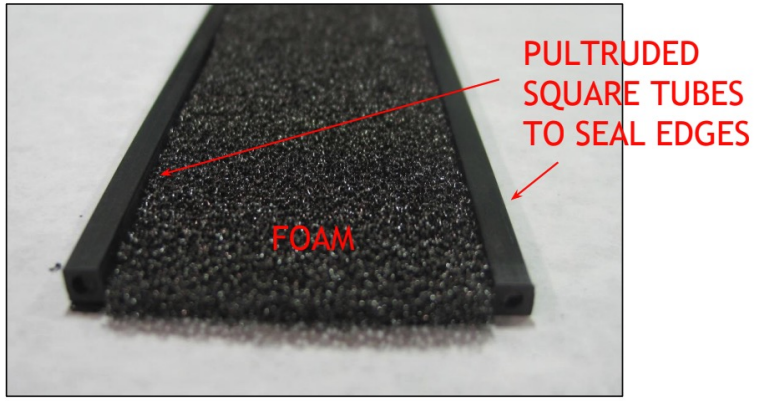


- How to bring in the air?
- Mechanical considerations
  - More support? Vibrations?
- Beam pipe bake-out studies (Jlab, LBNL)
  - Previous talks: EICSC Meeting 6/6/22, 2/28/23
    - 5 mm gap between beam pipe and 1st silicon layer

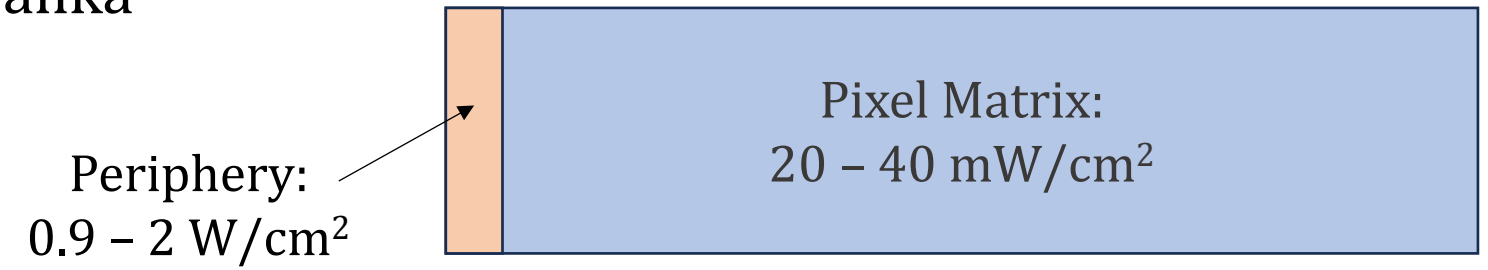




Cooling: OB, EE, HE



- Is air cooling viable?
- Liquid for the periphery?
- Global options?
- Cooling will be integrated with local support structures
- Internal air cooling project (LBNL)
  - Previous talks: EICSC Meeting 10/10/22, 2/28/23
  - See talks by Ziyuan & Malika

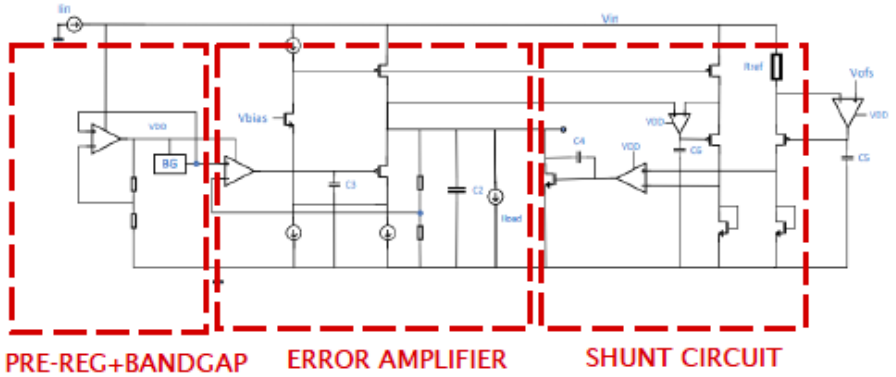


Summary

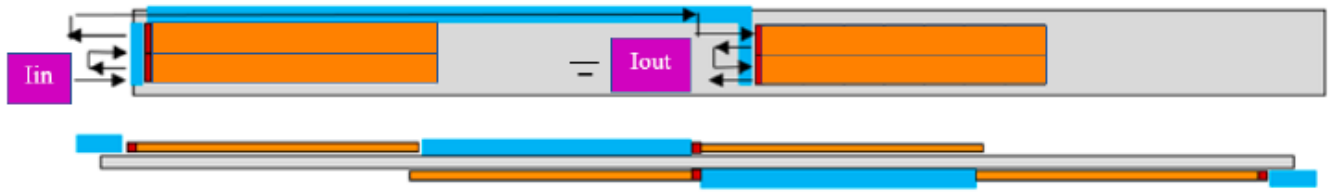
- A lot of progress in the last year on the ePIC SVT
  - Still a lot of work to do to get to construction readiness!
- More groups have joined the SVT effort
  - More are welcome!
- ER2 is advancing rapidly & will provide much needed information
  - Sensor size, power consumption, data transmission
- FY24 R&D & PED
  - Advance designs towards final, scale up prototype pieces
  - Path to TDR

Powering

- Shunt-LDO regulator design advancing
  - Submission of 65 nm prototype in Q1-24
  - Submission of 180 nm prototype in Q2-24

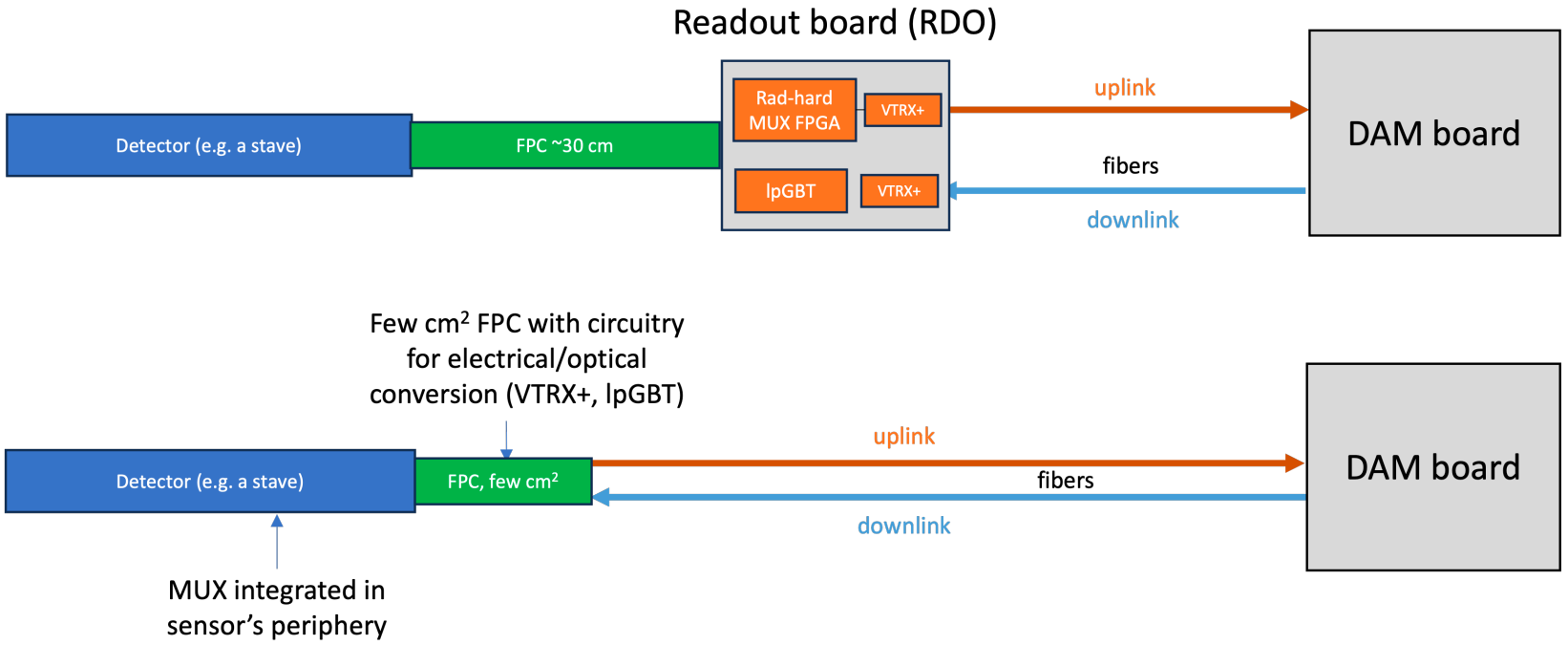


- Initial conceptual SP design for OB
  - 2/4 EIC LAS sensors in a serial powering chain in L3/L4
  - Assumed serial powering chains of 3 EIC LAS sensors in disks for now
  - Implications of power supply to sensor from left and right endcaps needs study



L4 serial powering scheme;
top – stave top view, bottom – stave side view

Powering scheme for the ePIC SVT @ https://indico.bnl.gov/event/18202/
Update on ePIC powering and associated services estimates @ https://indico.bnl.gov/event/18525/


Readout board (RDO)
Detector (e.g. a stave)
FPC ~30 cm
Rad-hard MUX FPGA
VTRX+
lpGBT
VTRX+
uplink
fibers
downlink
DAM board
Few cm² FPC with circuitry for electrical/optical conversion (VTRX+, lpGBT)
Detector (e.g. a stave)
FPC, few cm²
uplink
fibers
downlink
DAM board
MUX integrated in sensor's periphery

SVT by the numbers

Region	Layer	radius [mm]	length [mm]	X/X0
IB	L0	36	270	0.05 %
	L1	48	270	0.05 %
	L2	120	270	0.05 %
OB	L3	270	540	0.25 %
	L4	420	840	0.55 %

Region	Disk	z [mm]	inner radius [mm]	outer radius [mm]	X/X0
EE	ED0	-250	36.76	240	0.24 %
	ED1	-450	36.76	415	0.24 %
	ED2	-650	36.76	421.4	0.24 %
	ED3	-850	40	421.4	0.24 %
	ED4	-1050	46.35	421.4	0.24 %

Region	Disk	z [mm]	inner radius [mm]	outer radius [mm]	X/X0
HE	HD0	250	36.76	240	0.24 %
	HD1	450	36.76	415	0.24 %
	HD2	700	38.46	421.4	0.24 %
	HD3	1000	53.43	421.4	0.24 %
	HD4	1350	70.14	421.4	0.24 %