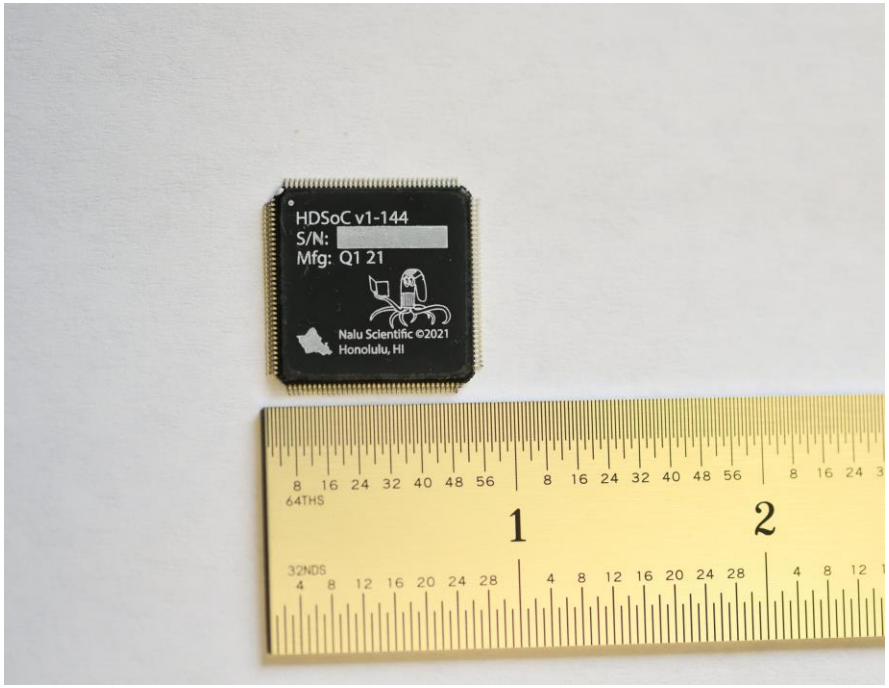
Nalu HDSoC Digitizer ASIC Evaluation

Topics:

- High-Level Overview
- System Information
- System & Test Setup
- Results
- Next Steps

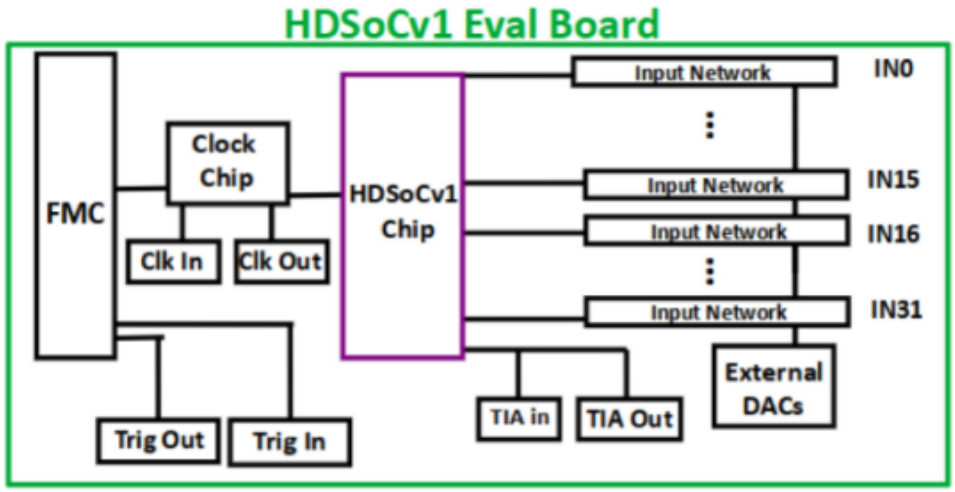


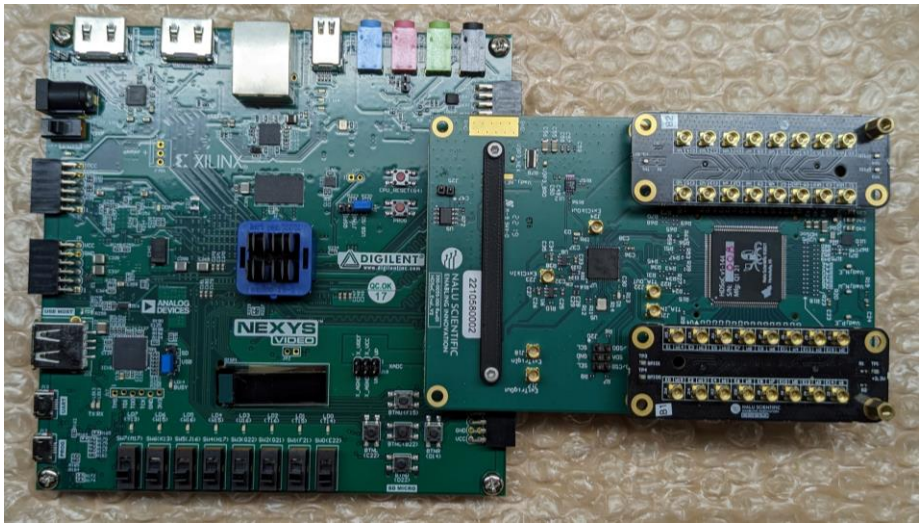
Steve Titus

Thursday, August 10, 2023

High-Level Overview

- Digitizer ASIC
- Developed by Nalu Scientific
- Version 1
  - 32 Channels
  - Sample Rate: 1-2 GSa/s
  - Sample Buffer: 2k
  - Eval Boards Available
- Version 2
  - 64 Channels
  - In Development
  - Under consideration for EIC as an alternate ASIC

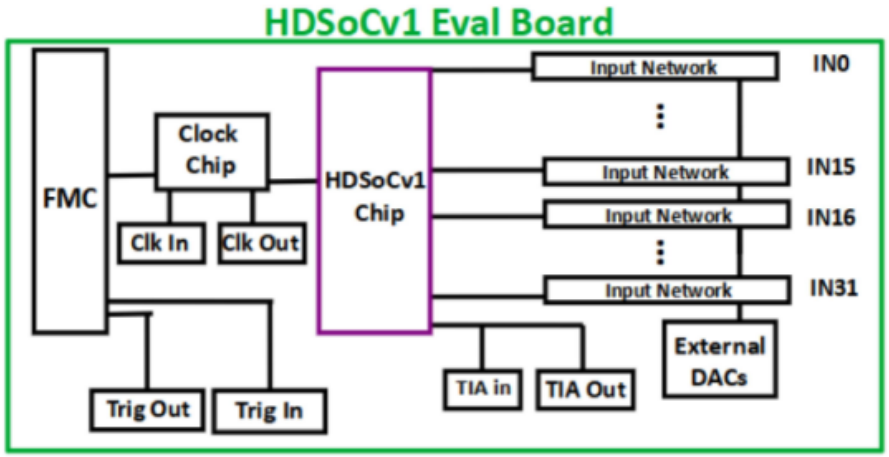


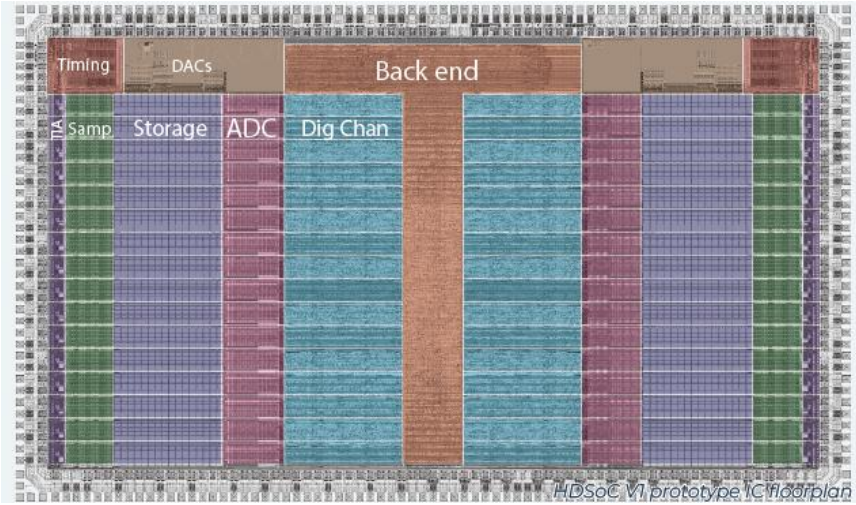


HDSOCV1 Eval Board And FPGA Dev Board

System Information - Inputs

- Inputs
  - Input range ± 1.25V, 0V centered
  - Recommended BW 500MHz
    - Absolute BW 600-700 MHz
  - 50 Ohm Termination
  - No Shaping On V1
    - Expected On V2





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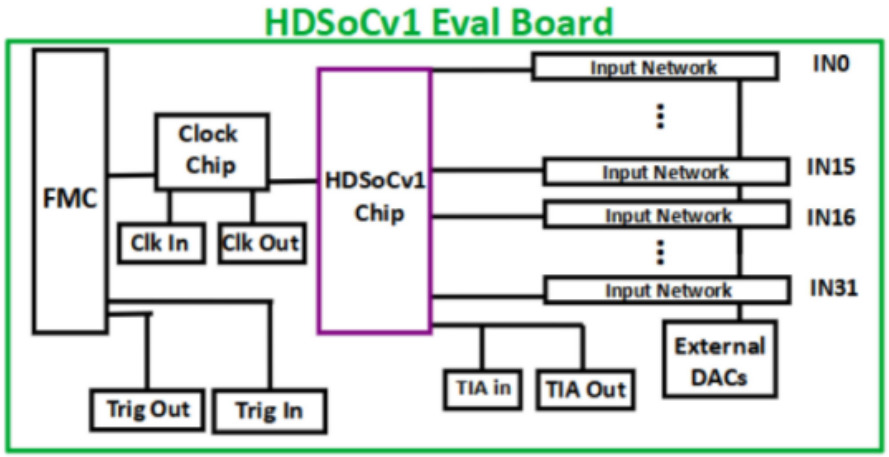
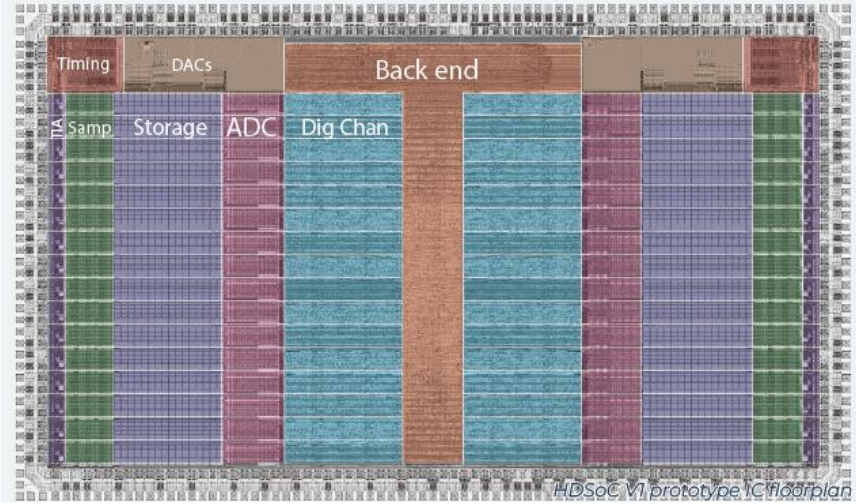
System Information - ADC

- Wilkinson ADC Array
  - All Channels Are Independent And Asynchronous
  - Conversion Time per channel ~5us
- Streaming Readout and External Triggered Capable





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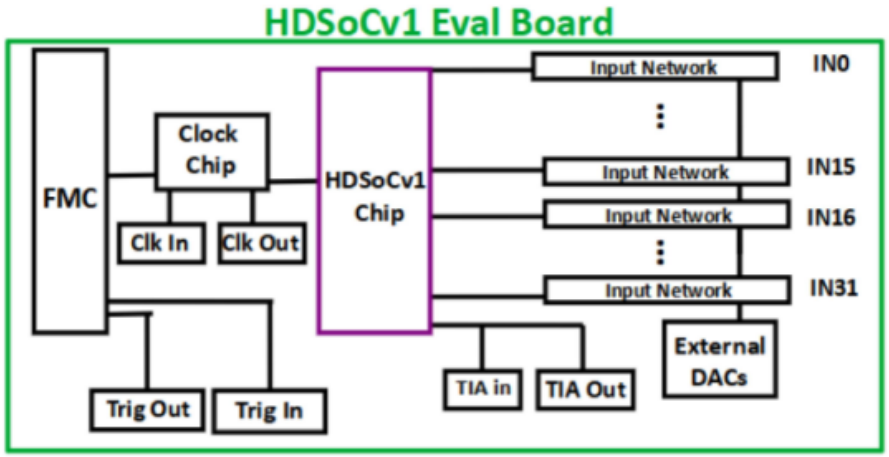
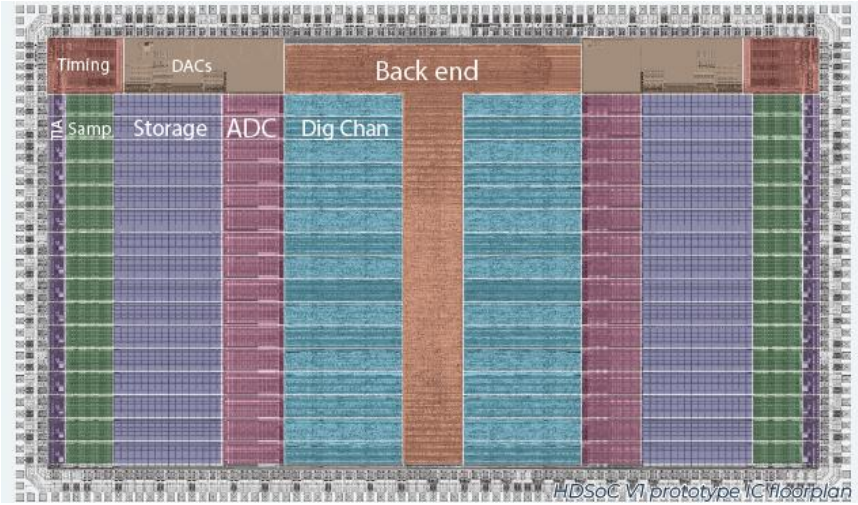
System Information - Clocks

- Clocks
  - SST (Main Reference Clock)
    - 15.625 MHz
  - Sysclk
    - 2x,4x, 8x SST Clock Frequency
  - Gccclk – AD Conversion & Serial Interface Reference
    - Dependent On Specific Board
    - 10x Sysclk
    - 312.5mhz On This V1





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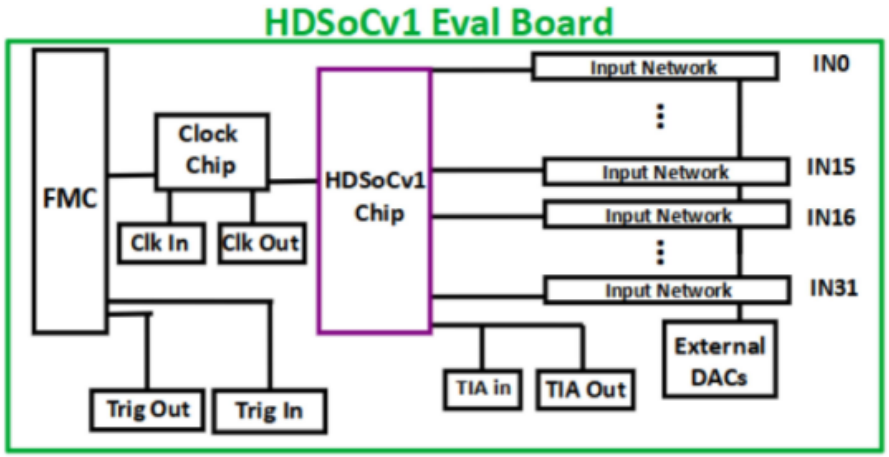
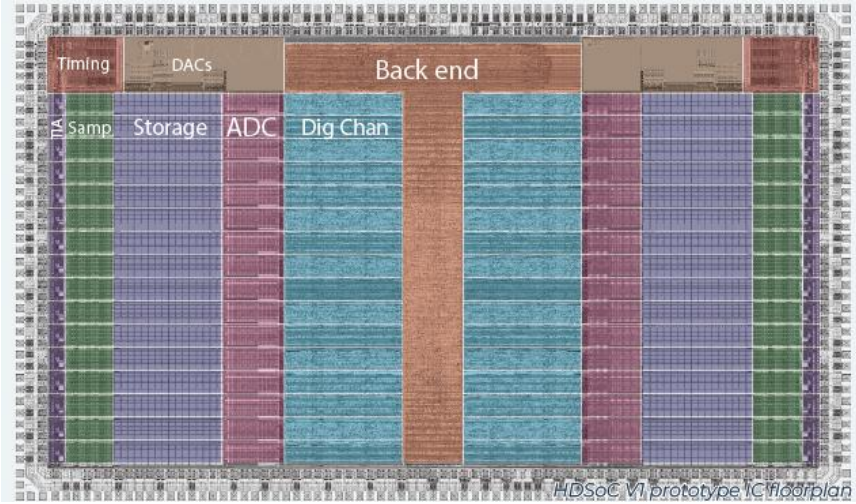
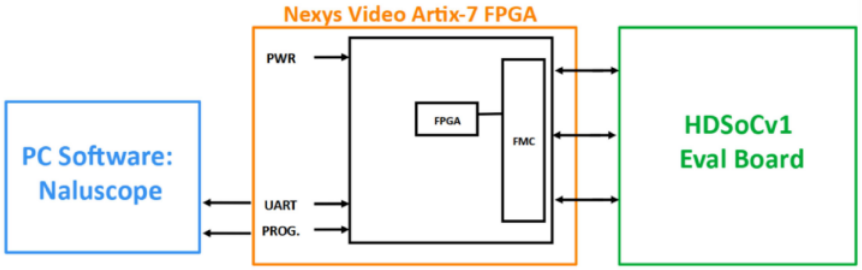
System Information Data Format

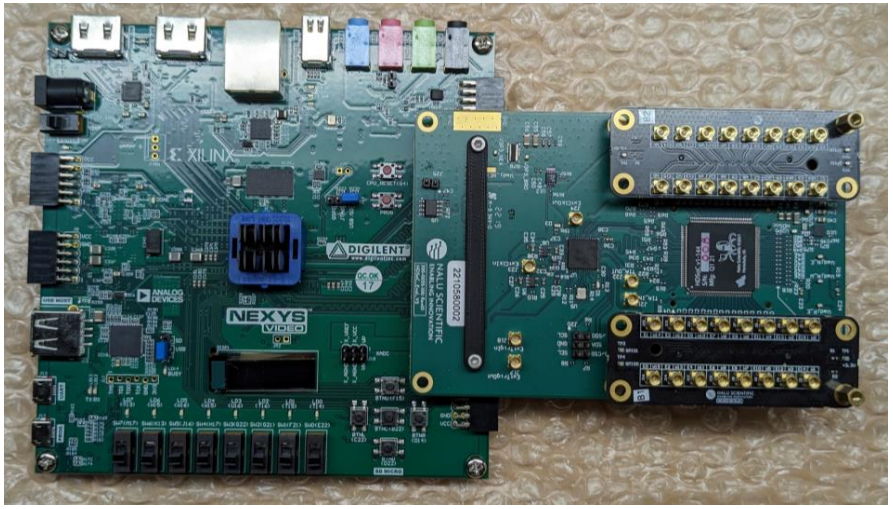
- Data Out Format
  - 32-bit Data From Sample
  - Header Defining
    - Time
    - Channel Number
    - Position





Eval Board System Setup

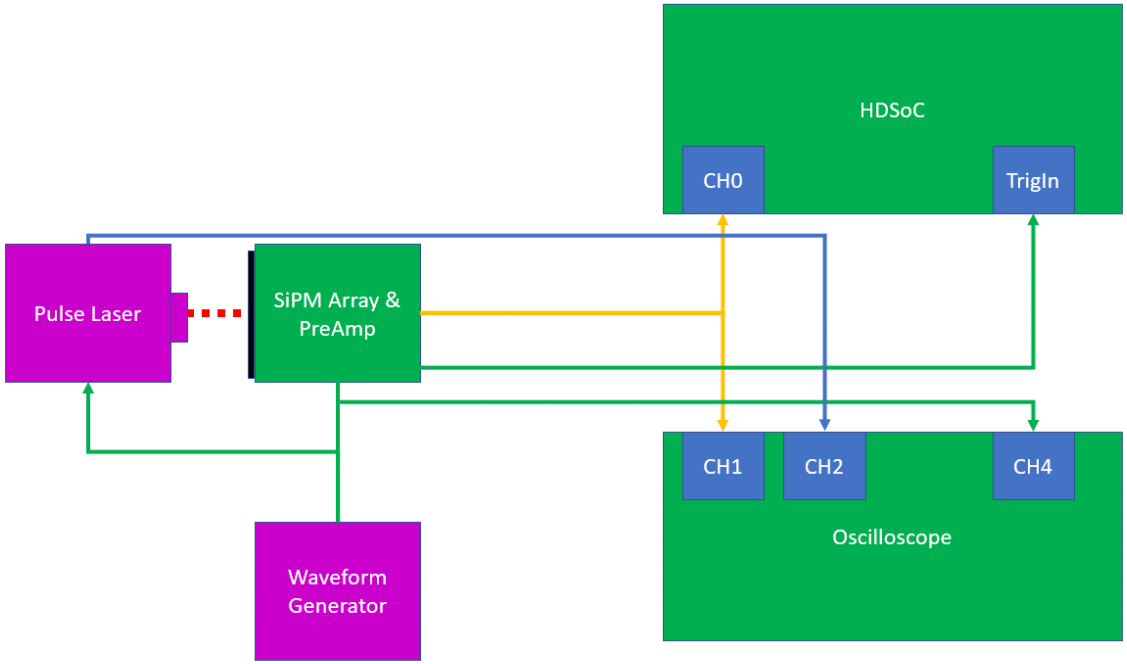




- Components
  - Hdsocv1 Evaluation Board
  - Nexys Video Artix 7 FPGA Development Board
  - PC With Naluscope Software
    - Nalu Provided
    - GUI Based
    - Interfaces With Hardware And Displays Data
    - Important Features still in development (ex: Counts to mV)

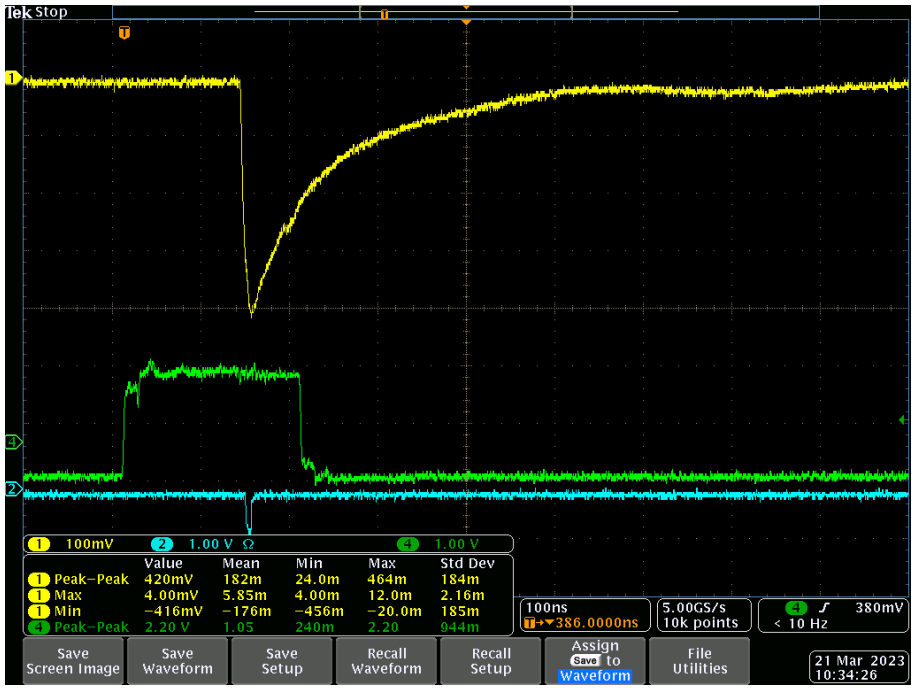
- Connections
  - Hdsocv1 To FPGA:
    - FMC High-density Board-to-board Connector
  - FPGA To PC:
    - UART Via USB Cable
      - 10Hz Trigger Rate
    - Ethernet
      - Tested To 300Hz Trigger Rate
        - Limited By Current Firmware

Test Setup

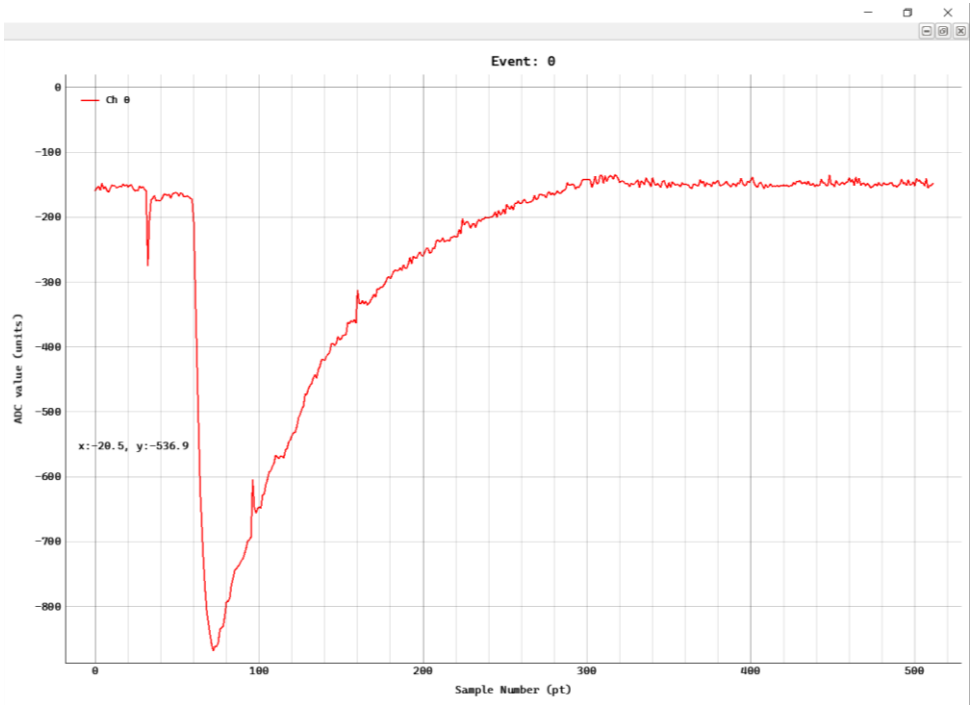


- Triggered Test Setup
  - SiPM was connected to HDSoC and Oscilloscope to capture data in parallel
  - A waveform generator sent a trigger pulse to the SiPM Laser and HD SoC
    - 50ns delay on from trigger to laser pulse
- Streaming Readout Test Setup
  - Same Setup as triggered, replacing trigger with a 10kHz laser pulse.
  - HDSoC was unsuccessfully able to trigger on the falling edge of a SiPM Pulse
    - Due to current limitations in the software
  - A positive edge square wave from a waveform generator was used instead

Test Results – Triggered



Oscilloscope Capture



HDSoC Capture

- Input
  - SiPM Signal
    - 800mV Amplitude
    - ~300mS Settling time
- Note - Signal Spikes have been resolved in the software

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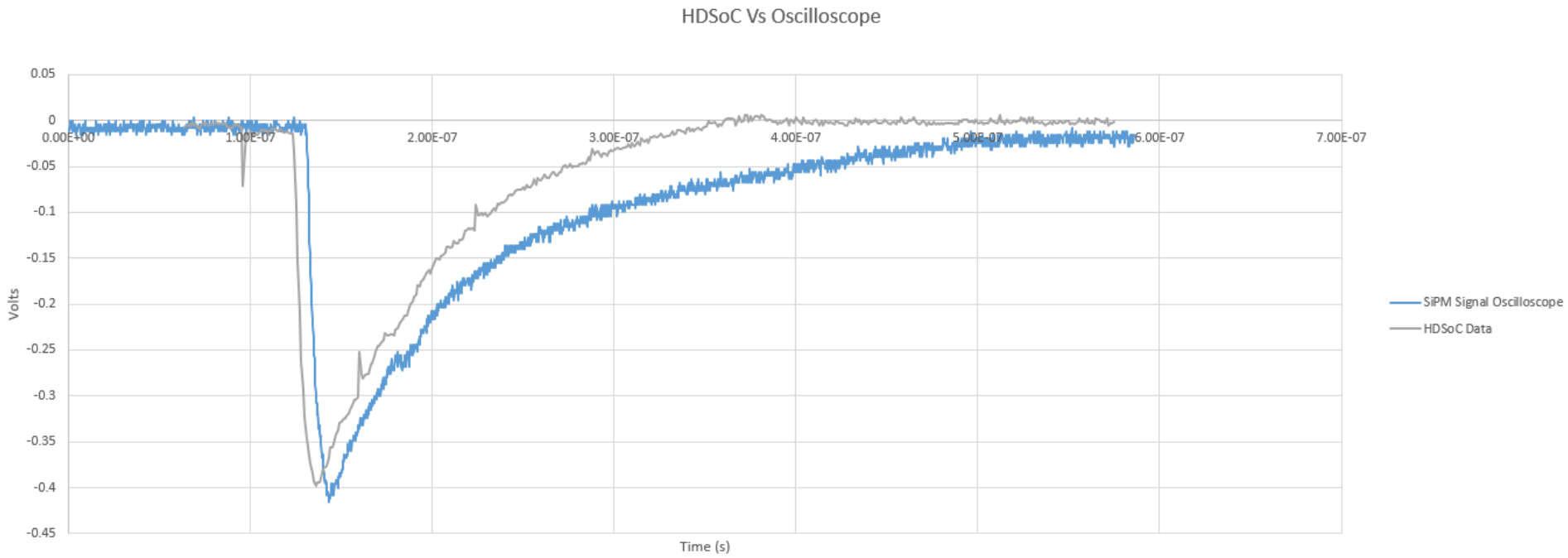
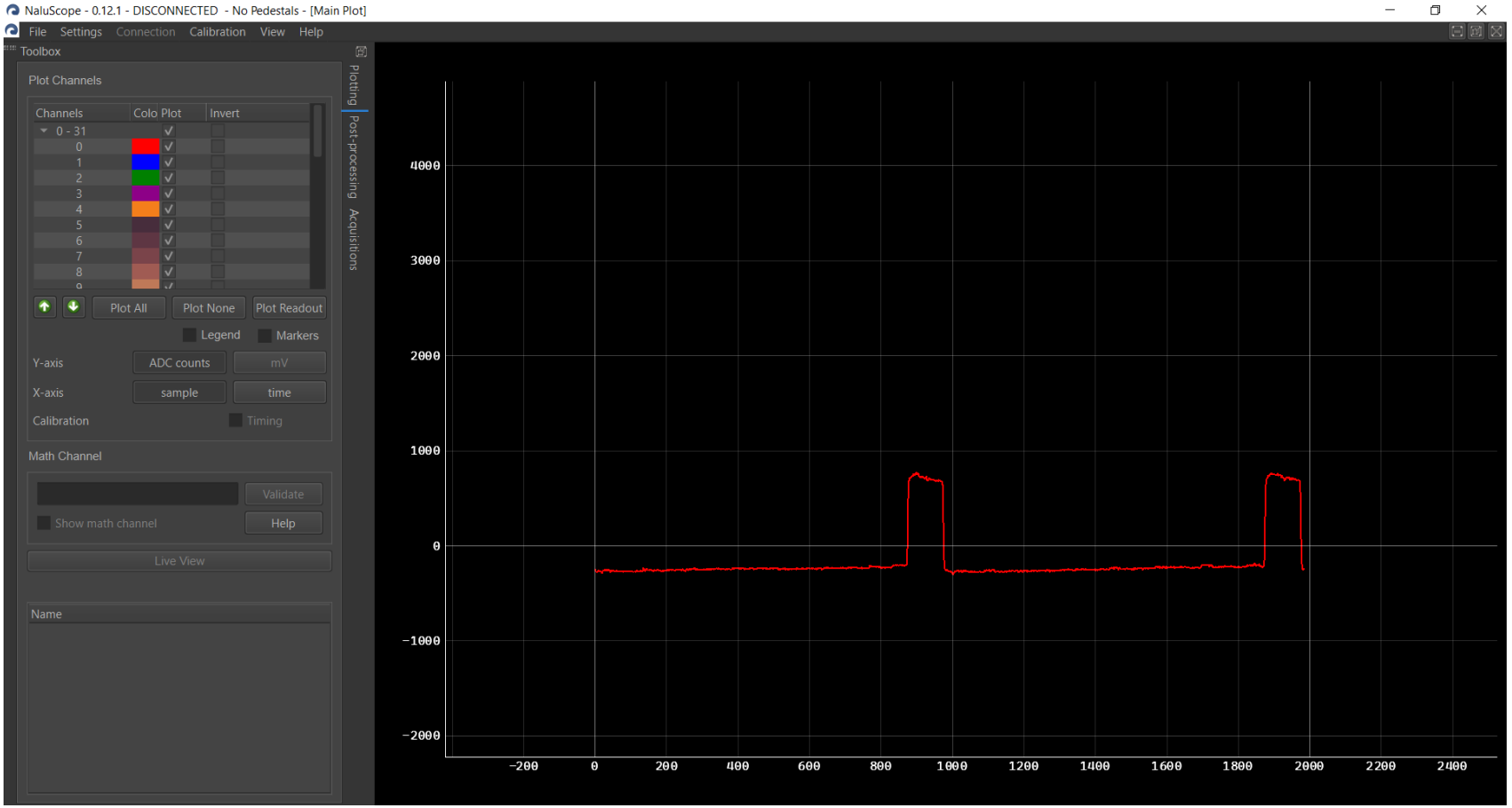
Test Results – Triggered



- Some signal shape differences were observed
- Above signals were linearly scaled to estimate
- Nalu does not have any shaping circuitry on the V1 eval board
- Nalu does not have a conversion from ADC counts to mV yet
  - Needed to confirm and quantify shaping

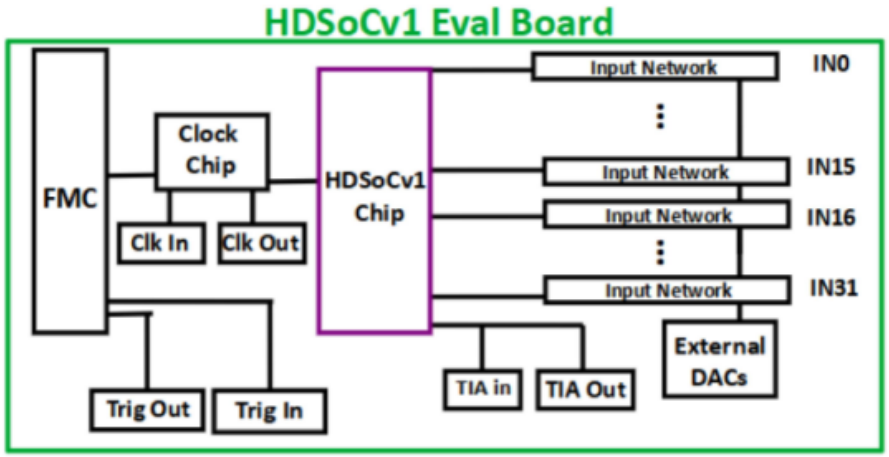
Test Results – Square Wave

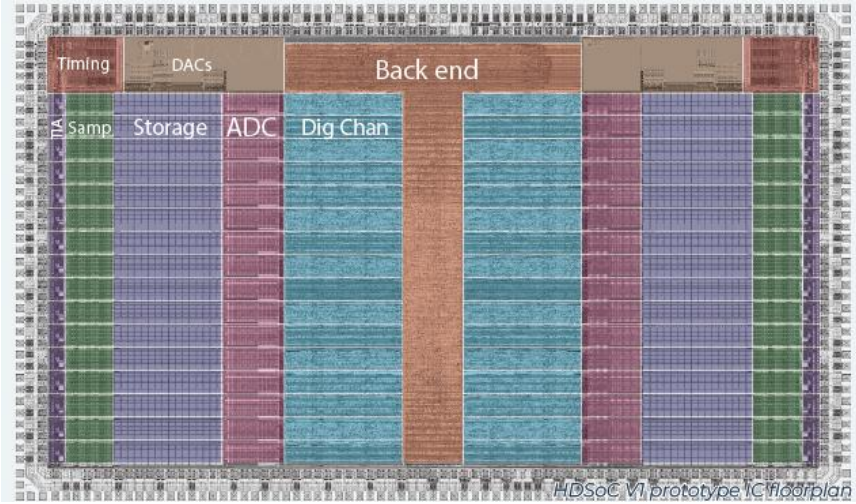


- Input
  - 800mV Square Wave
  - 200ns Period
- Voltage droop after rising edge was observed in NaluScope but not on the Oscilloscope

Next Steps

- Continue working with Nalu to trigger on negative edge SiPM Pulse
- Investigate signal shaping once counts to mV is available





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