# RDO discussion

## Input from Micromegas tracker

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# FEB – RDO locations

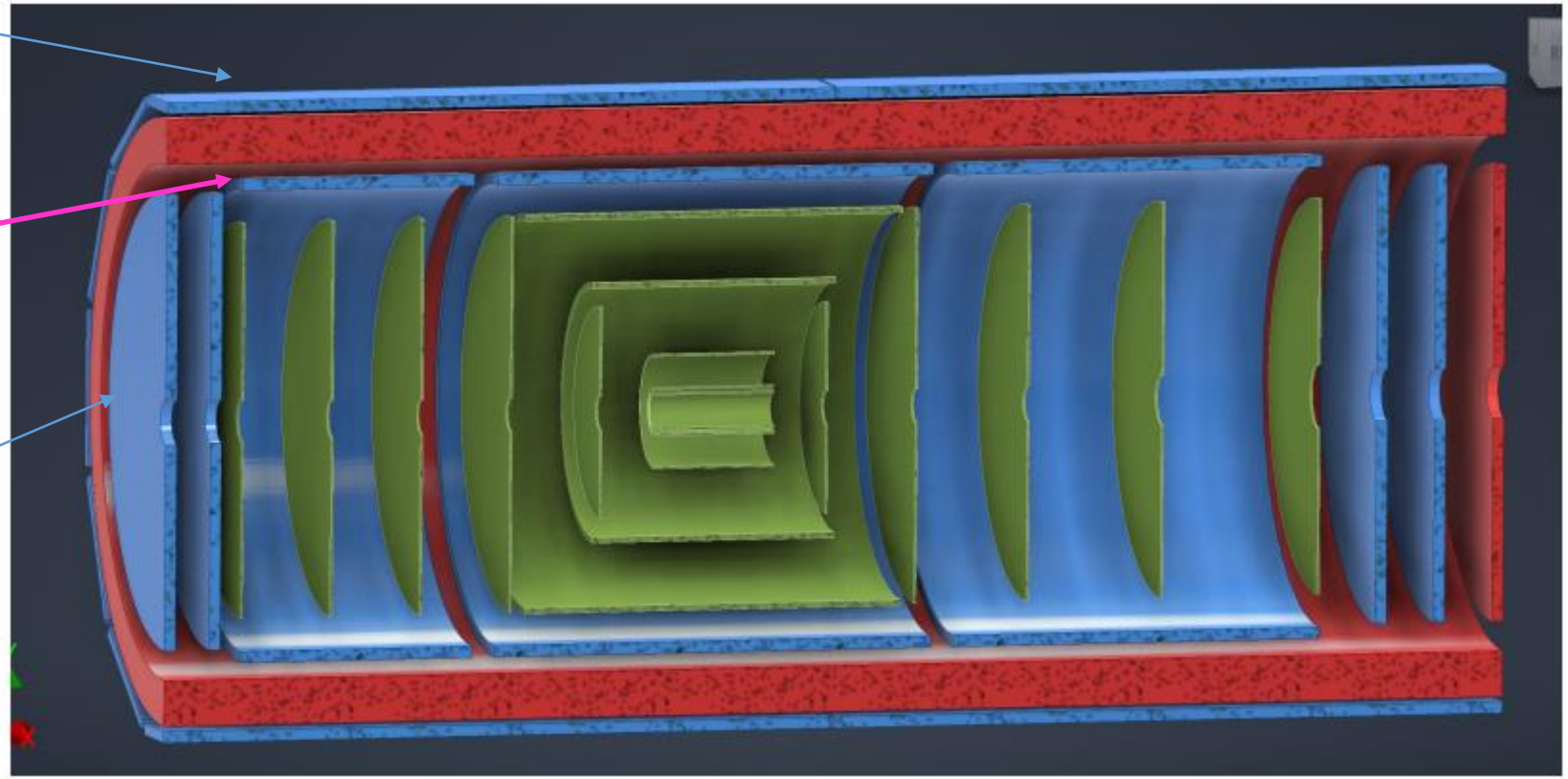
# Recent update of ePIC tracking configuration

- [ePIC Tracking Working Group Meeting (15 juin 2023) · Indico (bnl.gov)]

µRWell ?

Cylindrical Micromegas ? (Saclay interest)

GEM / µRWell ?




- Very recent for me: had not yet enough time to seriously work on it

# Recent update of ePIC tracking configuration

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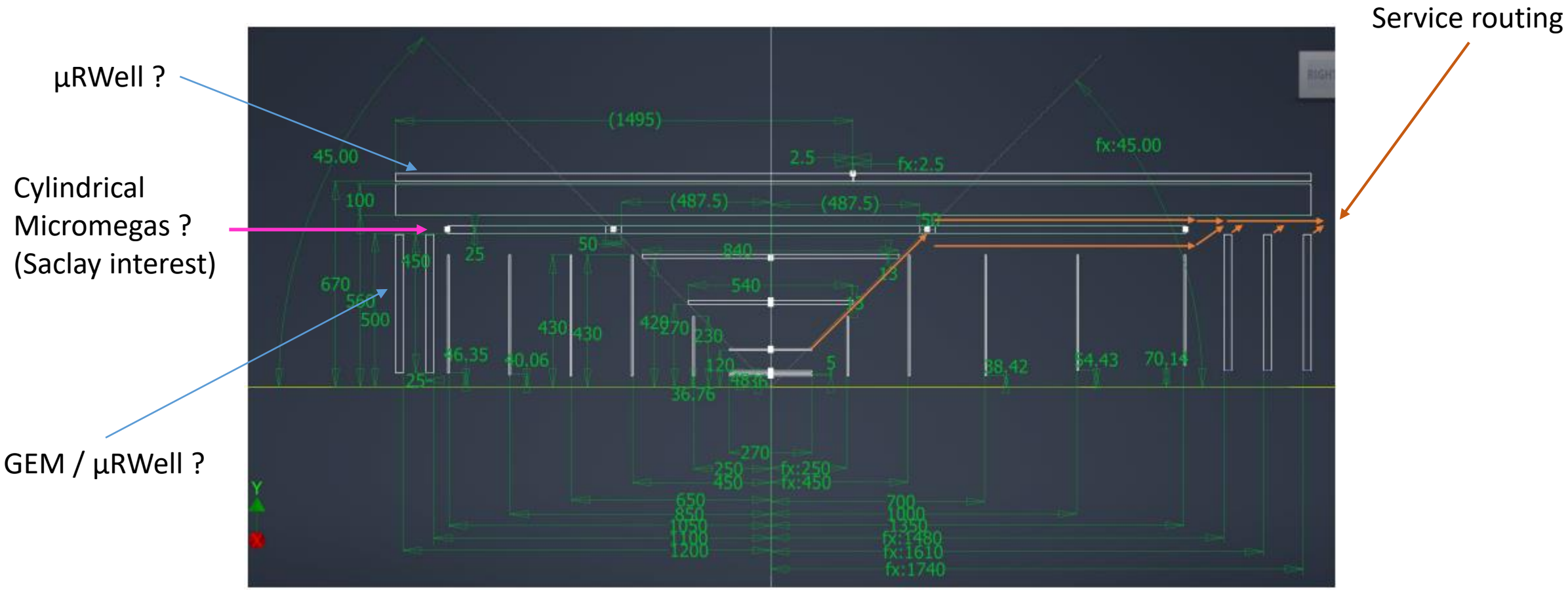
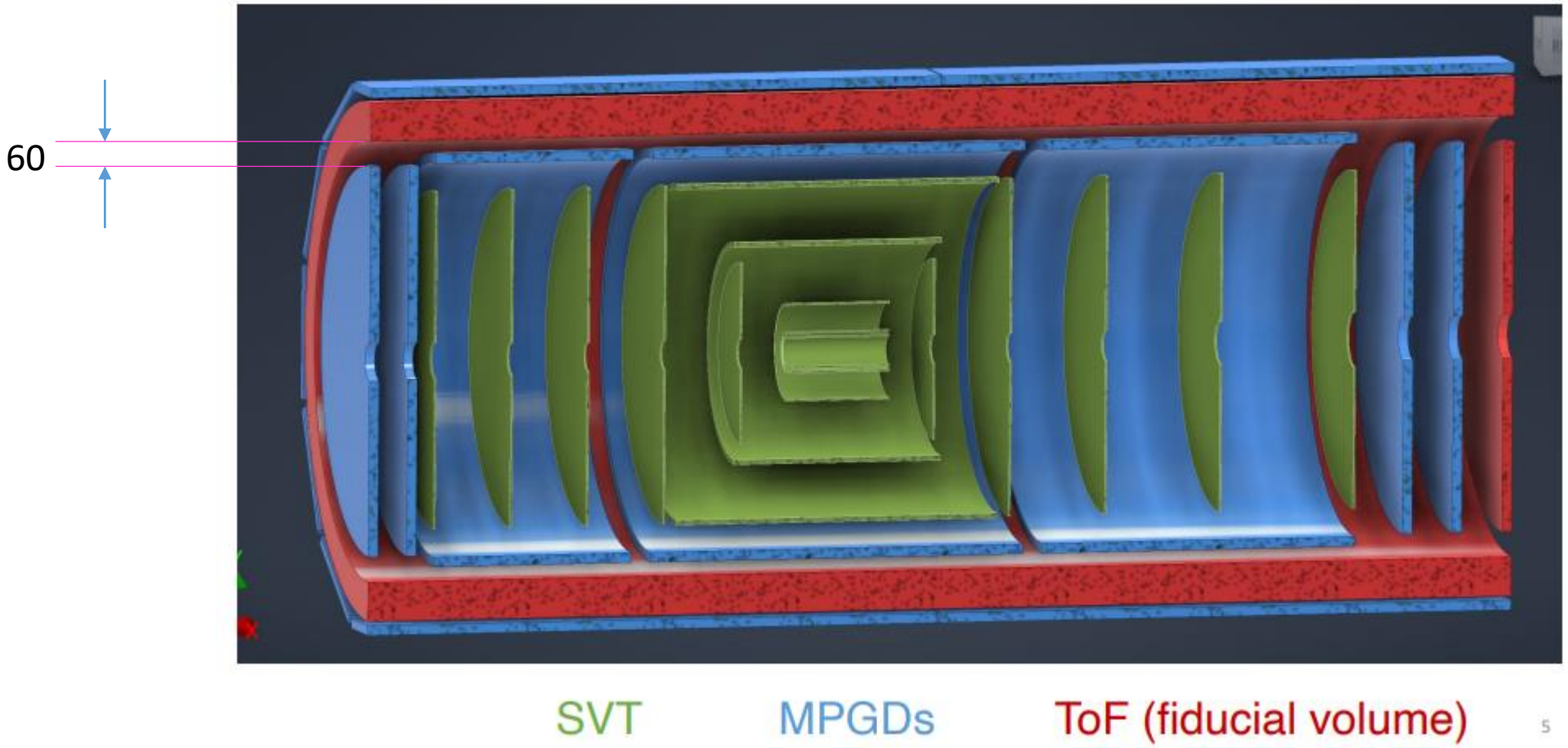



- A solid base for detector and readout definition
  - → Need to achieve quickly the same maturity as for Athena CyMBaL tracker
    - https://indico.bnl.gov/event/13103/contributions/55234/attachments/37448/61701/210930_EicAthena_Cymbal_v3.pdf

# Spatial constraints for inner barrel cylindrical tracker

- Space is stringent: 6 cm

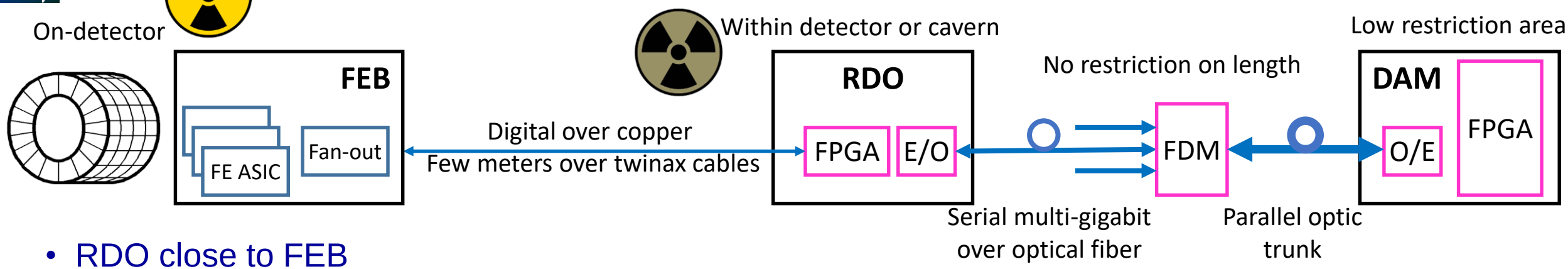
  → Detectors, gas pipes, HV cables




  → What about on-detector frontend electronics:

  - FEBs + LV distribution + RDO interface cabling + cooling
  - Will it fit within the space and material budget envelopes

# FEB location: on-detector




**FDM** – fiber distribution module (patch panels, etc.)

- RDO close to FEB
  - → Moderate radiation environment, space & power stringent
- RDO ↔ FEB
  - → Clock & synch commands – on FEB fan-out or multi-drop
  - → I2C – daisy chain
  - → Test
  - → Data – single or several uplinks per ASIC

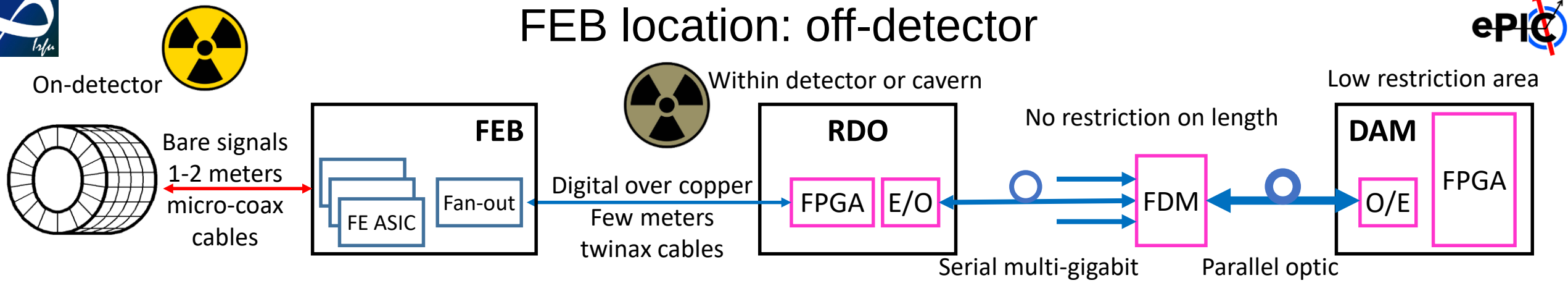
RDO ↔ FEB

Rafael

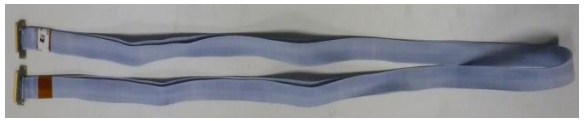
65nm PLL

- FEB
  - → No on-board intelligence, no board-level data aggregation
  - → High fidelity fan-out can be the Rafael ASIC or a development based on EICGENR&D_2022_06
    - Used solely for clocks and commands; not for I2C
- On detector FEB: best option for S/N
  - → Difficult for all the rest

# FEB location: off-detector




- Off-detector FEB: best for material budget
  - → Make sure S/N remains acceptable
    - Clas12: 2.2 m long lightweight micro-coaxial cables
      - 40 pF/m capacitance
      - Electronics designed for high capacitance detectors
    - Painful decision
  - → As a consequence, RDO can be placed further away from the detector



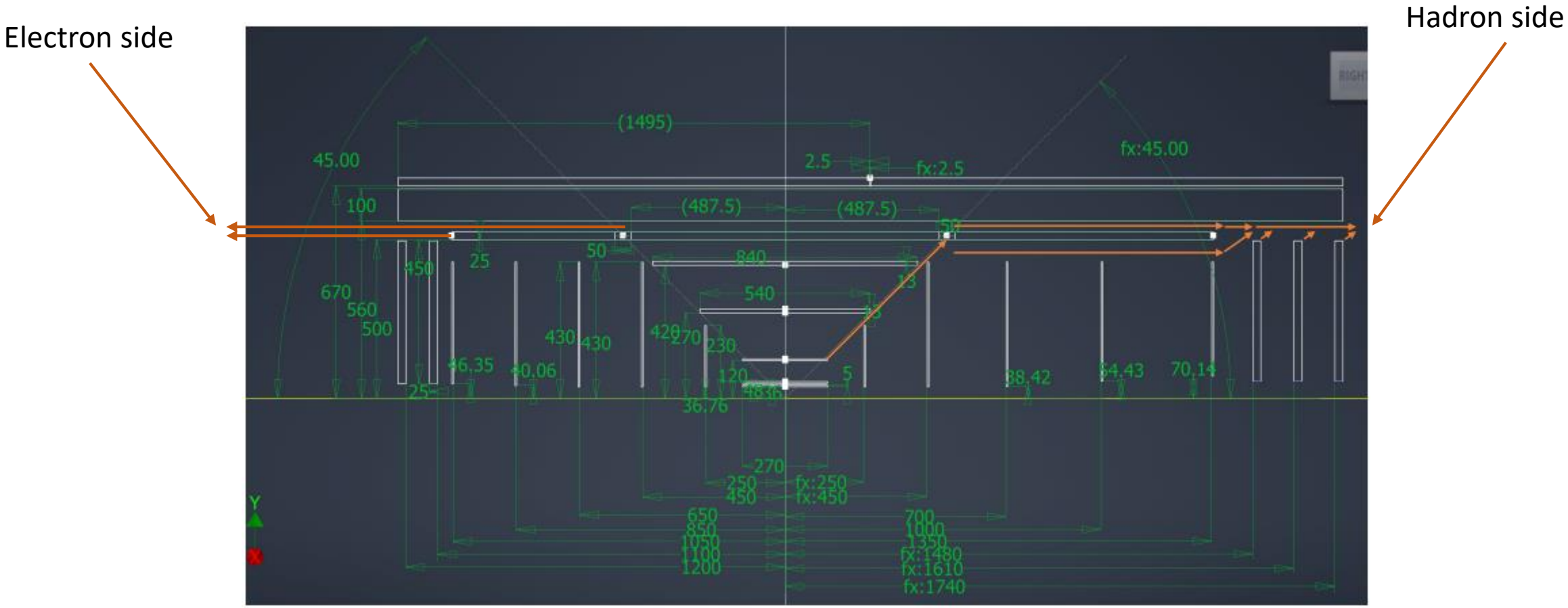
**FDM** – fiber distribution module (patch panels, etc.)

- Other options possible
  - → Analog on-detector fronted
  - → Combined off-detector FEB-RDO
  - → Optical interface between FEB and RDO

- Need a wider knowledge of available space to place electronics and services

# Where to get information about available space for electronics?

- Assuming off-detector FEB for space and material budget restrictions




- Place FEBs (hence corresponding RDOs) on both sides: hadron and electron
  → Detector cable length ~2 m
- FEB and RDO: magnetic field ?

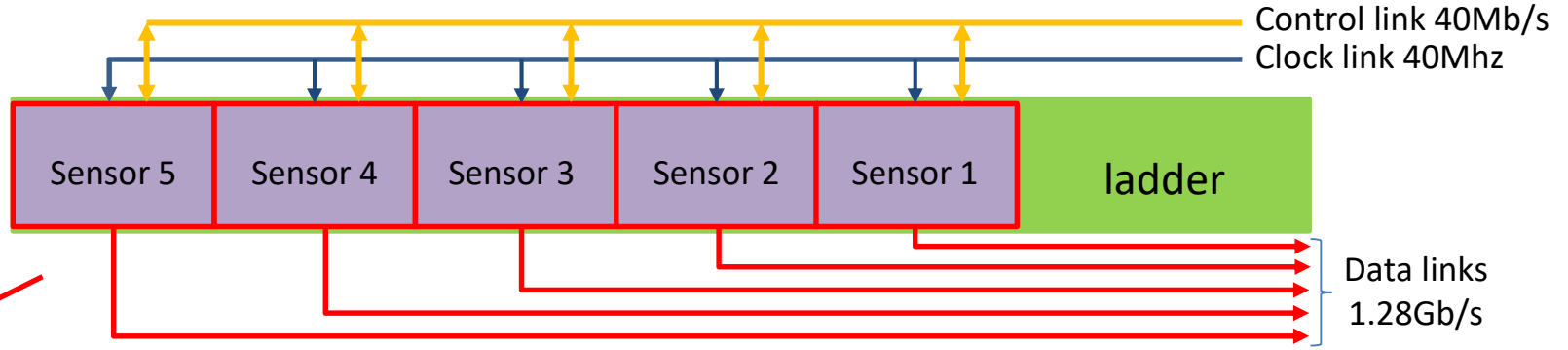
# FEB – RDO link

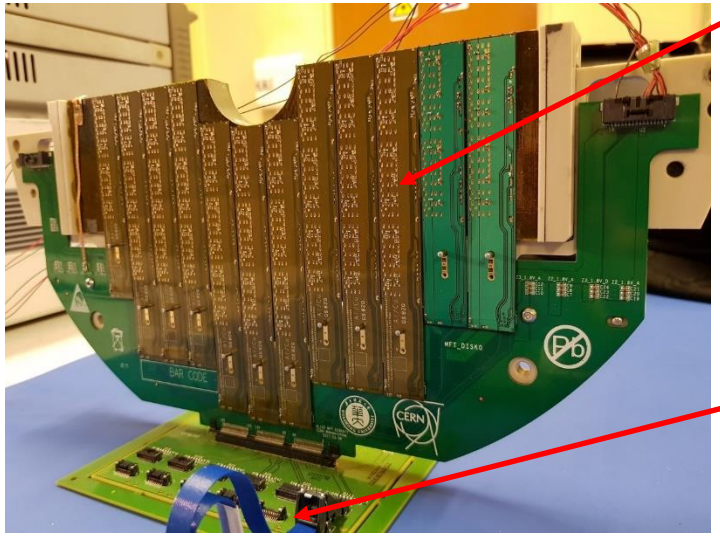
# Twinax copper cable performance example: Alice MFT

- Muon Forward Tracker: ladders with a variable number of ALPIDE silicon sensors

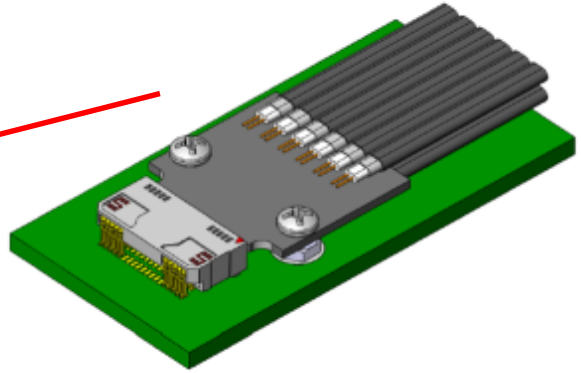
→ ALPIDE sensor: 512K pixels

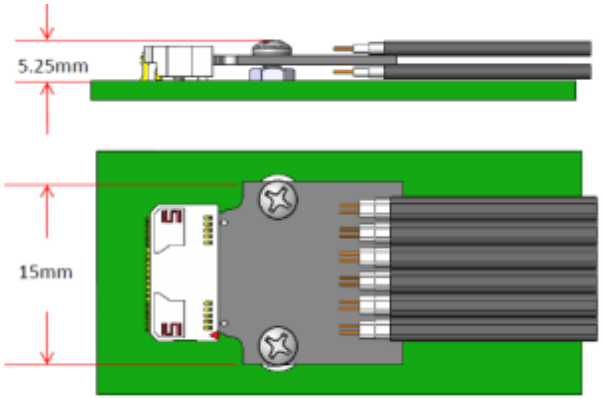
- Pixel = 29 x 27 $\mu m^2$
- ZS, triggered or continuous
- 1.28 Gbit/s upstream data link
  - Pre-emphasis capability
- 40 MHz clock
- 40 Mb/s control



Samtec 12-ribbon FireFly twinax cables with low profile connectors





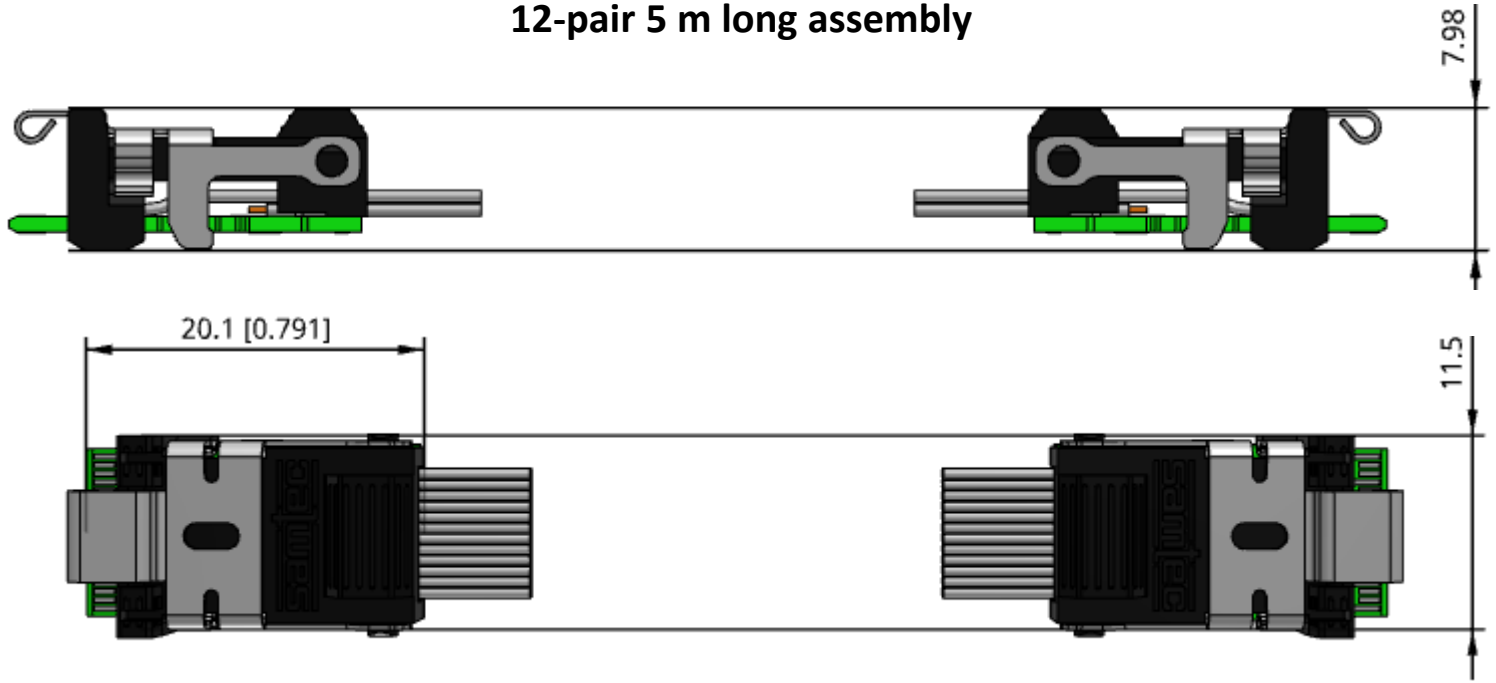

→ Signal integrity studies

- Up to 8m of cable and 9 connectors in the path
- Reliable communication with BER better than $10^{-14}$
  - Adjust pre-emphasis

# Twinax copper cable example: Samtec FireFly

- https://www.samtec.com/products/ecue
- https://suddendocs.samtec.com/catalog_english/ecue.pdf
- Configurable assembly
  - → 8 or 12 pairs
  - → up to 10 m
- Impressive signal integrity figures
  - → Qualified for 10-50 Gbit/s speeds

**Example of configured part number: ECUE-12-500-T1-FF-01-1**
**12-pair 5 m long assembly**

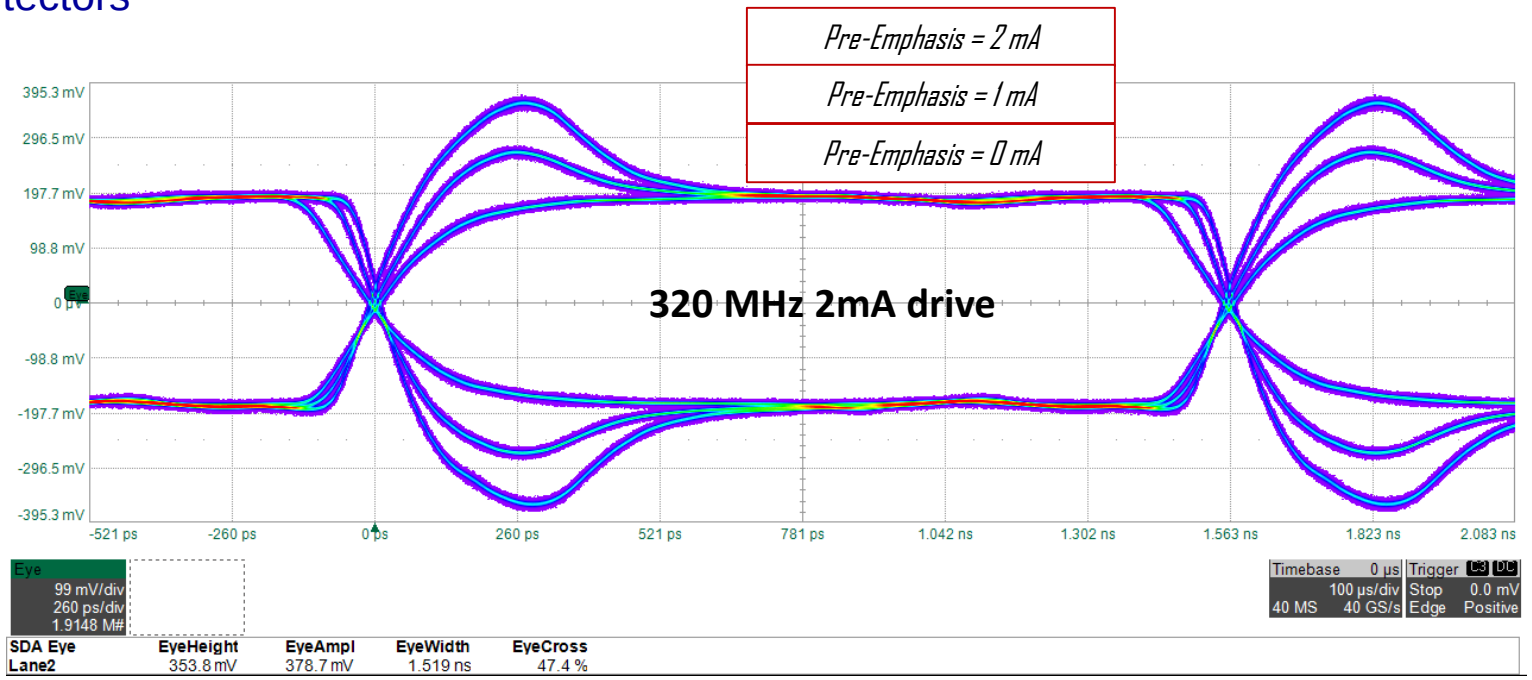



- Max length for O(1 Gbit/s) speed?
- Rigidity, weight?
- Flammability?
- Cost?

  - → Contact Samtec technical service
  - → R&D on data transmission and on clock / synchronous command distribution?

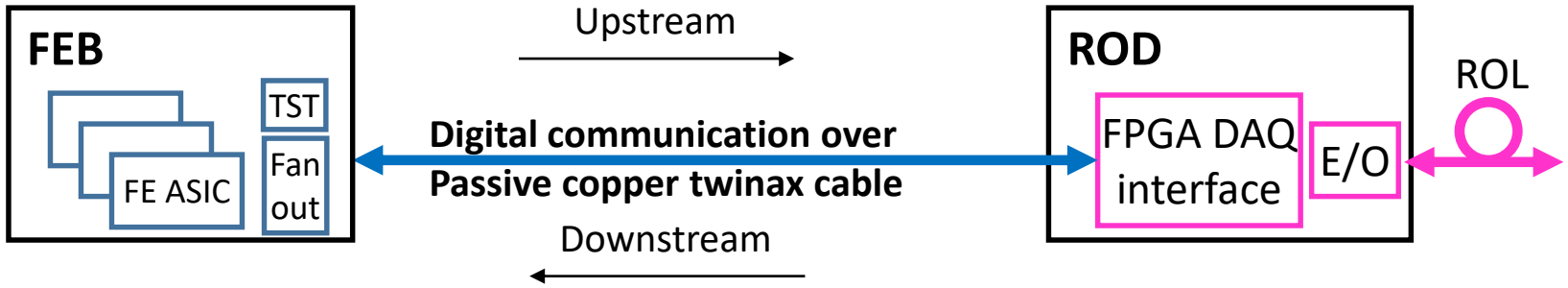
# Common practices to improve signal integrity on long transmission lines

- Drive strength choice of differential lines:
  - → 1 mA, 2mA, 4mA, 8mA
- Pre-emphasis strength and duration:
  - → 1 mA, 2mA
  - → 150 ps, 300ps
- Rafael clock/command fan-out example (more in backup and Rafael)
  - → 130 nm 3-to-1-to-13 radiation hard chip
    - Developed for CMS timing detectors
  - → 1.2 V
  - → CLPS differential
    - CERN low power
    - 200 mV, 400 mV diff swing
  - → Measurements over 2 m cable
    - Coaxial SMAs
  - → Additive jitter ~2 ps
    - Specs up to 400 MHz
    - Satisfies 640 MHz
    - Decent at 1.28 GHz
  - → Irradiation tests
    - 6 m SMA cables
    - 200 Mbit/s




Modern FPGA receivers equipped with circuitry to determine optimal sampling point
Error detection and correction sequences improve further BER figures

# FEB-RDO link MPGD example

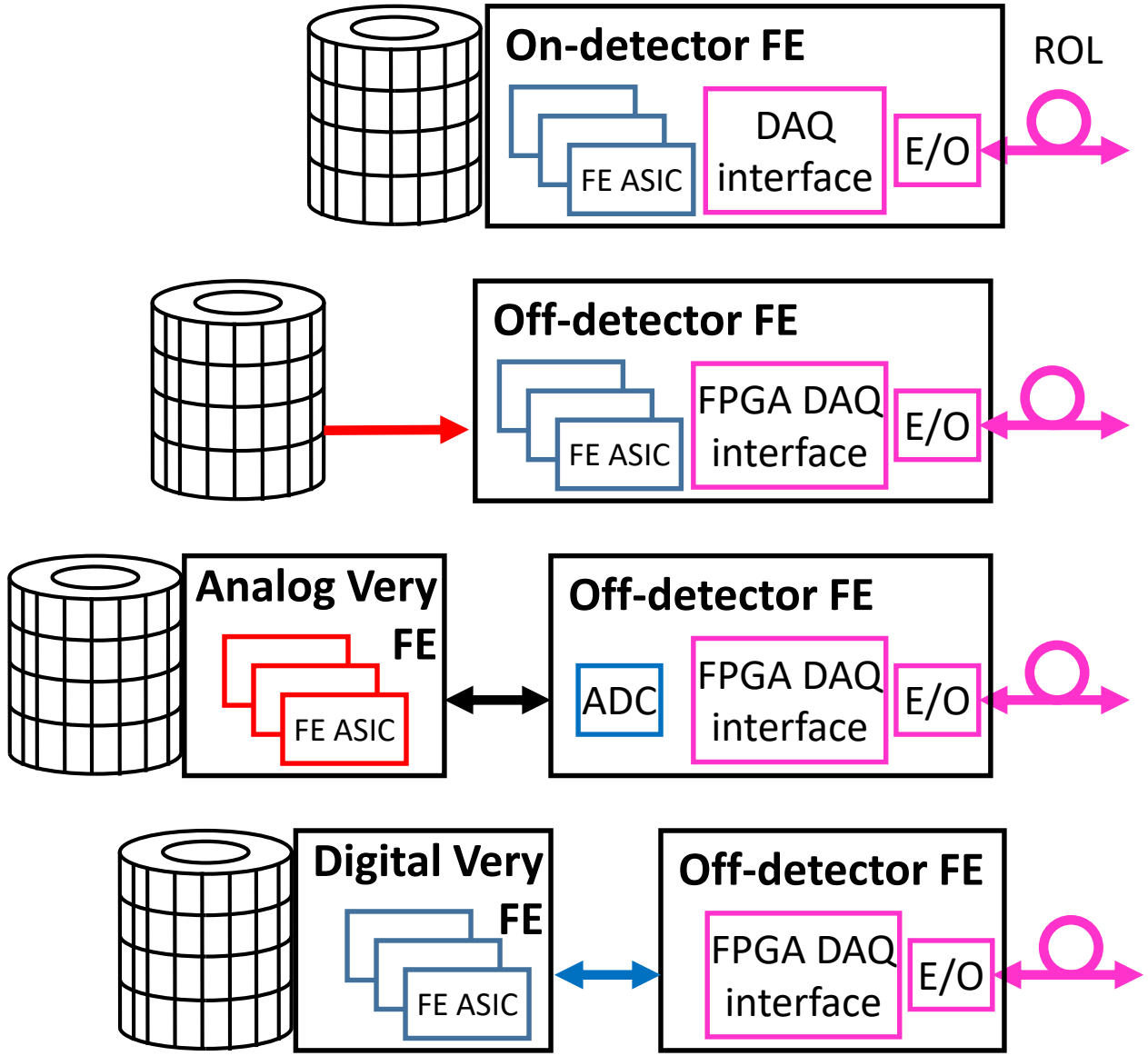



- 512-channel on-detector digital very FE
  - → 8 64-channel FE ASICs (*e.g.* future SALSA) with
    - 1 Gbit/s output data link
    - Unique system clock
      - On-board 1-to-8 fan-out
    - Synchronous command encoding trigger
      - On-board 1-to-8 fan-out
  - → Common on-onboard test pulse logic
    - Requires a test pulse
  - → Bi-directional I2C SDA + unidirectional I2C SDC
    - Chained
- Off-detector on-detector interface
  - → 3 downstream lines:
    - Clock, command, I2C SDC
  - → 8 upstream lines
    - 8 data links
  - → 1 bi-directional I2C SDA line
  - → Almost fits to single 12-pair Samtec FireFly copper cable
    - Test sequence may be initiated by I2C
- The FEB size (number of channels) to be adapted according to detector segmentation, available space …
  - → Number of pairs in FireFly can be less than

# Backup

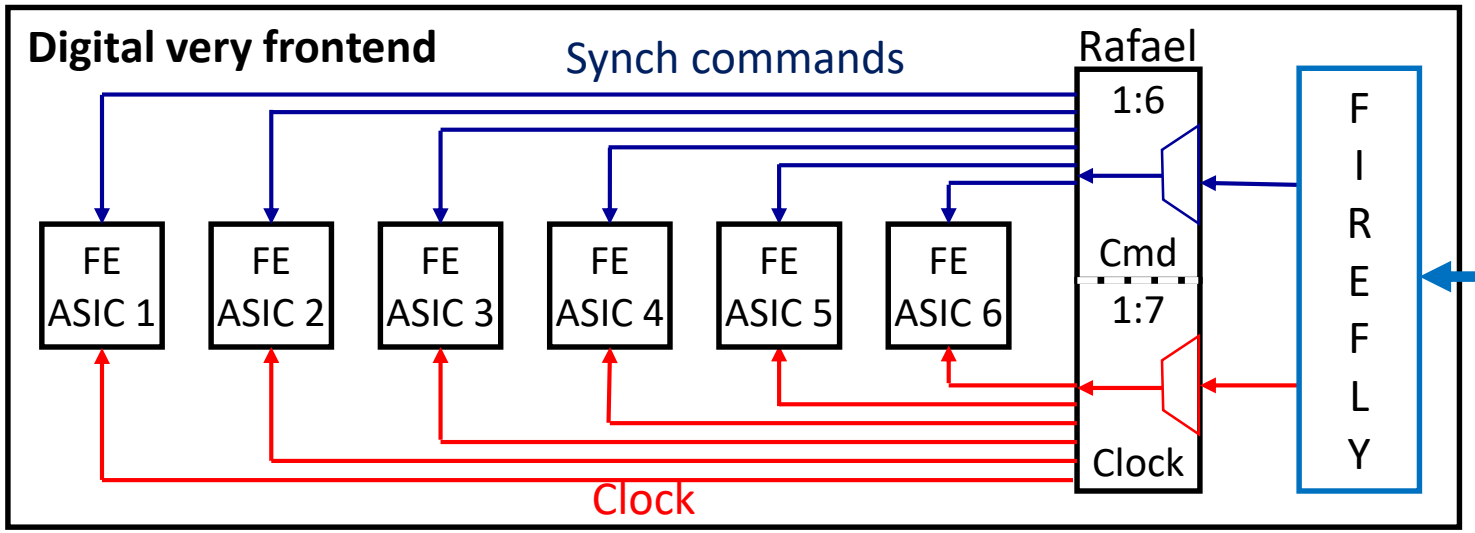
# Readout optical link for variety of frontends

- Whatever FE organization ROL must provide
  - → Communication with ASICs
  - → Communication proper to DAQ interface
    - Configuration, run control, monitoring
- DAQ interface: downstream to ASIC
  - → Clock: unique or multiple
    - Measurement – if not through dedicated “pure” path
    - Communication with ASICs
    - SCL line for I2C
  - → Synchronous commands for ASICs
  - → Slow control
    - I2C SDA chain
      - + multi-drop I2C SCL
  - → Auxiliary
    - Trigger, test sequence
      - If not part of synchronous commands
- DAQ interface: upstream from ASIC
  - → Acquisition data
    - Point-to-point
      - N ASICs x M output links per ASIC
  - → Slow control
    - If I2C SDA line cannot be bi-directional



# Clock and fast command distribution example

- Rafael - Radiation-hArd Fan-out ASIC for Experiments at LHC - developed at Irfu, CEA Saclay
  - → 3 inputs and 13 outputs
  - → CLPS signaling
    - CM voltage: 0.6 V
    - Differential swing: 200-400 mV
    - Programmable drive and emphasis
  - → Single buffer: any input to 13 outputs
  - → Double buffer
    - Input 1 to 6 outputs
    - Input 2 to 7 outputs
  - → Up to 400 MHz and beyond
  - → Low additive jitter of < 2 ps
  - → LHC-level TID, neutron, SEU
  - → 130 nm technology
  - → Possibility to embed a PLL
    - If no jitter cleaner PLL in ASICs




- Commercial counterparts
  - → IDT 8P34S2108: https://www.renesas.com/eu/en/document/dst/8p34s2108-datasheet
  - → TI CDCLVD1216: http://www.ti.com/lit/ds/symlink/cdclvd1216.pdf