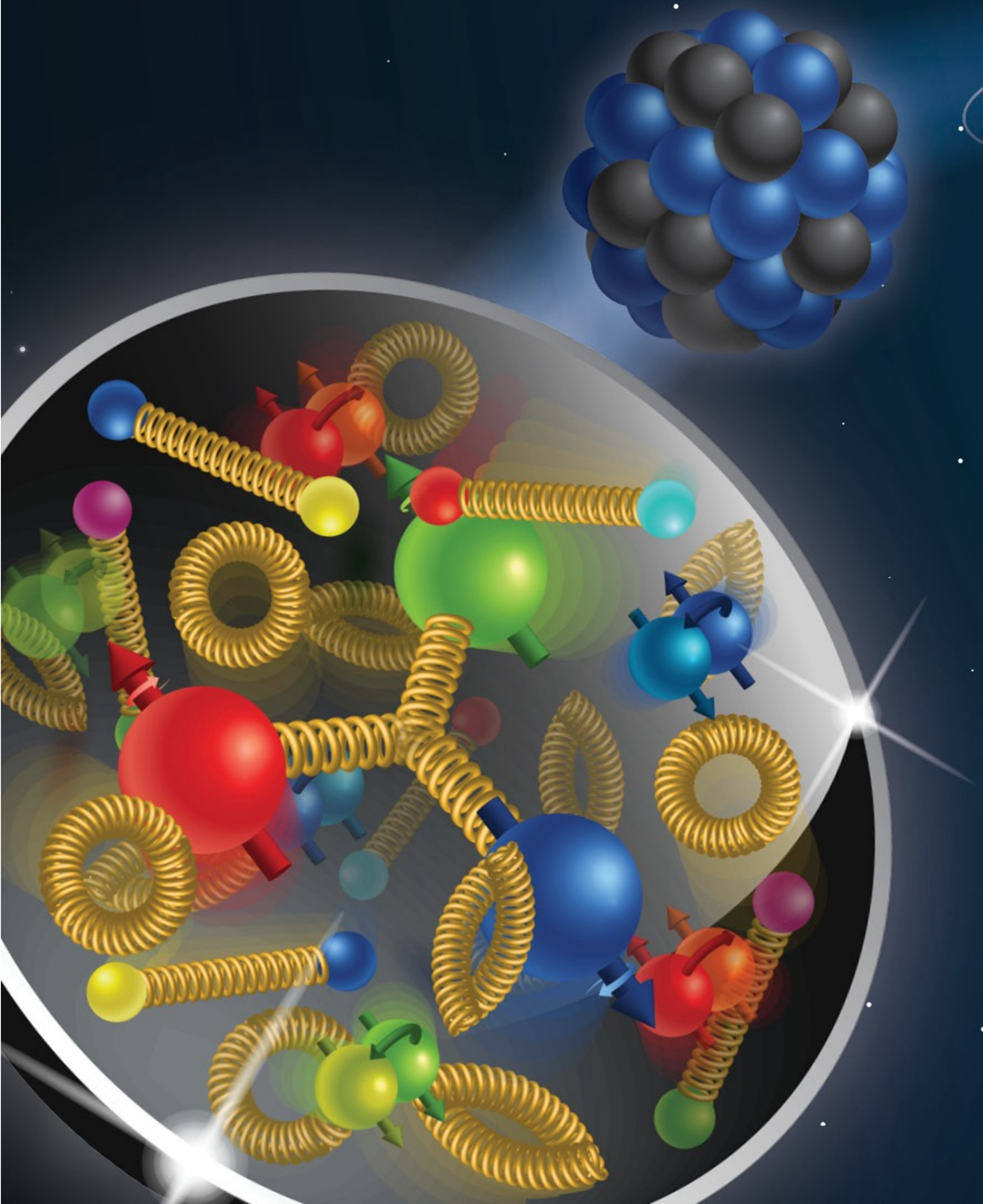


WBS 6.10.03
Tracking Detectors

Brian Eng (JLab)

EIC Detector Comprehensive Design Review

August 29-30, 2023

Electron-Ion Collider

BROOKHAVEN NATIONAL LABORATORY
Jefferson Lab
U.S. DEPARTMENT OF ENERGY | Office of Science

Outline

- Charges
- Requirements
- Layout
- Details
  - Inner Barrel
  - Outer Barrel
  - Disks
- Services
- Interfaces
- Schedule
- Conclusion

Charges

1. Given the detector progress over the last two years and the status of the ePIC detector, are the projected timelines of the Electron-Ion Collider detector feasible? Do there remain significant open detector technology questions?
2. Are the requirements for the detector and their flow down sufficiently comprehensive for this stage of the project to complete the design of the various detector technologies?
3. Are the interfaces between the elements of the design adequately defined for this stage of the project and to proceed with the detector long-lead procurement items?
4. Is the design of these long-lead procurement items sufficiently advanced and mature to start procurement in 2024? Are the technical specifications complete?
5. Is the projected design maturity of the further detector components likely to be accomplished by the end of 2024 for CD-2 and CD-3?
6. Is the overall schedule for completion of the design, production, and installation of detector components realistic?

Charge #2

Requirements

- https://eic.jlab.org/Requirements/index.html

	Momentum Resolution	Spatial Resolution
Backward (-3.5 to -2.5)	$\sim 0.10\% \times p \oplus 2.0\%$	$\sim 30/p_T\ \mu m \oplus 40\ \mu m$
Backward (-2.5 to -1.0)	$\sim 0.05\% \times p \oplus 1.0\%$	$\sim 30/p_T\ \mu m \oplus 20\ \mu m$
Barrel (-1.0 to 1.0)	$\sim 0.05\% \times p \oplus 0.5\%$	$\sim 20/p_T\ \mu m \oplus 5\ \mu m$
Forward (1.0 to 2.5)	$\sim 0.05\% \times p \oplus 1.0\%$	$\sim 30/p_T\ \mu m \oplus 20\ \mu m$
Forward (2.5 to 3.5)	$\sim 0.10\% \times p \oplus 2.0\%$	$\sim 30/p_T\ \mu m \oplus 40\ \mu m$

Summary on ITS-3 ALICE – EIC SiC

Overall a very positive and successful meeting → clear goal to cooperate as much as possible in boundary conditions.

Main lessons learned and next steps

- ITS3 open to sharing their sensor design with EIC → necessary agreements will need to be put in place in the next month.
- ITS3 development made significant progress → received a lot of critical technical information to guide the next steps in R&D for both sensor and system design/integration of the ePIC SVT
- but there remains still some risk in the ITS development → ALICE team will need to remain focused on their requirements and timeline challenges

  → ITS3 welcomes/seeks partnership in development with EIC designers contributing to ITS3

  → Received extremely valuable input to overall schedule and workforce needs for EIC SVT

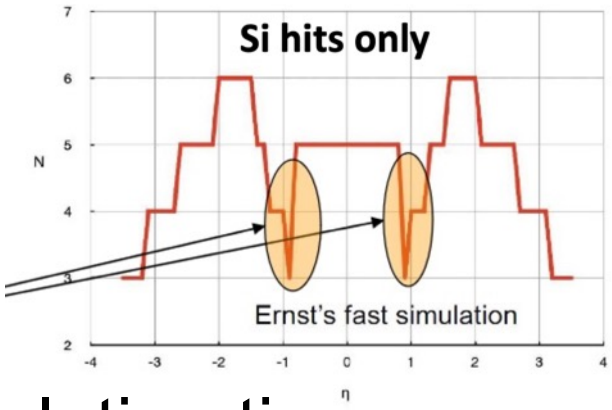
  Example: relation between schedule for ITS3 ER2/ER3 submission and evaluation and the EIC/LAS development schedule → adjust our schedule to give more time for the sensor modifications and the schedule and integrate lessons learnt from ITS3

  → ITS3 suggests we put in place a backup plan as our workforce is still growing, and the overall EIC SVT schedule is aggressive
- All the inputs are currently folded in an updated plan by the EIC SVT team

Updates will be presented in the respective ePIC meetings (TIC & TWG) by the SVT team

Charge #1

Tracking Detector Layout Modifications

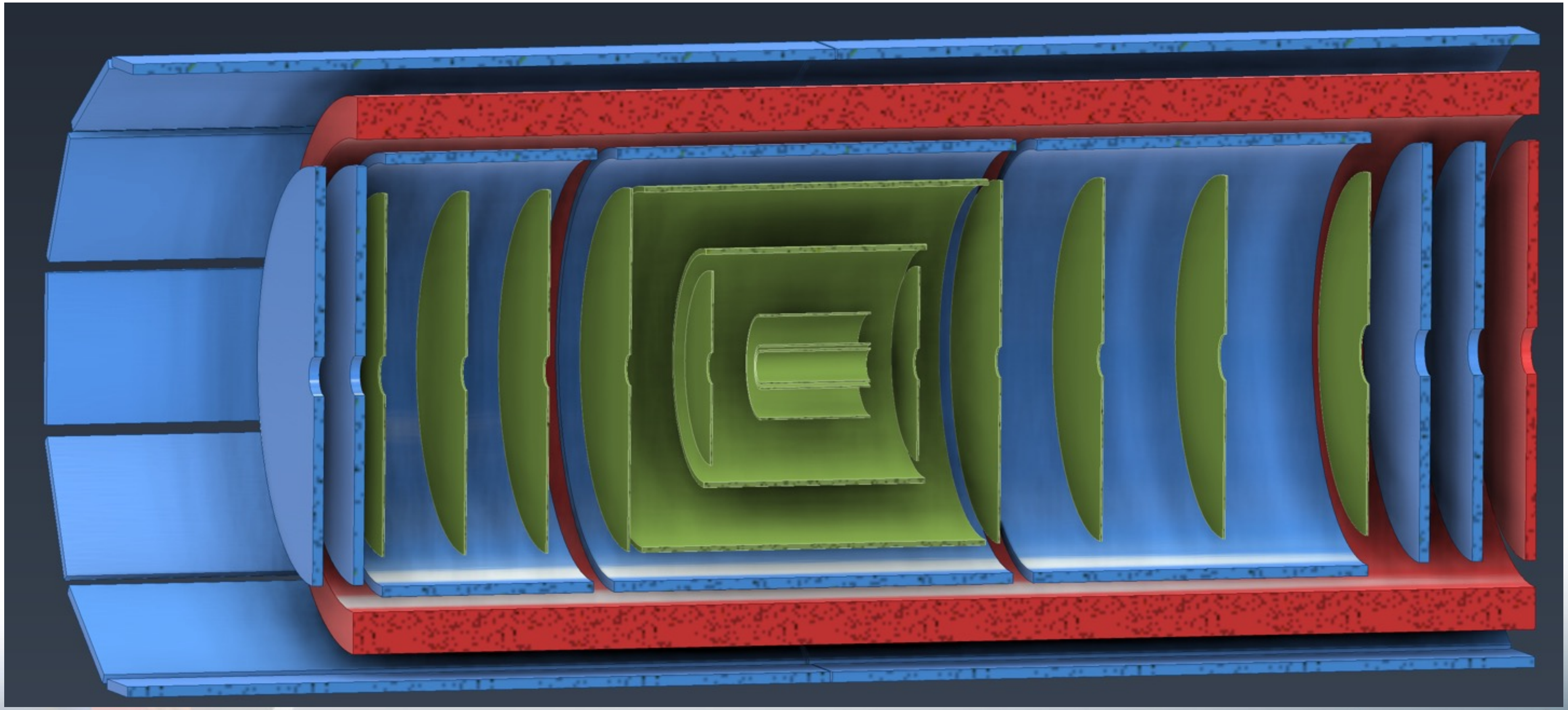


- Low number of hits in certain rapidity ranges
  - Need more planes
- Solve impact from 5 (2) μs MAPS frame accumulation time
  - Need enough hits from fast detectors to form a tracklet with a good pointing resolution
  - Need to utilize ToF and maybe Barrel-ECal AstroPix as possible
    - Note: Barrel ToF has good t-resolution but spatial resolution is not not to great
- Current layout finalized in June 2023

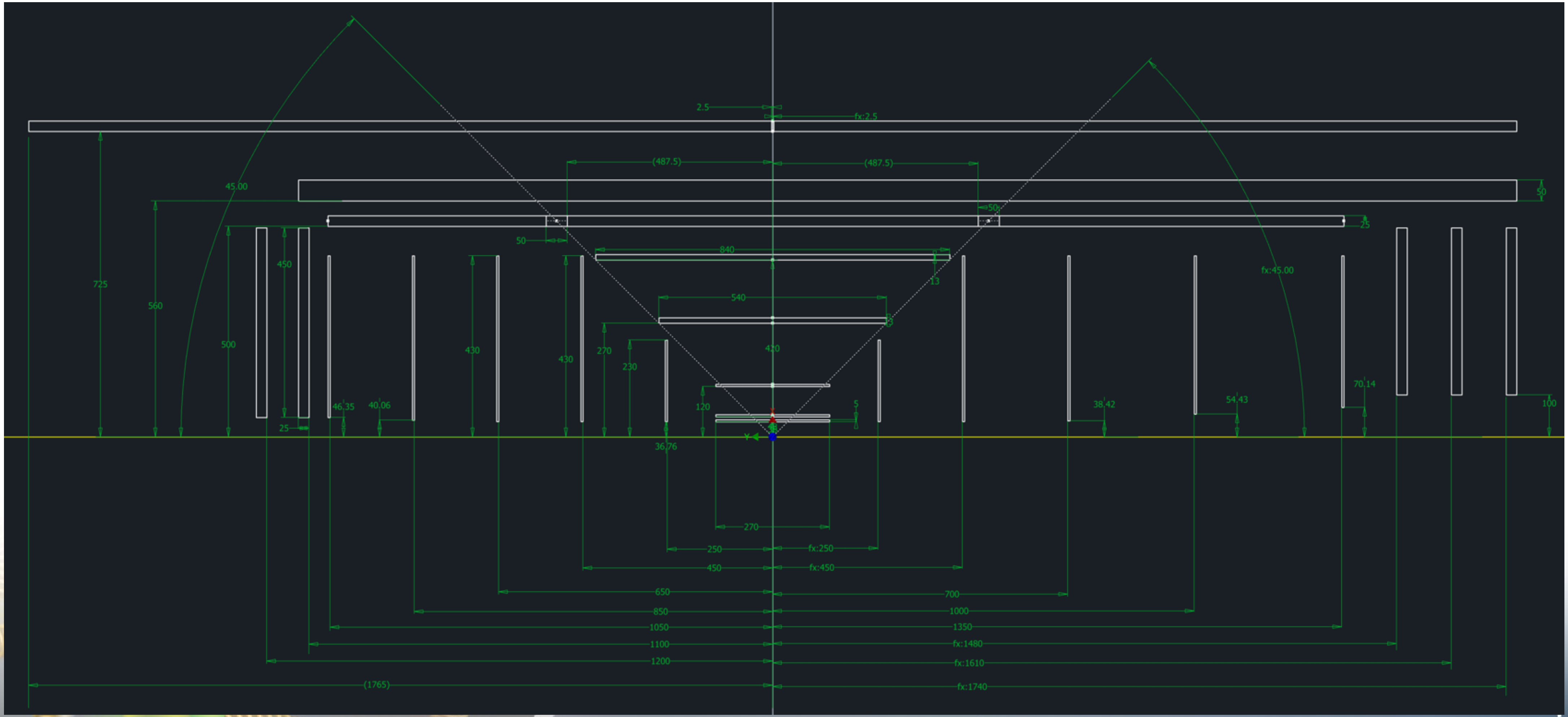
Charge #1

Tracking Detectors Layout

- Silicon
- MPGD
- ToF
  - PID WBS

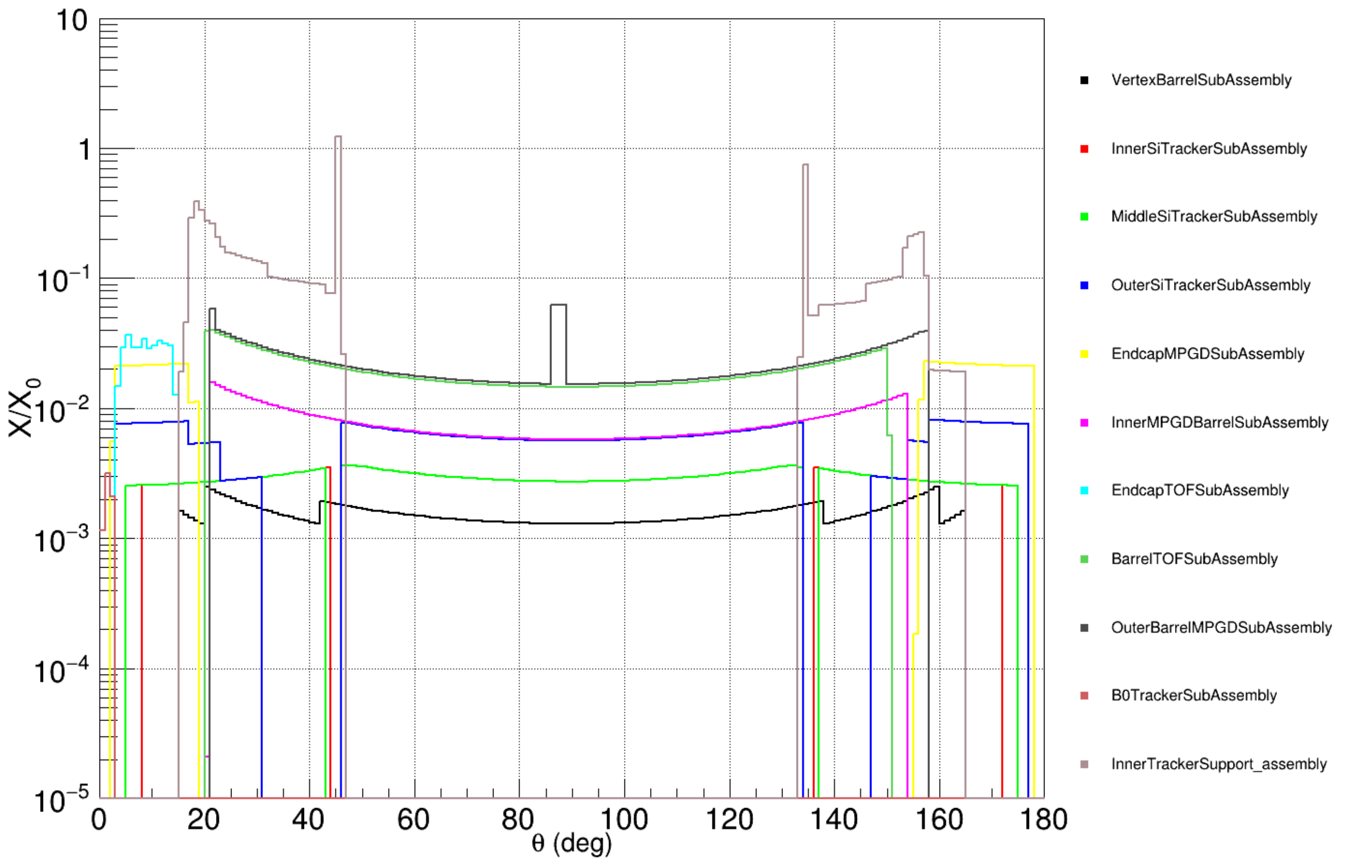


Tracking Detectors Layout



Electron-Ion Collider

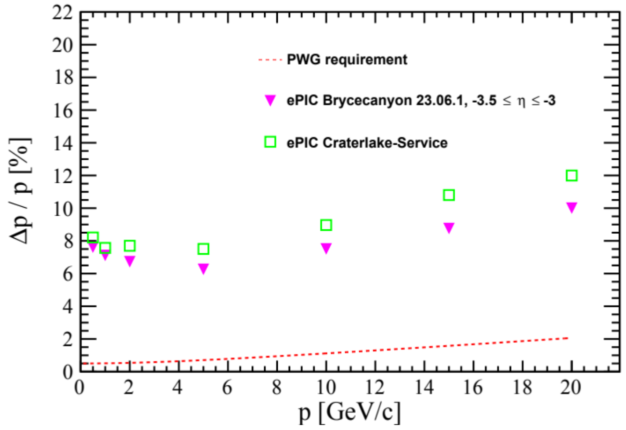
Simulation – Material Scan

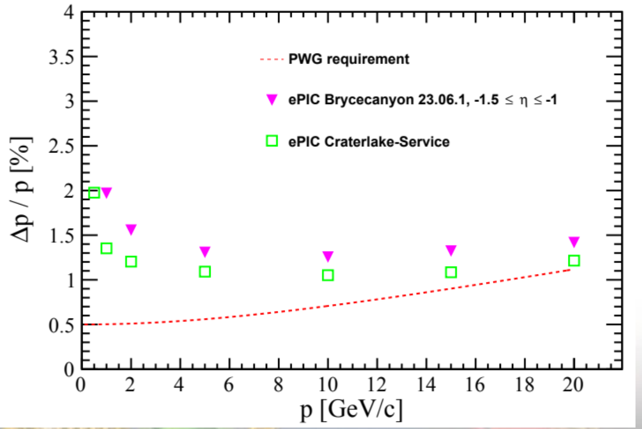


Volume Name	Material Budget
VertexBarrelSubAssembly	0.00130081
MiddleSiTrackerSubAssembly	0.0027159
OuterSiTrackerSubAssembly	0.00572107
InnerMPGDBarrelSubAssembly	0.00577311
BarrelTOFSubAssembly	0.0146295
OuterBarrelMPGDSubAssembly	0.0153859
InnerTrackerSupport_assembly	0
BeamPipe_assembly	0.00364154
EndcapMPGDSubAssembly	0.0212798
EndcapTOFSubAssembly	0.0279914

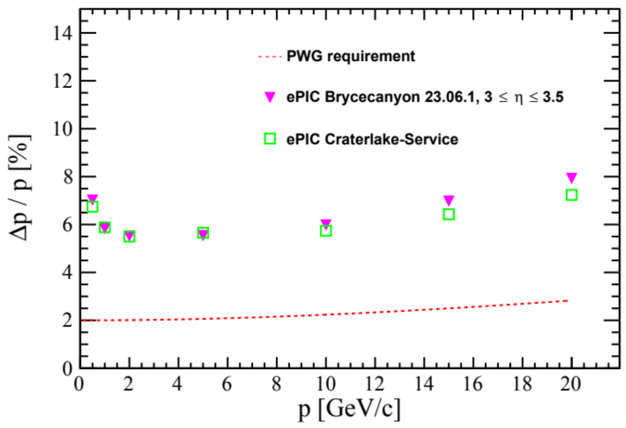
Simulation – Momentum Resolution

Backward



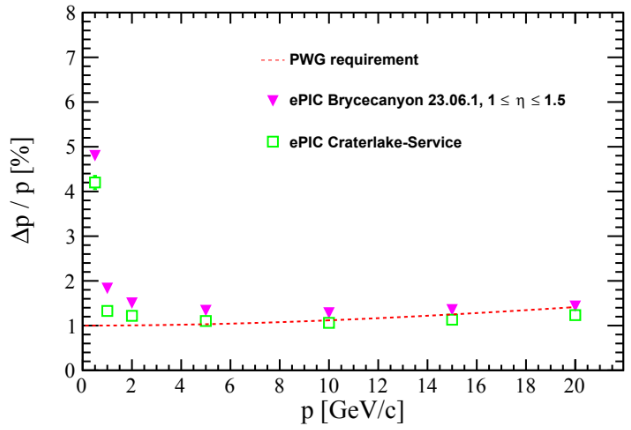


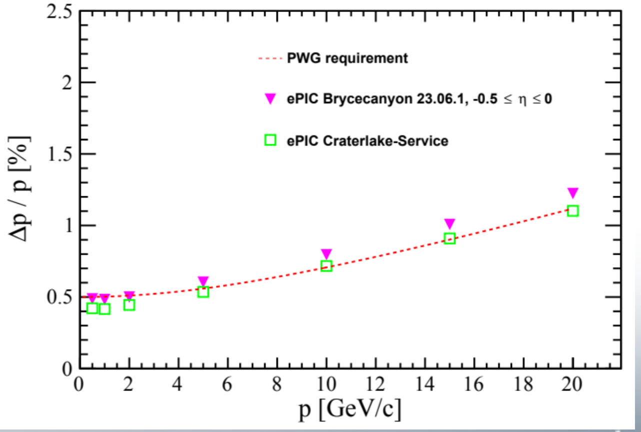
Central



- Fixed Energy Pions, flat in η
- Brycecanon = old layout
- Craterlake = new layout

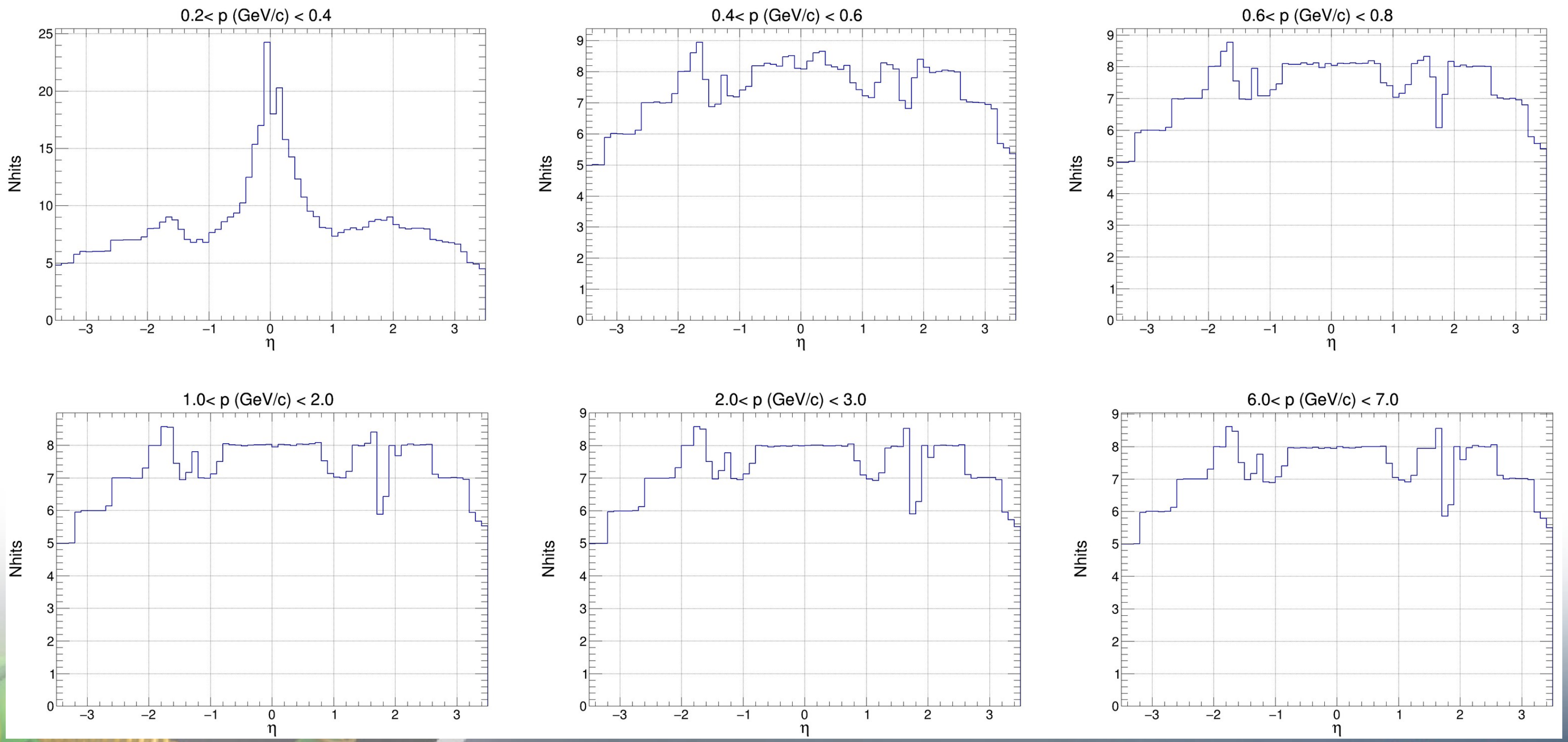
Forward





Simulation – Nhits vs η

- Only tracking detectors included, will improve further once calorimeters included, removes dip at rapidity ±1



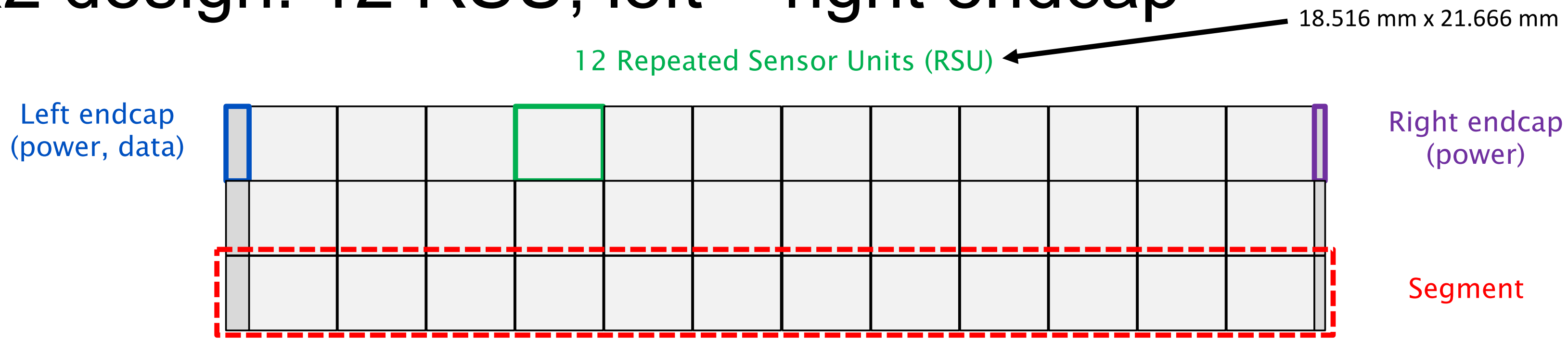
Charge #5

Silicon

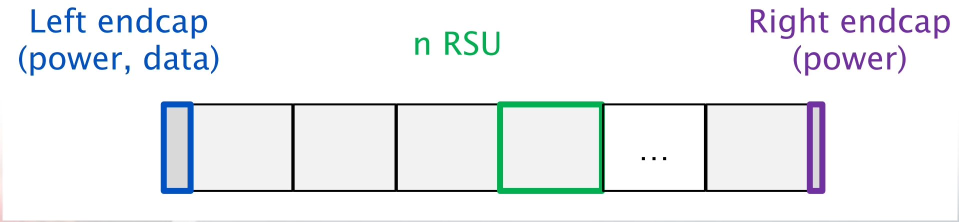
- MAPS (monolithic active pixel sensors) in 65 nm CMOS technology, developed with ALICE ITS3 collaboration
  - Inner Barrel: Directly use ITS3 wafer scale sensor
  - Outer Barrel: EIC Large Area Sensor (LAS), modification of ITS3 sensor
- ITS3 Sensor Development
  - MLR1 – Q4 2020: prototype circuit blocks
  - ER1 – Q4 2022: MOSS and MOST sensors, proof of principle, stitching
  - ER2 – Q1 2024: sensor to satisfy ITS3 requirements
  - ER3 – Q2 2025: final production

Silicon

- ITS3 ER2 design: 12 RSU, left + right endcap



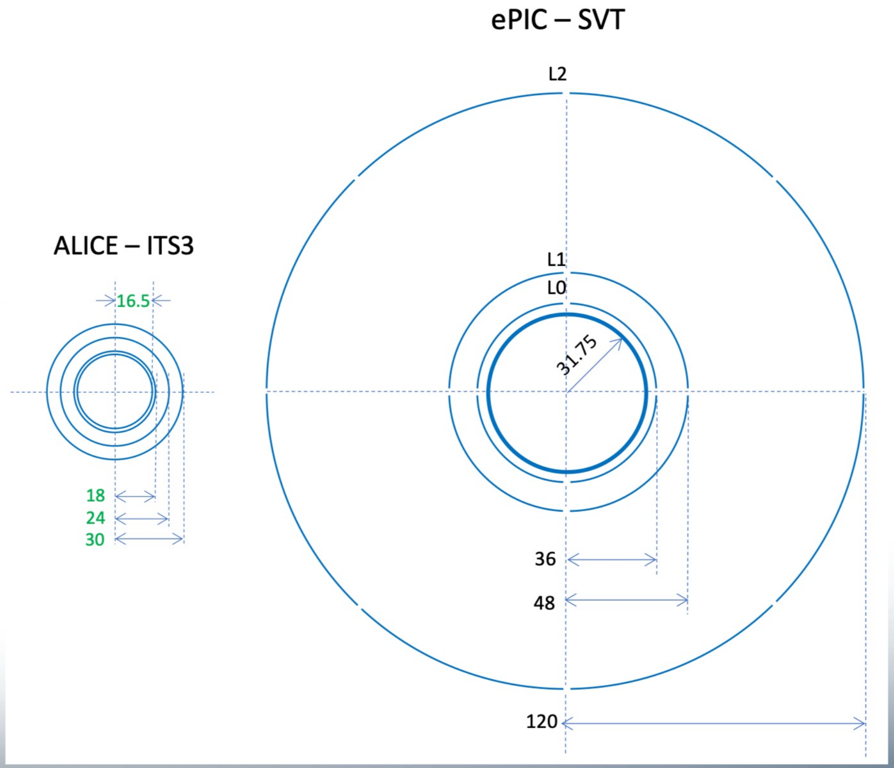
- Large Area Sensor (LAS) optimized for high yield, low cost, large area coverage



Inner Barrel

- Three layers of thin, bent, wafer scale ITS3 based sensors
- ITS3 concept adapted to ePIC radii
- X/X0 % = 0.05

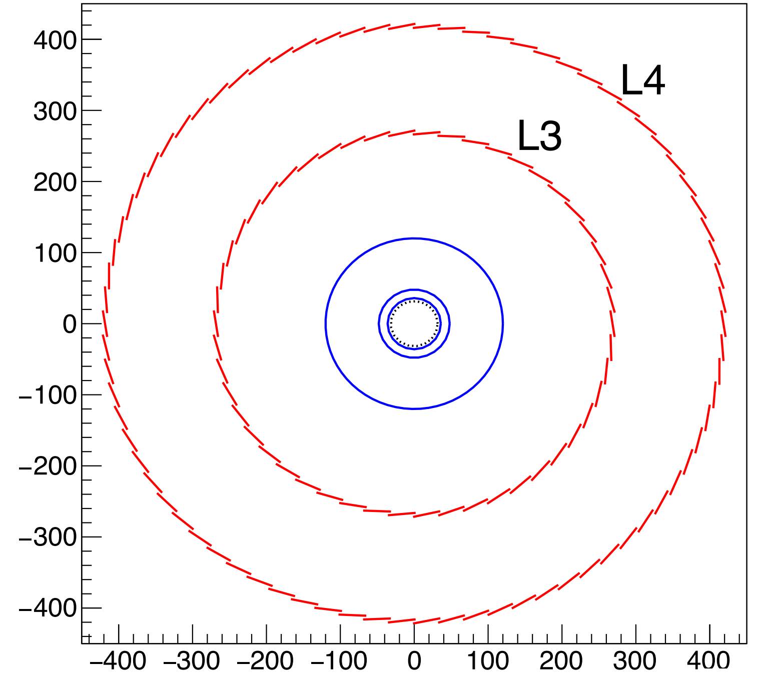
Layer	Radius (mm)	Length (mm)	Segments
L0	36	270	3
L1	48	270	4
L2	120	270	5



Outer Barrel – Silicon

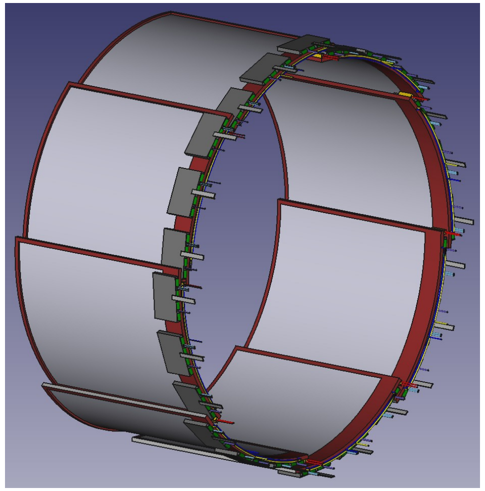
- Traditional stave design

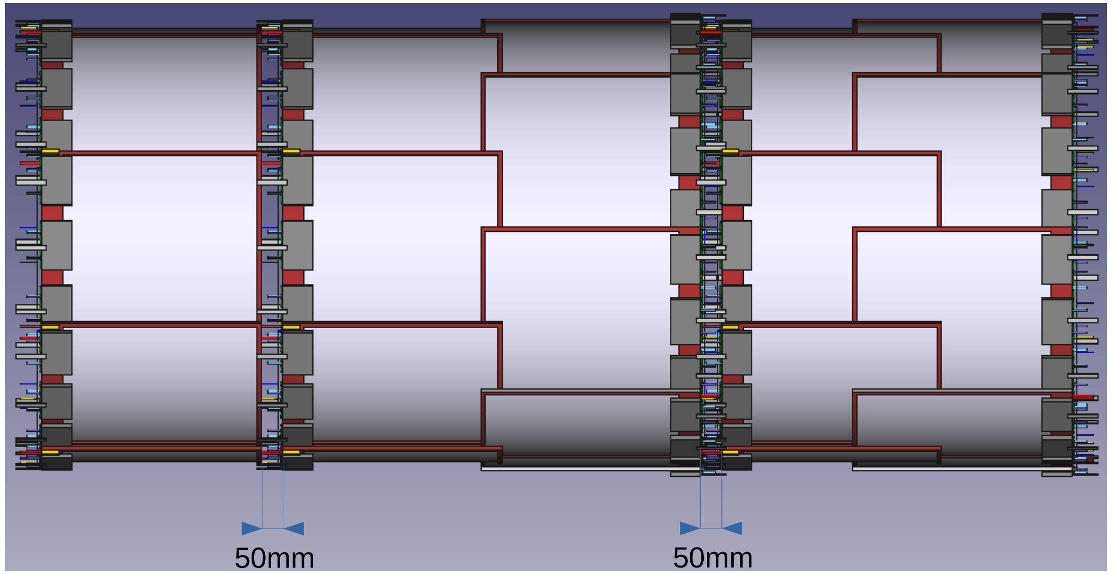
Layer	Radius (mm)	Length (mm)	X/X0%
L3	270	540	0.25
L4	420	840	0.55



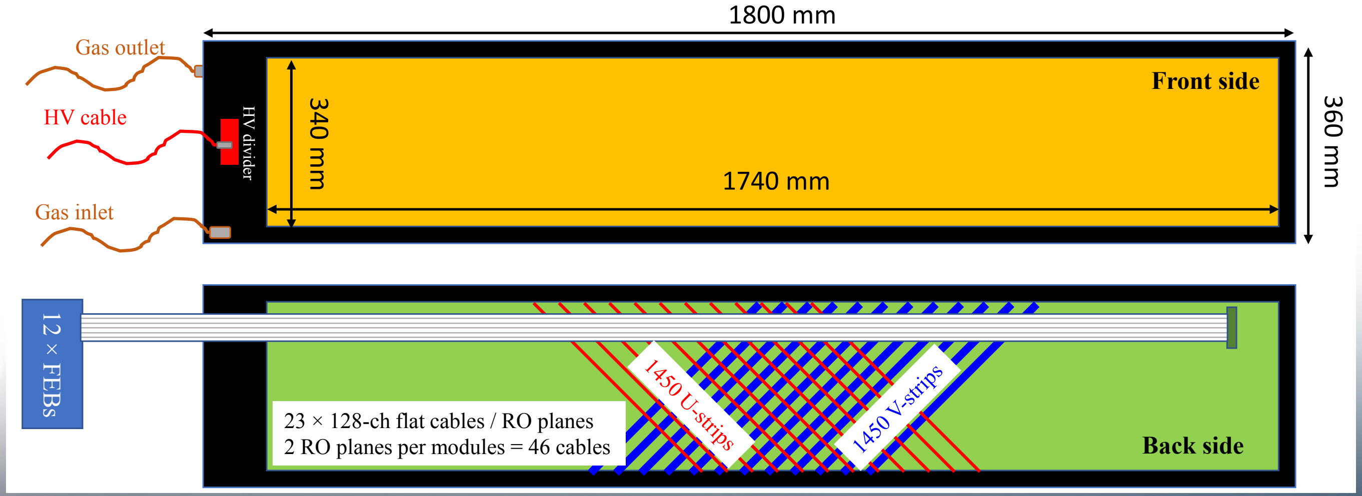
Outer Barrel – MPGD

- Micromegas
- Single Tile
  - 51.25 x 44 cm
  - Simplifies production
  - 40 Tiles Total
  - ~30k Channels



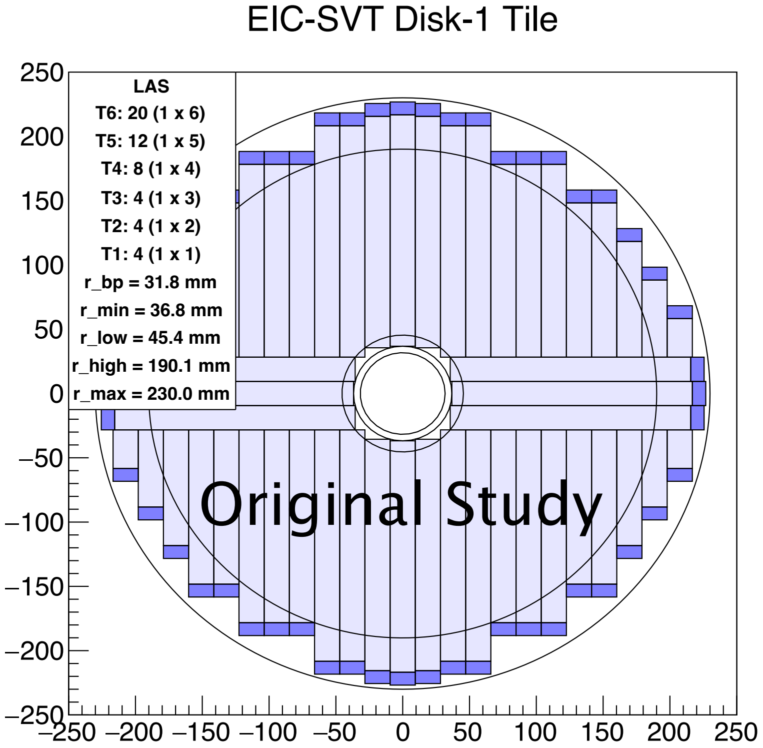


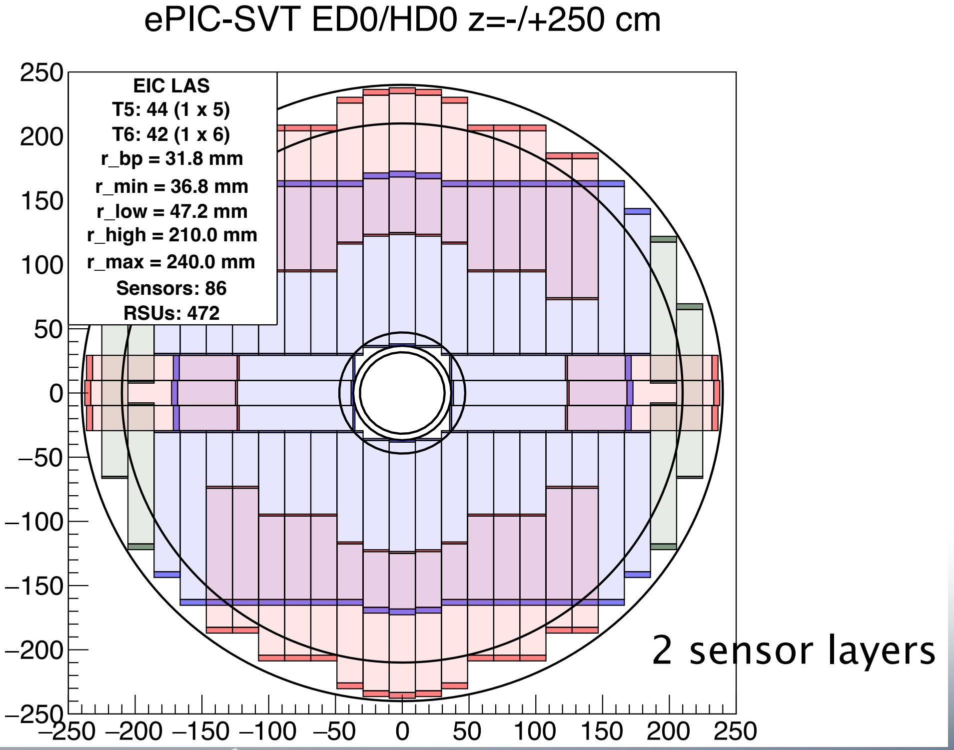
- uRWELL
- Capacitive-sharing 45° U-V strips
  - Pitch: 1.2 mm pitch
  - ~140k Channels



Forward/Backward Disks – Silicon

- Foundry rule/limitation, need to limit number of sizes (2-3 total)

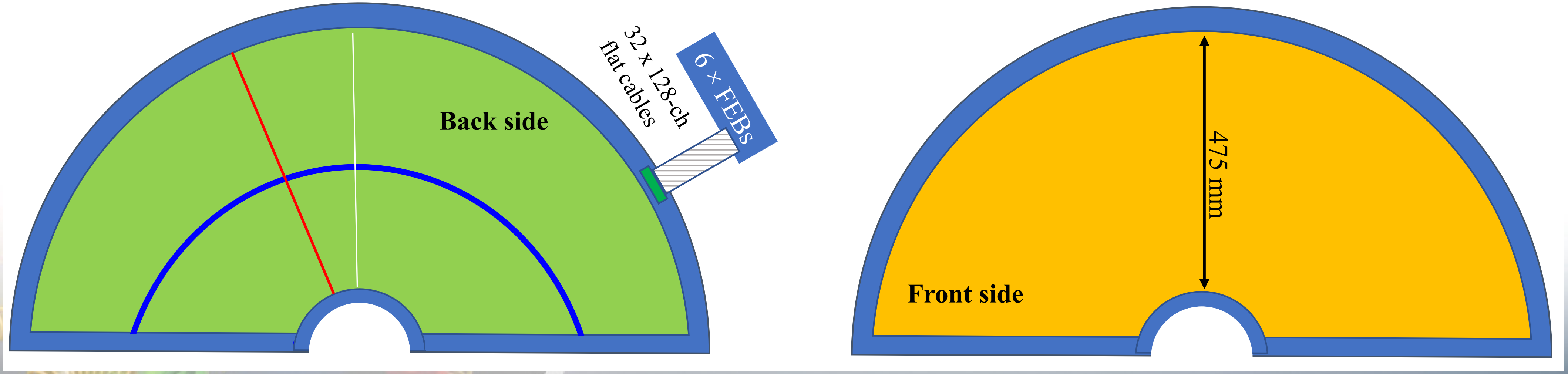




Electron-Ion Collider

Forward/Backward Disks – MPGD

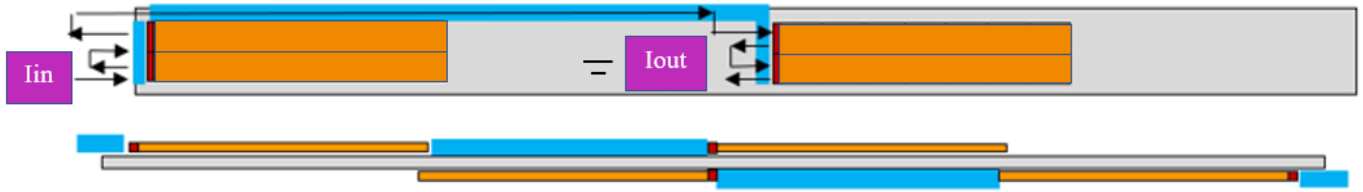
- Capacitive-sharing 45° r-phi strips
- Pitch: 1.2 mm pitch
- ~2 × 1570 phi-strips + ~ 2 × 400 r-strips = ~4k strips per disk (32k channels for 8 disks)



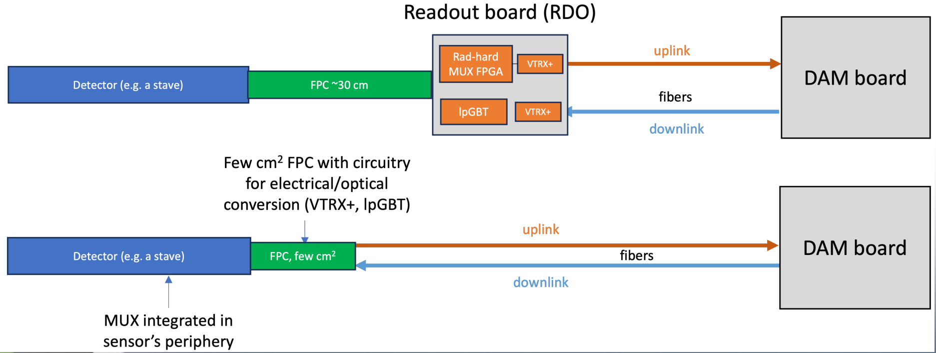
Electron-Ion Collider

Services – Silicon

- Power: OB/Disks use serial power via constant current scheme
  - Shunt-LDO regulators convert current into voltage needed by LAS
  - External (but close) to LAS sensors

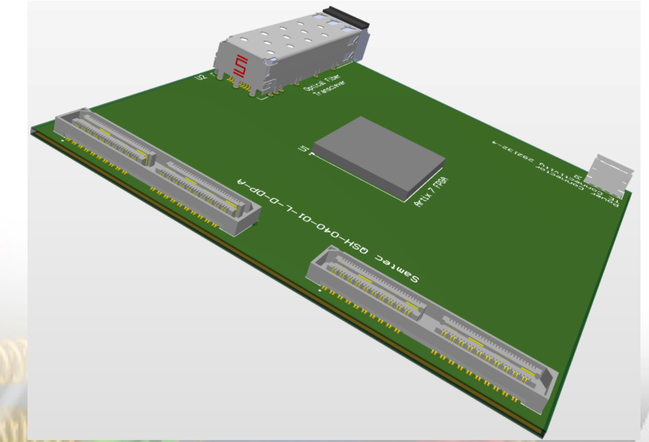


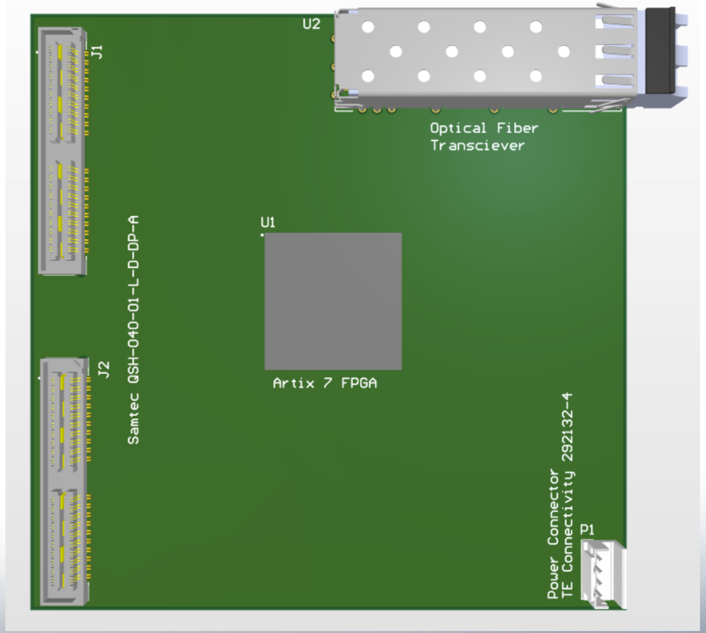
- Readout: optical links
  - ITS3 uses multiple 10Gbps links, not needed for ePIC
  - Multiplex externally (Rad-hard FPGA) or internally (modification to sensor itself)



Services – MPGD

- Common ASIC for all MPGDs: SALSA
  - Initiative of Sao Paulo University (USP) and CEA Saclay (IRFU)
    - Previous chips: USP – SAMPA, IRFU – AFTER, AGET, DREAM
- ASIC details in Fernando's 6.10.08 talk
- RDO details in Jeff's 6.10.09 talk





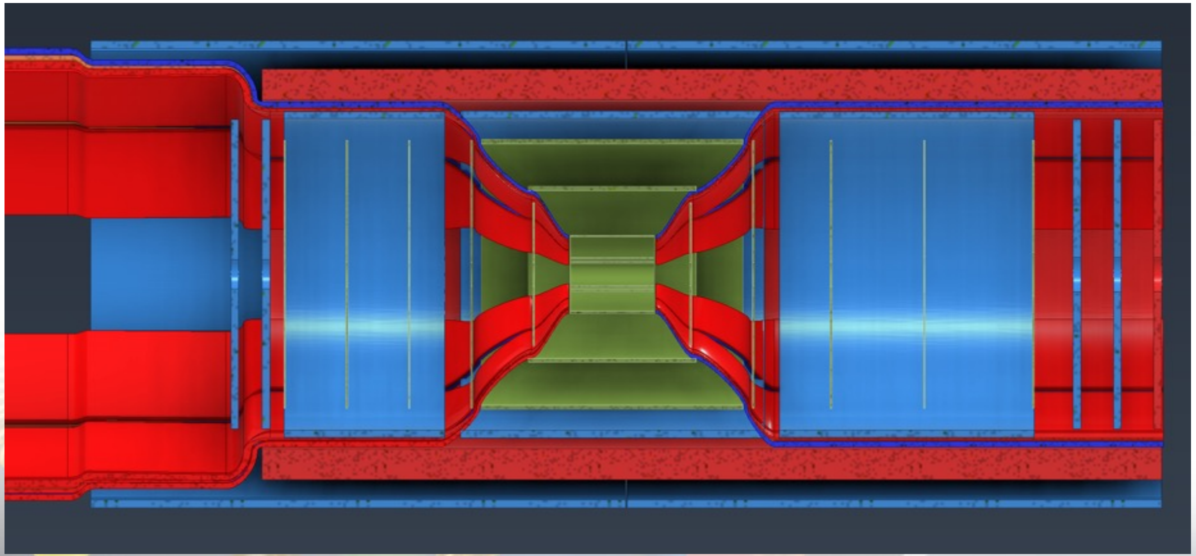
Services

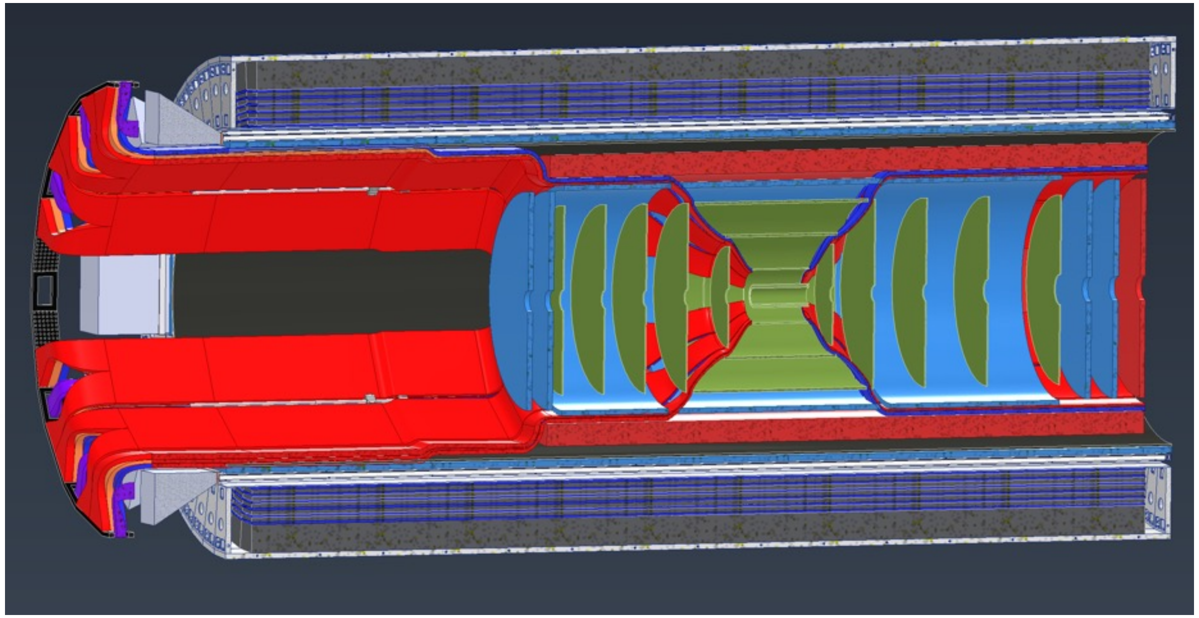
Subsytem	Type	Item	Material	Quantity	Diameter (cm)	Cross Area (cm^2)	+50% Packing for Bundles	Average Length (in)	Total weight (lbs)
Red Path IP to pfRICH Inner face									
Vertex Silicon	Power	18 awg LV Sagita	Aluminium	12	0.8	6.03	9.05	120.00	1.20
	Signal	Signal Bias		34	0.2	1.07	1.60	120.00	0.85
	Signal	Data *		204	0.6	57.68	86.52	120.00	102.00
	Cooling	*		12	0.3	0.85	1.27		
Sagita Silicon	Power	LV serial power		29	0.9	18.45	27.67		
	Signal	Signal Bias		771	0.3	54.50	81.75		
	Signal	Data *		771	0.2	24.22	36.33		
	Cooling	Cooling Pipes *		356	0.3	25.16	37.75		
Silicon Disks	Signal	Sensor Bias	Aluminium	1100	0.3	77.75	116.63	120.00	275.00
	Cooling	cooling	tygon	550	0.63	171.45	257.17	120.00	275.00
	Power	LV current	Aluminium	92	0.9	58.53	87.79	120.00	9.20
	Signal	Data		1100	0.3	77.75	116.63		
Inner MPGD	Signal	FEE Data	Firefly	60	1	47.12	70.69	120.00	1.50
	Power	Hv		40	0.32	3.22	4.83	120.00	4.00
	Power	Lv		20	1.163	21.25	31.87	120.00	2.00
	Cooling	Gas	Polyethylene	20	0.4	2.51	3.77	120.00	5.00
	Cooling	Cooling	Polyurethane	33	0.63	10.29	15.43	120.00	16.50
EE MPGD Disks	Power	FEE PWR	20 awg (3 pair)	11	1	8.64	12.96	120.00	0.00
	Signal	FEE data	Fibers	128	0.32	10.29	15.44	120.00	3.20
	Power	2kv Hv	Coax	4	0.24	0.18	0.27	120.00	0.40
	Signal	Flat Signal Cables		128	0.3	76.80	115.20	120.00	3.20
	Cooling	Gas	Tygon	8	0.4	1.01	1.51	120.00	2.00
	Cooling	Cooling	Tygon	16	0.63	4.99	7.48	120.00	8.00

- Inner most trackers cable path
- ~71% space used
- More details in Rahul's talk

Services

- RED = power
- BLUE = cooling/gas
- ORANGE = signal





Charge #3

Interfaces

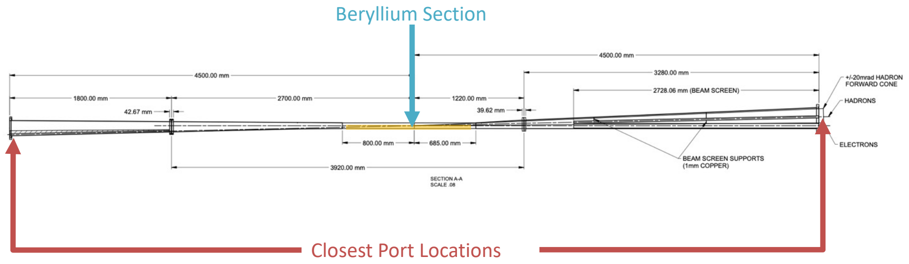
- https://eic.jlab.org/Interfaces/InterfaceMatrix.html

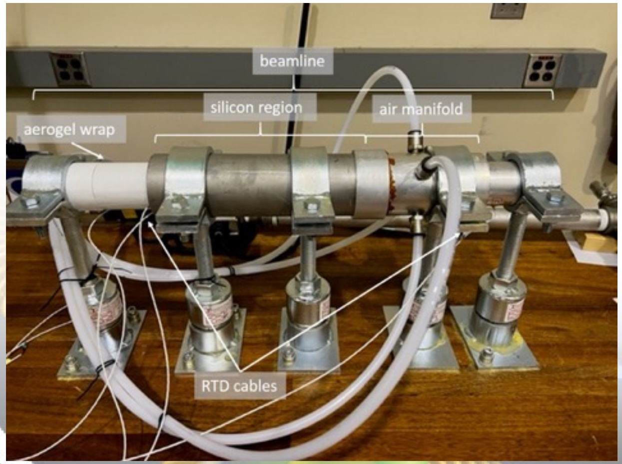
- Some highlights
  - Outer barrel limited by DIRC
  - Disks limited by pfRICH/AC-LGAD
  - Requires cooling/power from infrastructure
    - See Rahul's Talk
  - Inner Barrel first vertex layer 5mm from beampipe

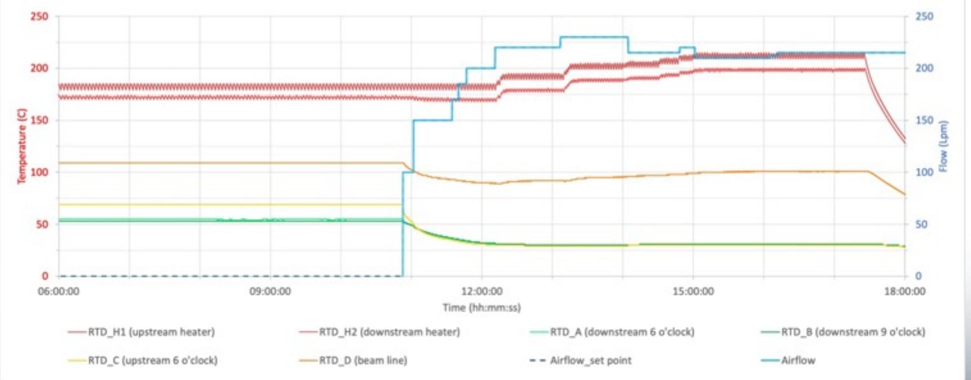
Charge #3

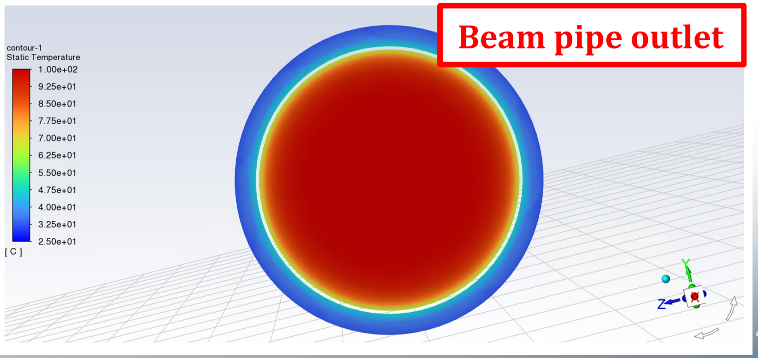
Interfaces – Beam Pipe

- Unique beampipe
  - Tapered beampipe, tracking detectors must be installed prior to beampipe installation in central detector
  - Beampipe exposed to ambient prior to installation
  - Need min 100℃ in beampipe to break H_2O bonds
    - Silicon detector epoxy limited to 30℃ due to CTE



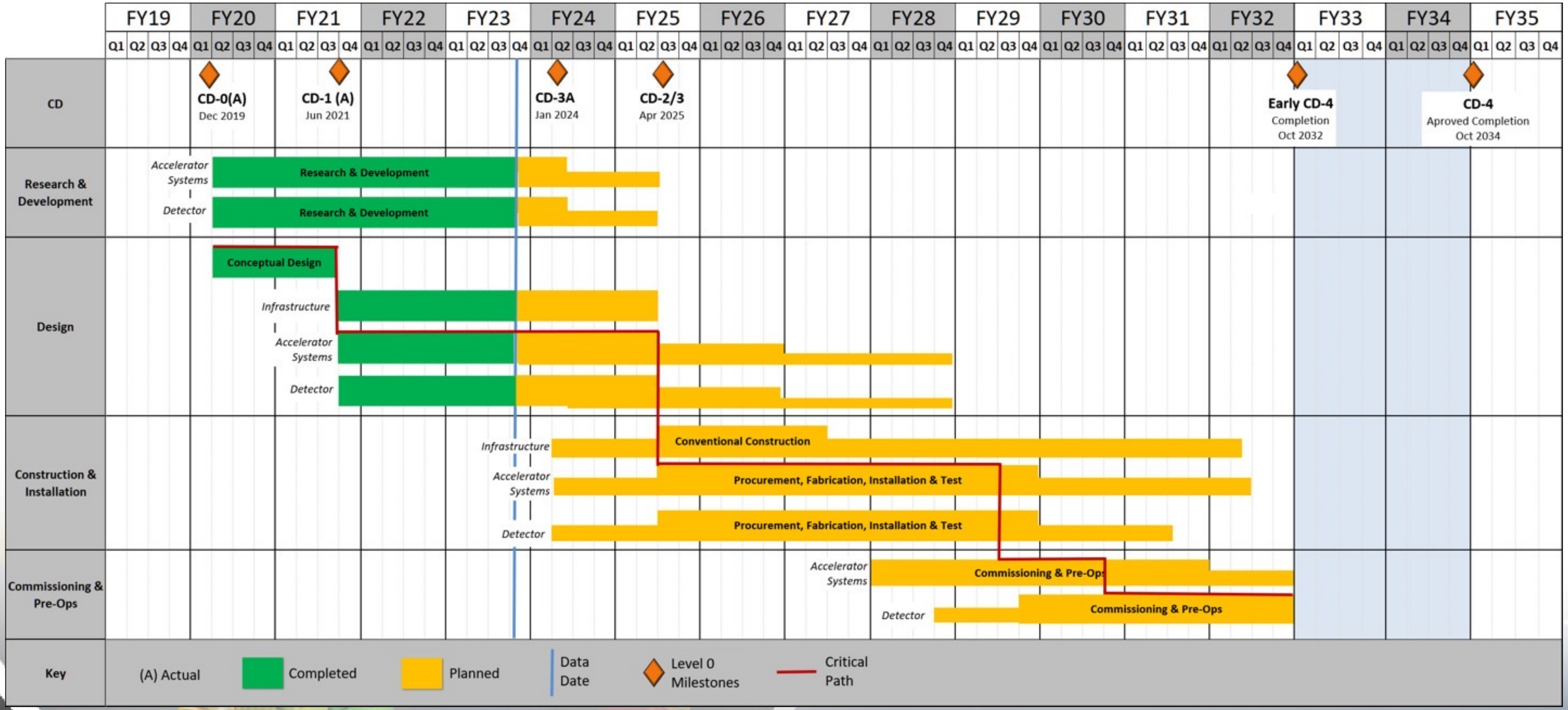






Charge #6

Schedule



- Inner Barrel Silicon (ITS3)
  - ER2 – Q1 24
- Outer Barrel/Disk Silicon (LAS)
  - 2025-2027
- Stave/Disk Construction Complete
  - Q4 28
- Ready for installation
  - Q2 29

Conclusion

1. Given the detector progress over the last two years and the status of the ePIC detector, are the projected timelines of the Electron-Ion Collider detector feasible? Do there remain significant open detector technology questions?
   - Yes, but relies on CERN/ALICE efforts. No, detector technologies are well understood.
2. Are the requirements for the detector and their flow down sufficiently comprehensive for this stage of the project to complete the design of the various detector technologies?
   - Yes, design requirements and geometry constraints are defined and tracked by EIC System Engineering.
3. Are the interfaces between the elements of the design adequately defined for this stage of the project and to proceed with the detector long-lead procurement items?
   - Yes, interfaces are defined and tracked by EIC System Engineering.
4. Is the design of these long-lead procurement items sufficiently advanced and mature to start procurement in 2024? Are the technical specifications complete?
   - N/A, no LLP for tracking detectors.
5. Is the projected design maturity of the further detector components likely to be accomplished by the end of 2024 for CD-2 and CD-3?
   - No, but this is expected due to silicon sensor schedule
6. Is the overall schedule for completion of the design, production, and installation of detector components realistic?
   - Yes, but with a technically driven schedule

BACKUP

Collaboration

- Current progress is the result of many people’s effort. Included (in no particular order) are some that generated some of the included figures and plots
  - Laura Gonella, University of Birmingham
  - Ernst Sichtermann, LBNL
  - Roland Wimmer, BNL
  - Francesco Bossu, CEA Saclay
  - Kondo Gnanvo, JLab
  - Peter Jones, University of Birmingham
  - Stephen Maple, University of Birmingham
  - Shyam Kumar, INFN Bari

Collaboration

UNIVERSITY OF BIRMINGHAM

INFN

BERKELEY LAB

UKRI Science and Technology Facilities Council

Brookhaven National Laboratory

Berkeley UNIVERSITY OF CALIFORNIA

Jefferson Lab

Los Alamos NATIONAL LABORATORY

OAK RIDGE National Laboratory

UNIVERSITY OF LIVERPOOL

UNIVERSITY OF OXFORD

MIT

PURDUE UNIVERSITY

CTU CZECH TECHNICAL UNIVERSITY IN PRAGUE

Brunel University London

Lancaster University

Services – Silicon

- Shunt-LDO regulator design