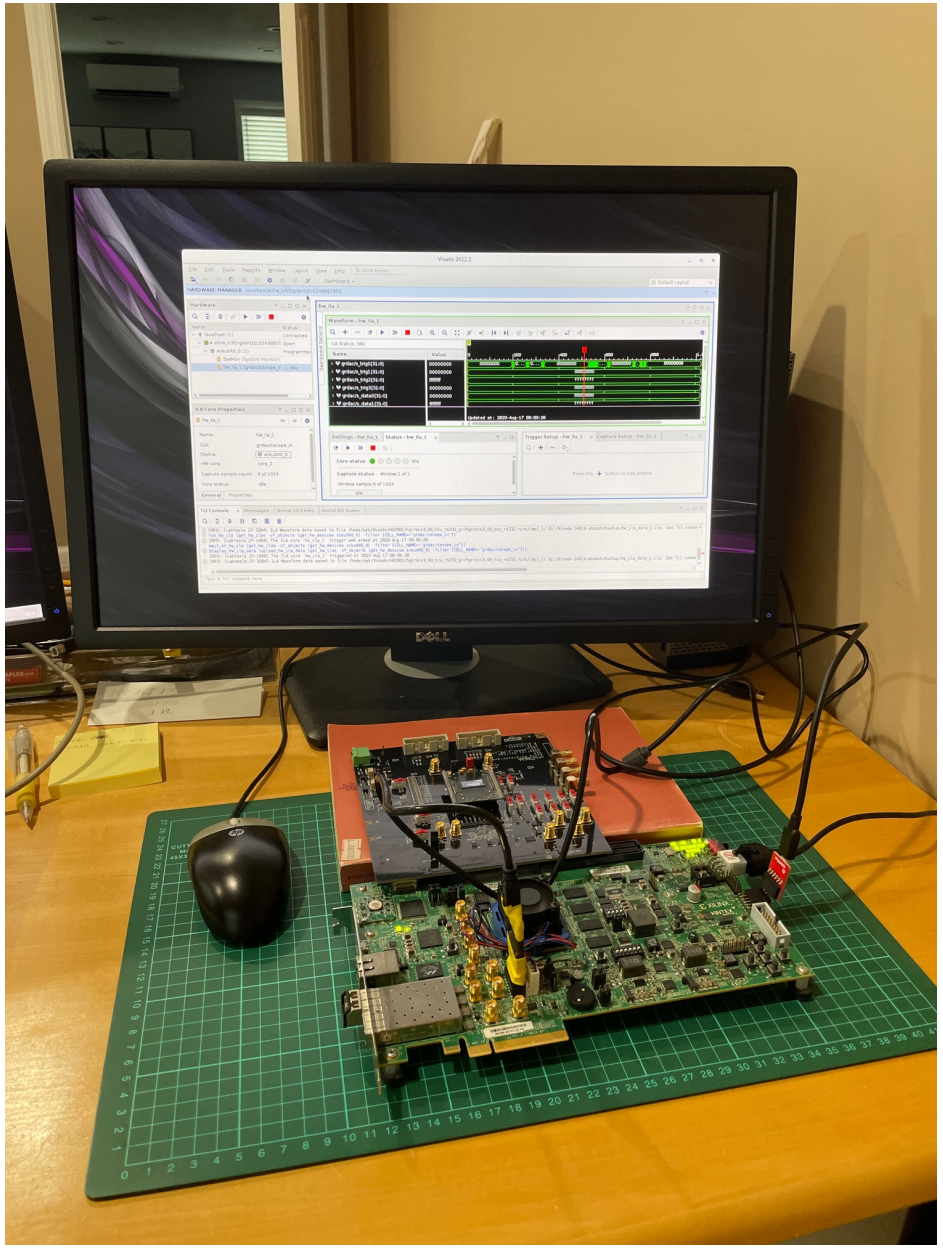
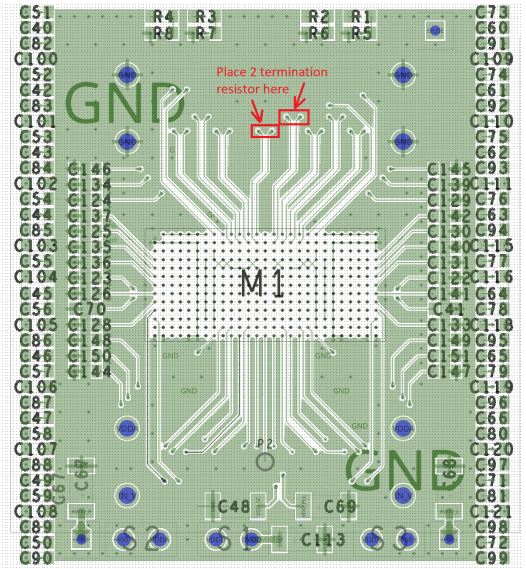
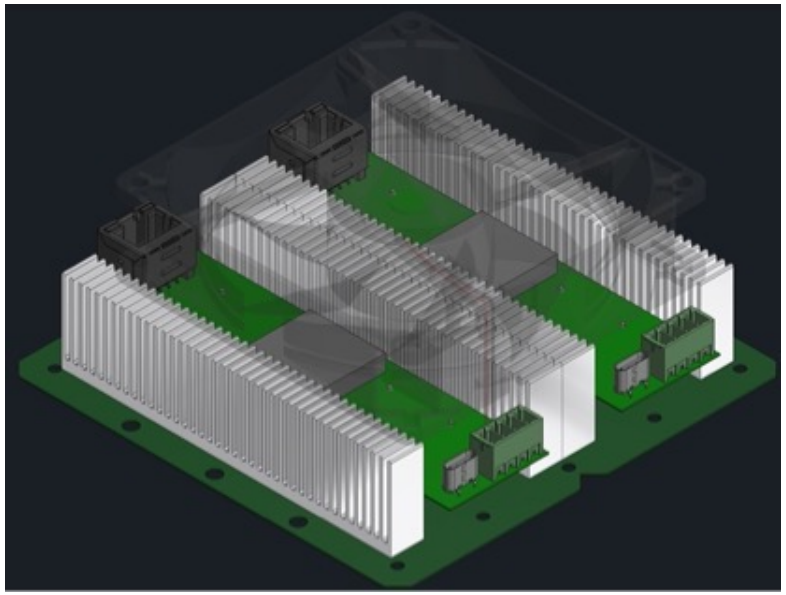
HRPPD ASIC FEE update

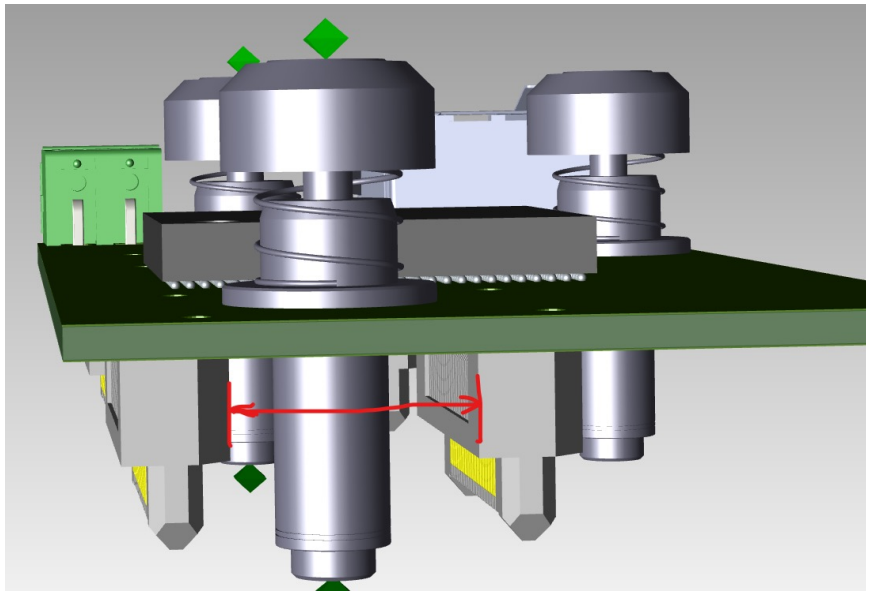


- A small HGCROC3 installation at BNL
  - Essentially a Linux-based copy of Oak Ridge setup
    - KCU105 FPGA kit provided by John Kuczewski (BNL)
    - Carrier board by Norbert Novitzky (ORNL)
    - HGCROC3 mezzanine board by Damien Thienpont (IN2P3)
    - FPGA firmware by Miklos Zeller (Debrecen)
  - Should be sufficient for writing an RCDAQ driver
    - First via USB, then gigabit ethernet
  - Only partially functional so far
    - Issues with on-board termination
    - Will be sent to CERN this week …
    - … and hopefully fixed by Miklos

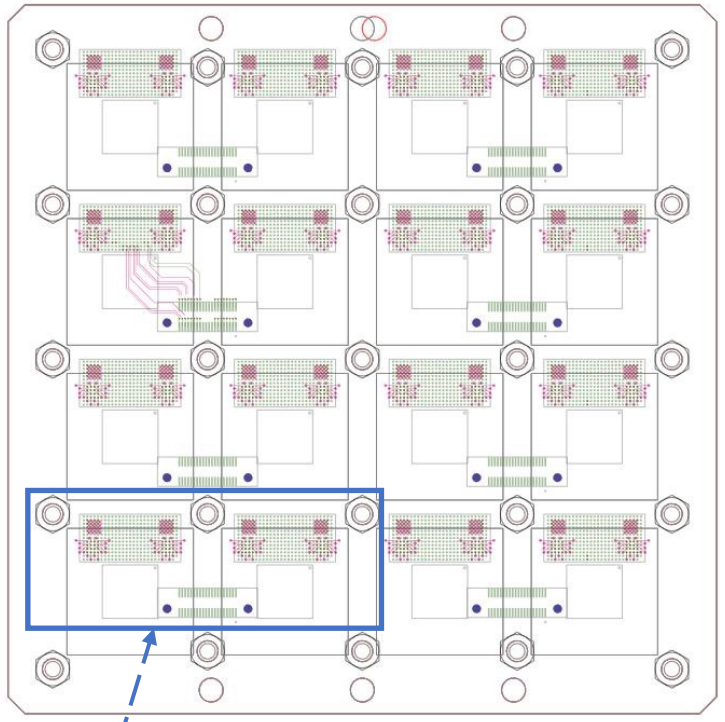


HRPPD ASIC FEE update

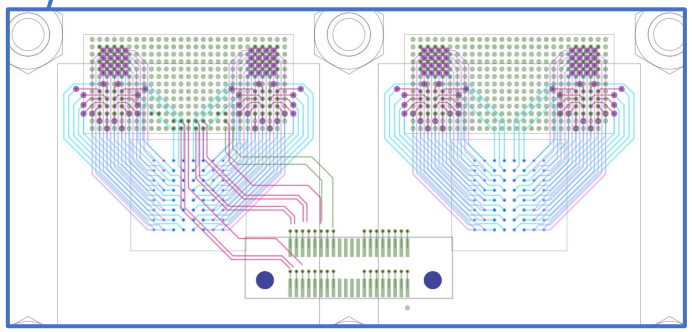


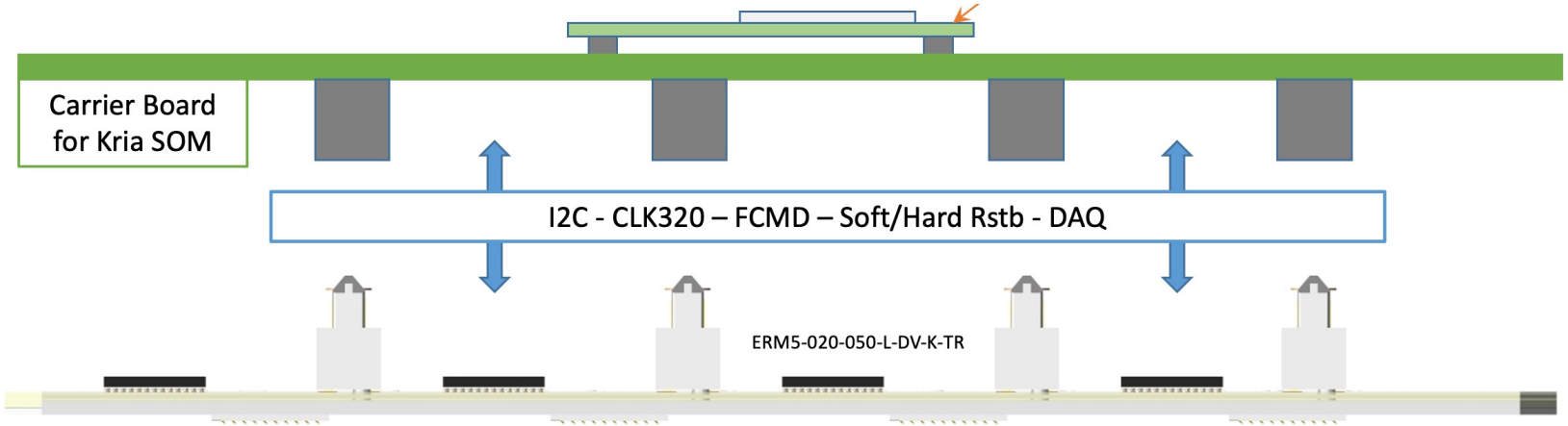


3D integration and cooling options by G. Nagy (Debrecen) and D. Cacace (BNL)



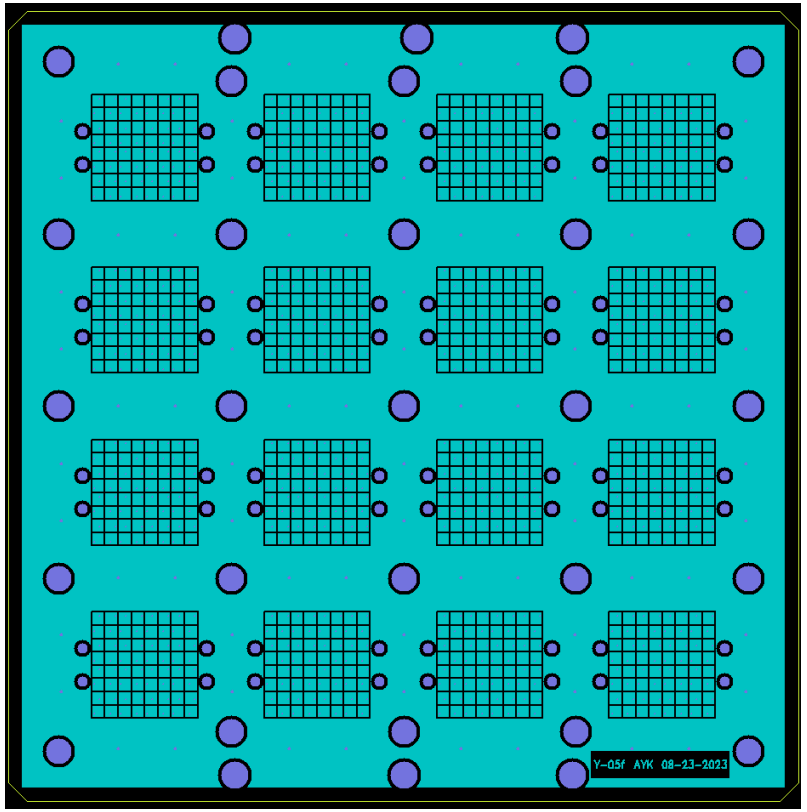
ASIC backplane design
by P. Dinaucourt (IN2P3)



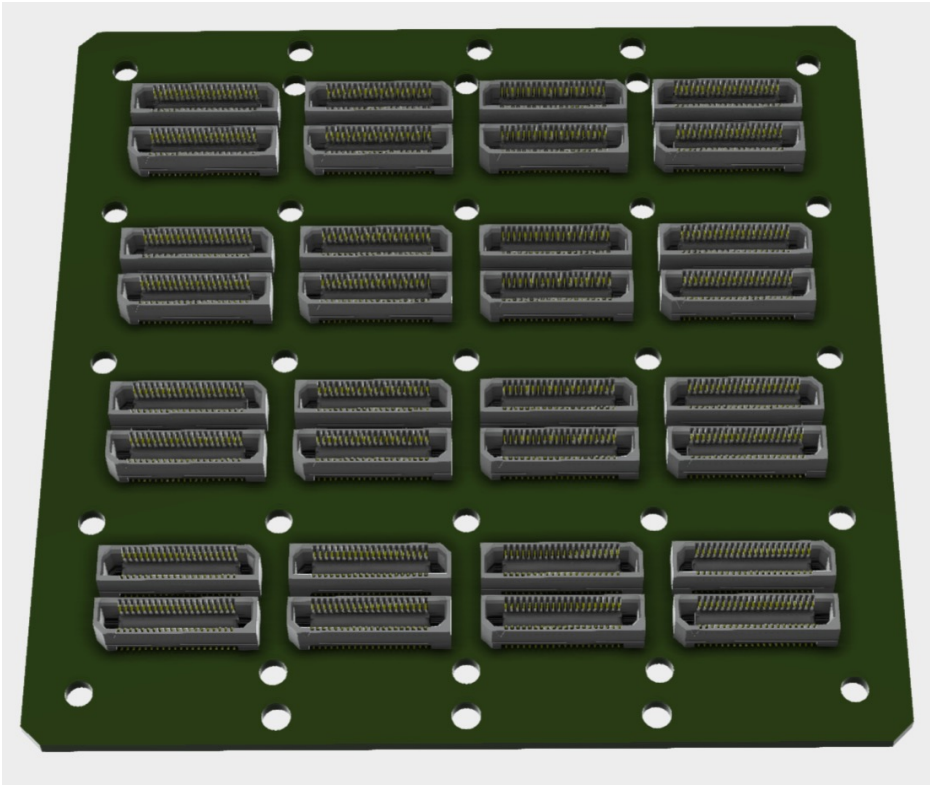


FRONT END BOARD 16 x BGA HGCROC HD 350 0.6mm

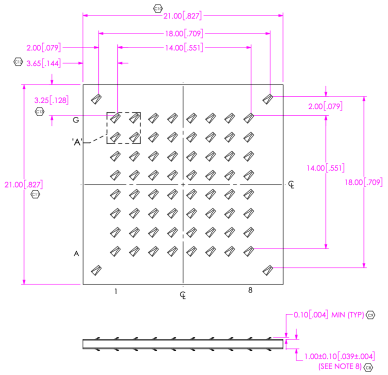
A dummy HRPPD readout board Y05f



bottom side (matches HRPPD rear side)



top side (32x Samtec ERF8 connectors)



- Got a quote for ten bare boards -> to be ordered today (last call!)
- Connectivity proposal for any of the sixteen 8x8 pad fields:
  - A set of [2x Samtec ERM8 -> MMCX] adapters, most likely 32ch (4x8) at a time
  - A set of ERM8-based grounding caps for all other 8x8 fields