# ALCOR ASIC

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INFN Torino

TIC meeting - FEE, Cooling
11.09.2023

ALCOR (**A** **L**ow Power **C**hip for **O**ptical Sensor **R**eadout)

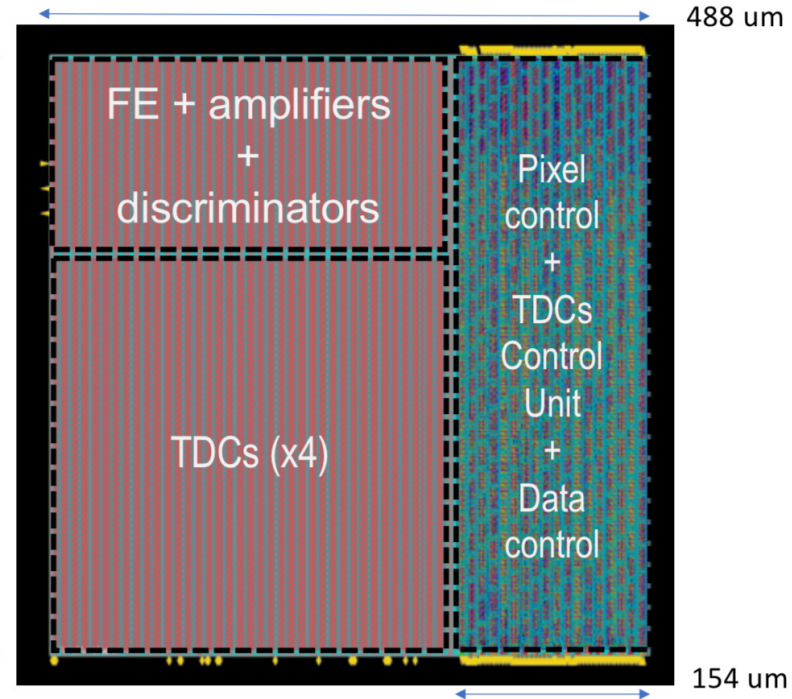ASIC developed for the readout of the **EPIC dRICH** SiPM sensors

- **32-pixel** matrix (8x4) mixed-signal ASIC

- Each pixel performs signal **amplification**, **conditioning** and **digitization**

- **Single-photon time tagging** and **Time-over-Threshold** measurements

- **Fully digital output**: 32-bit (64-bit in ToT mode) event words, 4 LVDS 320 MHz DDR Tx links
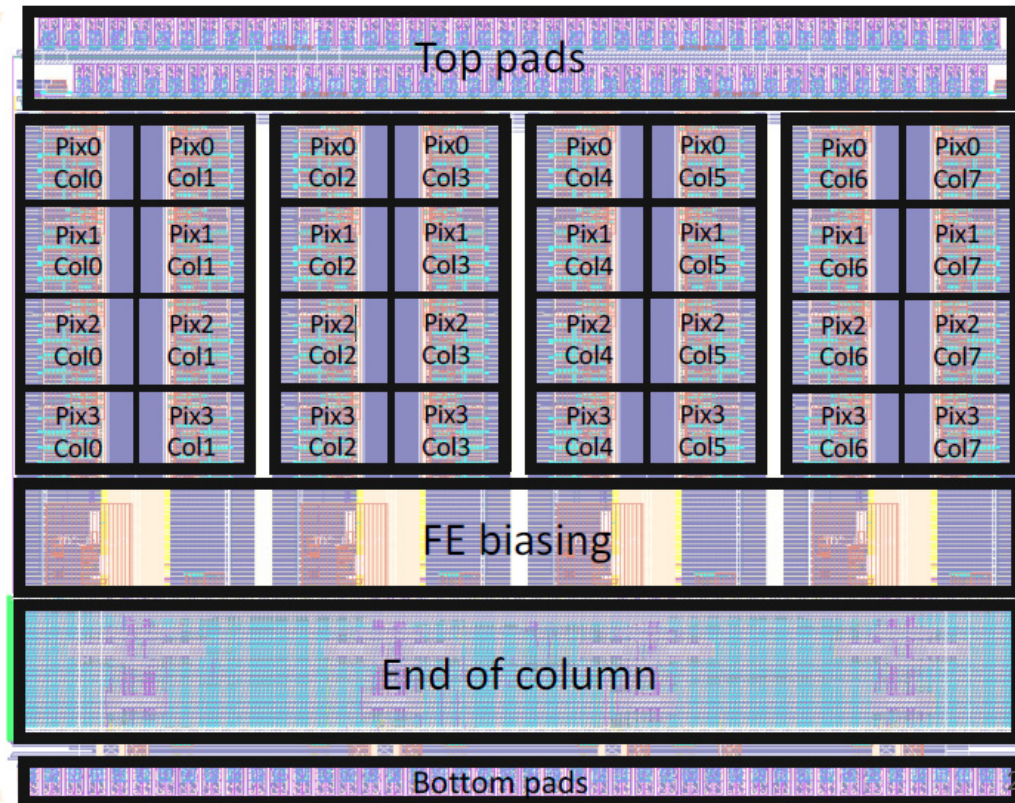
Pixel architecture

488 um

488 um
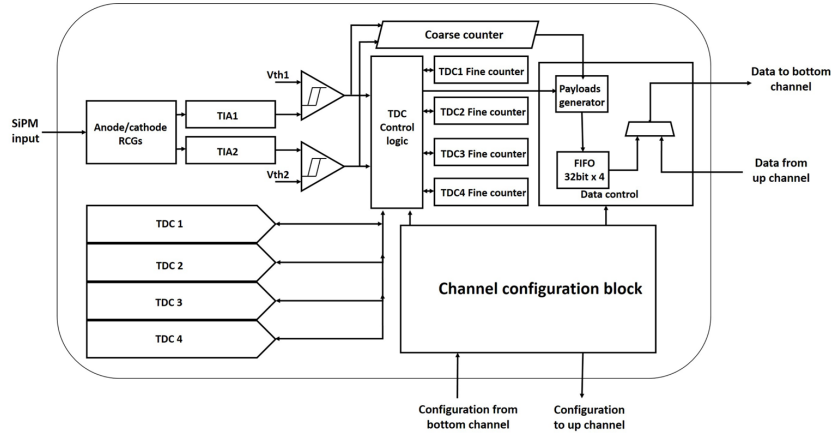
154 um

- TIA amplifier with **RCG input stage**

- 2 independent post-amp branches with **4 gain settings**

- Dual **leading edge discriminators** with independent (and per pixel) threshold settings (6-bit DAC)

- **4 TDCs** based on **analogue interpolation** with 25-50 ps time-bin

- Pixel control logic handles TDC operation, pixel configuration and data transmission
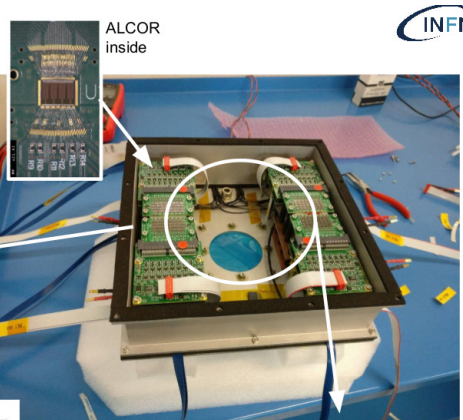
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ALCOR v1

- Originally designed for the readout of SiPMs at 77K, in the framework of Darkside (MPW, Dec 2019)
- Extensively used within the EIC dRICH Collaboration in the last 2 years
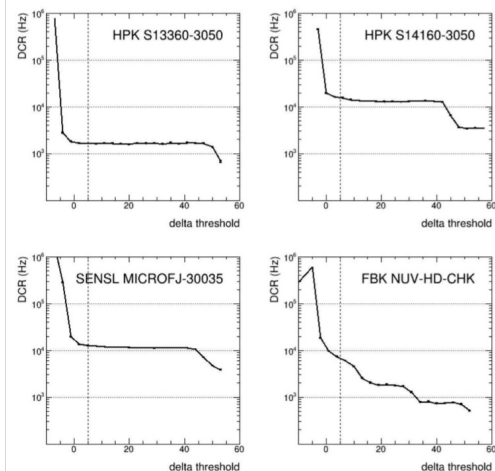

2022 test beam at CERN-PS

dRICH prototipe on PS beamline with SiPM-ALCOR box

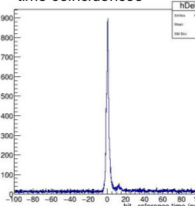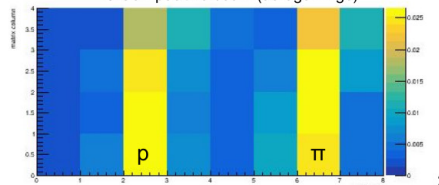ALCOR inside

beamline shared with LAPPD test

successful operation of SiPM **irradiated** (with protons up to 10¹⁰) and **annealed** (in oven at 150 C)

time coincidences

8 GeV positive beam (aerogel rings)

Slides from R. Preghenella (INFN BO)

ALCOR v2

ALCOR v2

- MPW, submitted in Dec 2022

- 60 chips, received in June, promising results from first tests

  - ✓ TDC logic critical error occurring at high rates solved also for DCR rate at room temperature
  - ✓ New FE gain settings more suited for single photon applications
  - ✓ On-chip analogue test-pulse also for EIC SiPM polarity
  - ✓ Improved functionalities from EoC special words (header, frame, CRC, status)
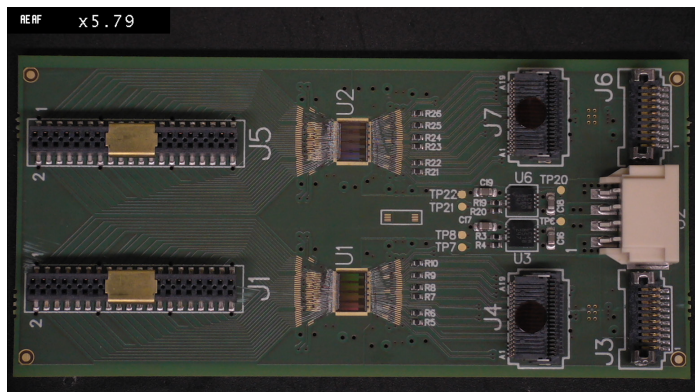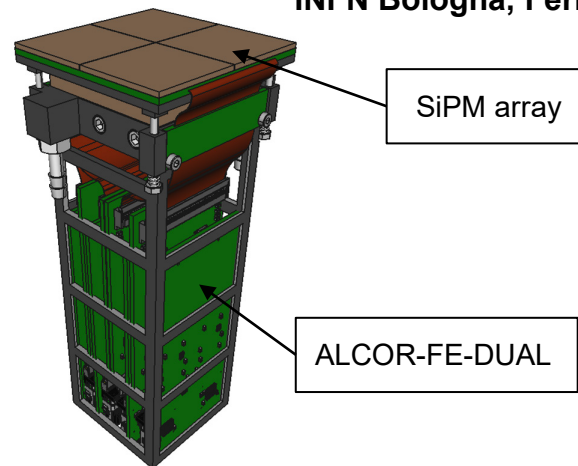
ALCOR v2.1

- INFN internal engineering run

- Submitted in Mar 2023, wafers delivered, dicing ongoing

- High number of chips will be available

- TDC logic bug fix (TFine-clock ambiguity, TOT orphans due to fake trigger at very low rates)

2023 readout system

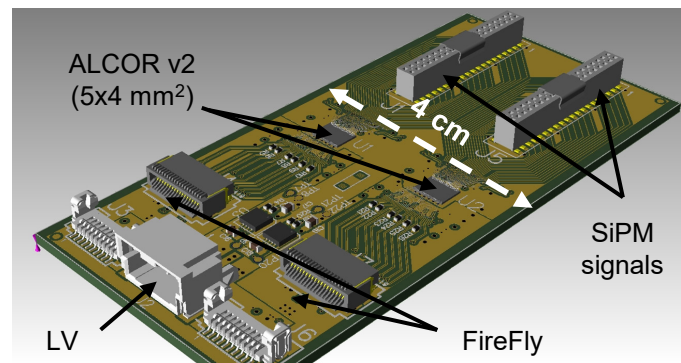## ALCOR-FE-DUAL

- Two **32-channel ALCOR v2** ASICs **wire-bonded** on the PCB

- 4 ALCOR-FE-DUAL boards for each **PDU** (256 channels)

- This system will be used for the 2023-2024 beam tests

Prototype photodetector unit (PDU)
INFN Bologna, Ferrara

SiPM array

ALCOR-FE-DUAL

designed by INFN Torino (M. Mignone)

ALCOR v2
(5×4 mm^2)

4 cm

SiPM signals

LV

FireFly

Next version: ALCOR v3

- **64-channel** version with **BGA package** (~256 IO pins)

- Revise **ALCOR FE** design to improve time resolution and rate capability of the SiPM+ALCOR system

  - Studies on SiPM capacitance and optimal coupling with ALCOR (AC coupling inside ALCOR)
  - Increase amplifier bandwidth
  - Improve response for afterpulses and re-triggering (hysteresis discriminator)

- **Digital logic** bug fix and new features

  - **Digital shutter** for data reduction (EIC bunch crossing: 10 ns → 1-2 ns time window)
  - Increase EoC FIFO size to cope with higher data rate
  - Remove orphan data due to re-triggering of events very close in time

- Operation of ALCOR with multiple of EIC clock frequency (98.52 MHz): 295.56 MHz or **394.08 MHz**

  - First tests on ALCORv1 at 390 MHz look promising but more detailed tests and simulations are required, digital implementation must be re-done with new constraints

ALCOR packaging

Standard packaging (QFP, QFN) is cheap but provides low number of pins and large area, which is not suitable for the implementation of the 64-channel ALCOR

Ball grid array (BGA) package

Inside the package, the chip is **flipped** so that the active side of the device is **bump-bonded** to the package substrate

- ➢ The whole bottom surface of the device can be used, not just the perimeter
- ➢ More interconnection pins wrt QFP or QFN
- ➢ Shorter interconnections reduce inductance, allow high-speed signals and carry heat better
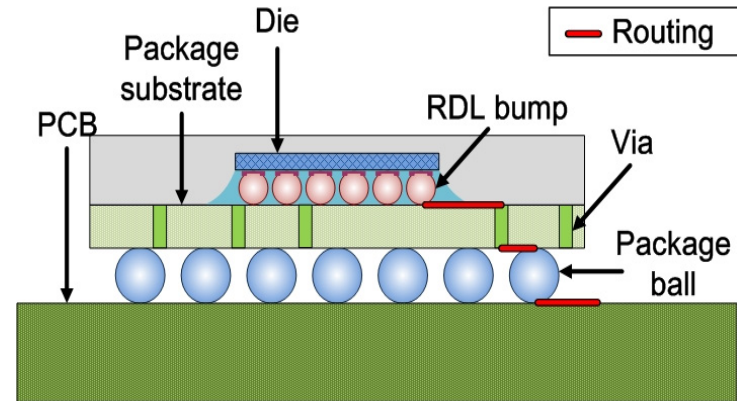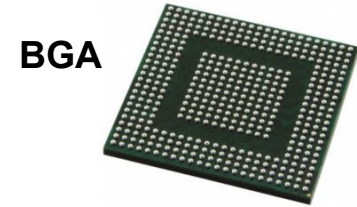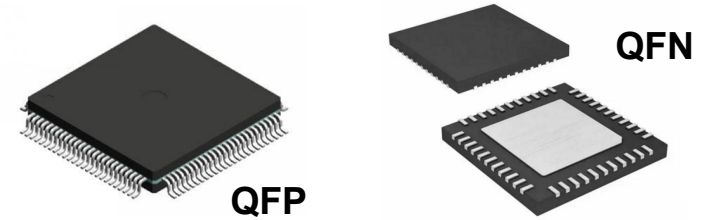
ALCOR v3 floorplan
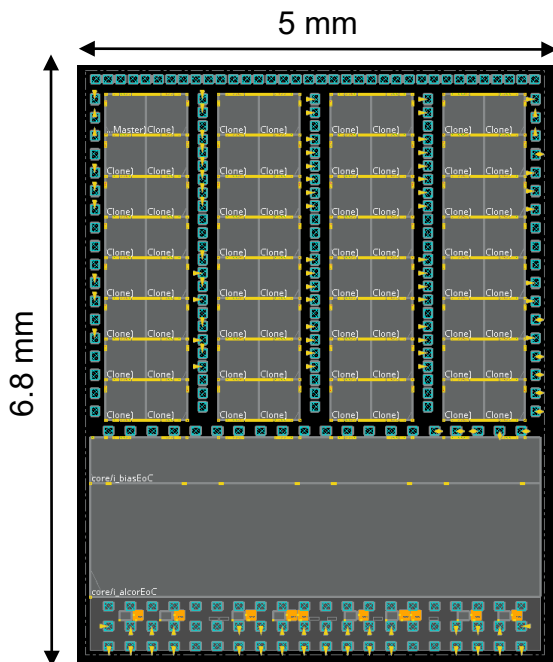
8x8 pixel matrix ASIC (64 channels)
- SiPM inputs bump pads between the pixel sectors
- Digital EoC in the bottom part

256 balls BGA package
- Power and ground on inner/mid contacts
- I/O on outer contacts

Next steps

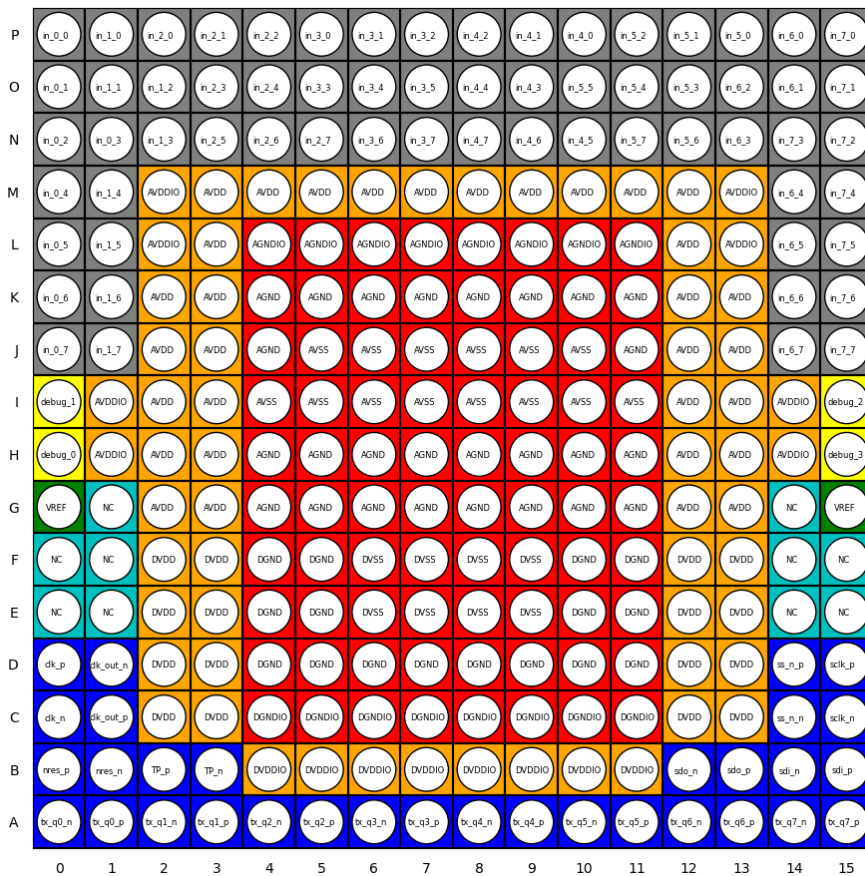❑ Preparation of **ALCOR FE-DUAL** boards for **beam-test** in October at CERN:

- 22 boards (44 ALCOR v2) already tested and validated

- Assembly of ALCOR FE-DUAL inside the PDUs will start on Sep 19th

- Results from the beam test will provide the validation of ALCOR v2 with dRICH SiPMs

❑ Design of **ALCOR v3** and its package ongoing

- **64-channel** MPW version to be submitted before Summer 2024

- Market survey with package manufacturers to define **BGA packaging** specs and costs

- Start design of the EPIC dRICH Front-End Board (FEB), hosting the ALCOR v3 chips inside the BGA package

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Spare slides

Digital shutter

ALCOR test pulse can also act as **"inhibit"** of the pixel digital logic and this can help to reduce data throughput

- Successfully used in beam tests to reduce occurrence of ALCORv1 TDC logic critical errors but current version of ALCOR cannot work with such short shutter time interval (inhibit signal is synchronous with clock, issues if leading/trailing edges of discriminator signal are across the time window)

- In EIC: 10 ns bunch crossing, 250 ps bunch length, select 1-2 ns → **5-10x data reduction** before ALCOR TDCs

Logic for asynchronous digital shutter implemented in ALCORv3

- Studies ongoing to define programmable delays needed to ensure same time window for all the channels
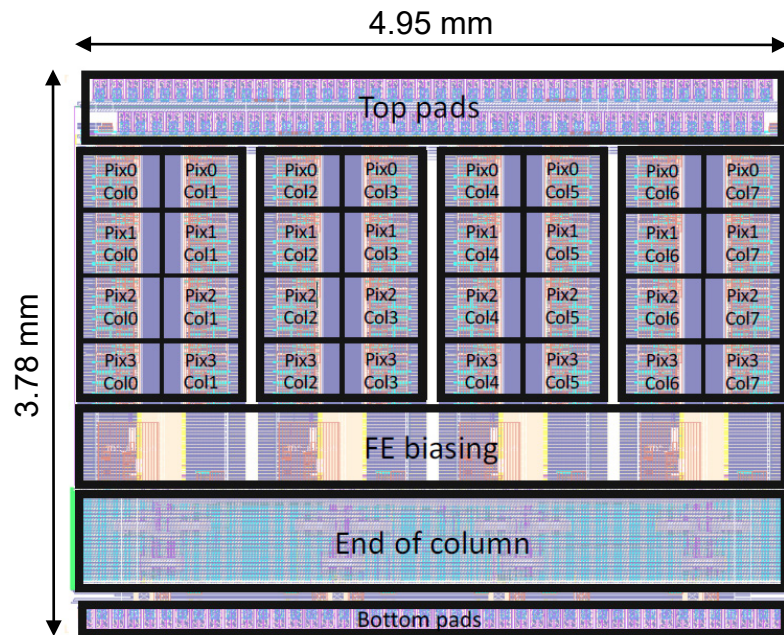
ALCOR I/Os

ANALOGUE (top, 44+38=82)

- 16 AVDD + 4 AVDD_IO
- 16 AGND + 4 AGND_IO
- 4 AVSS
- 32 inputs
- 4 debug outputs
- 2 bias Vref

DIGITAL (bottom, 20+24=44)

- 6 DVDD + 2 DVDD_IO
- 6 DGND + 2 DGND_IO
- 4 DVSS
- 2 clk, 2 reset, 2 test-pulse
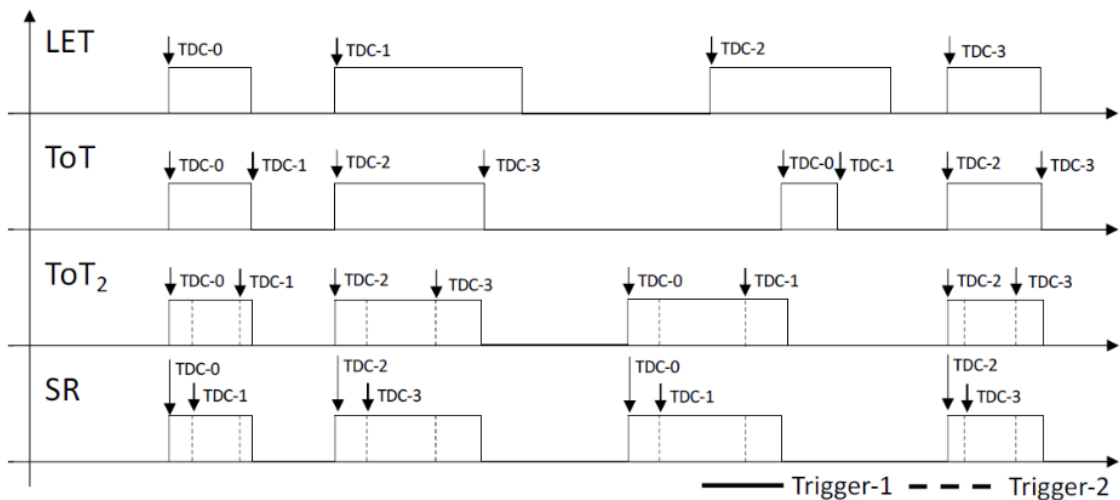- 8 Tx outputs
- 2 clk_out
- 8 SPI

ALCOR current version has 32 channels and 126 I/Os

ALCOR v3: targeting a **64-channel** version with **~256 I/Os**
(Area: ~6.8 x 5 mm^2, MPW blocks are 5 x 5 mm^2)

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ALCOR pixel operating modes

4 operating modes:

- **LET**: leading edge measurement
- **ToT**: Time-over-Threshold measurement using the first discriminator for both edges
- **ToT2**: Time-over-Threshold measurement using both discriminators
- **SR**: slew-rate measurement

Each mode can be set to:

- **FE**: normal operation mode
- **FE_TP**: send test-pulse to analogue front-end
- **TDC_TP**: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)

Each pixel can also be disabled

ALCOR V1/V2 maximum data rate

- Theoretical limitation: 4 links up to 640 Mb/s
  - 640 / 40 bits / 8 pixels => 2 MHz/pixel (1 MHz TOT mode)

- Simulation parameters
  - System clock: 3.1 ns
  - Input signal: Test Pulse to TDC
  - 256 hits per channel with constant period
  - 32 pixels readout
  - No status words

- Simulation measurements (full chip VHDL simulations)
  - No data loss up to 600 kHz / pixel
  - Data loss at higher rates due to End of Column FIFOs size (input FIFOs full flag)
  - The readout between Pixel Matrix and End of Column is capable up to 6 MHz per pixel
  - Single Pixel data loss (internal) at 7 MHz and more

- The data rate is limited by EoC FIFOs size (600 kHz/ch), then secondly by the number and speed of serializers (2 MHz/ch)

ALCOR v2

➢ MPW, submitted in Dec 2022

➢ **60 chips received mid June 2023**

Bug fixes and new features:

1. Solve TDC logic critical error occurring at high rates

2. Generation of special words from EoC (header, frame, CRC) also when status words are disabled

3. New FE gain settings more suited for single photon applications

4. On-chip test-pulse also for EIC SiPMs polarity

1. TDC logic critical error

ALCORv1 TDC logic bug

- occurs at high rates (DCR > 500 kHz)
- generates corrupted data which saturates the ASIC output bandwidth
- requires a full reset to recover

bad points due to TDC logic error

ALCOR V1 - gain 0
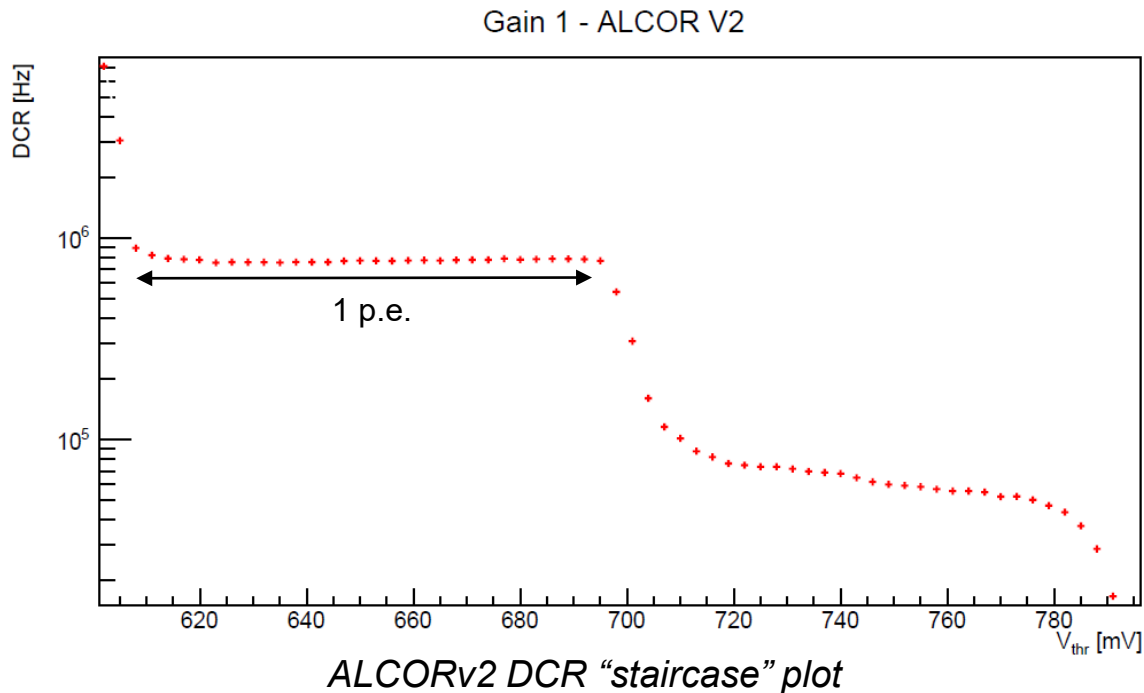

ALCORv1 DCR "staircase" plot
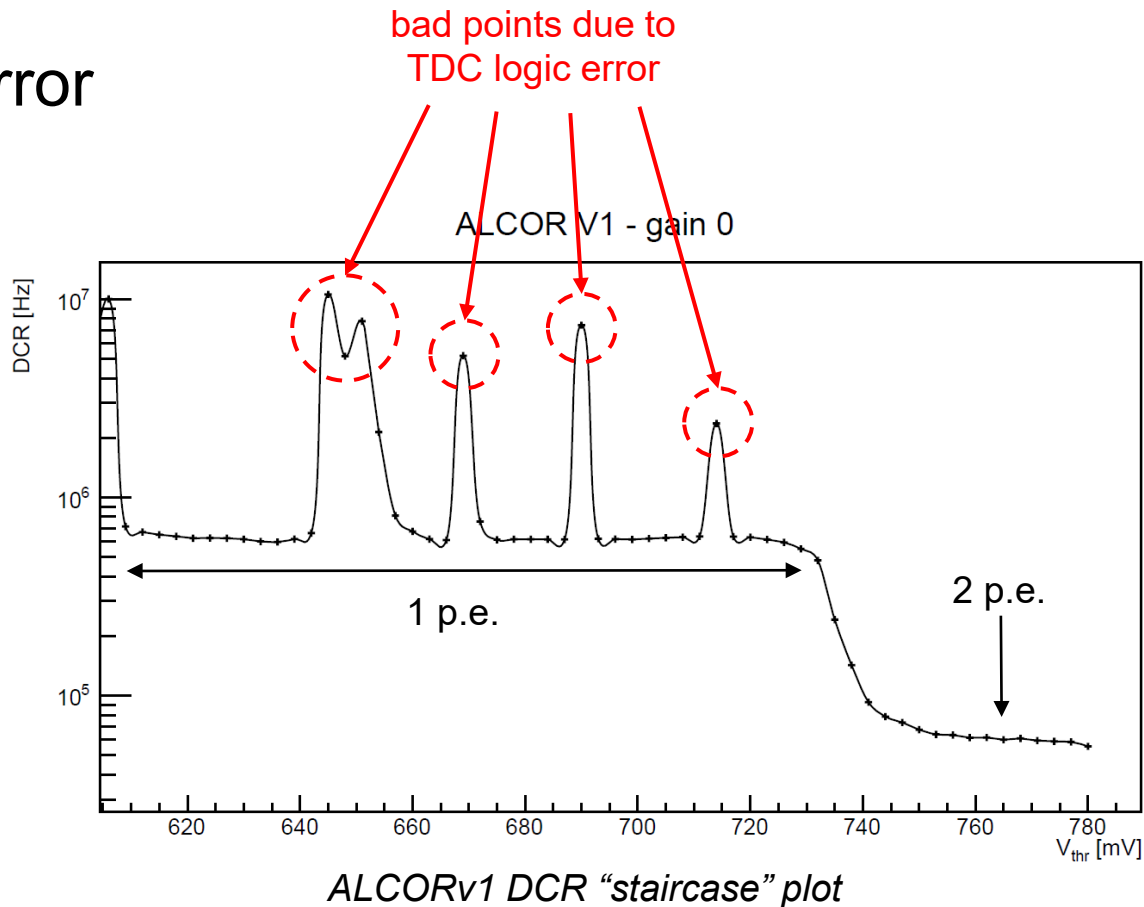
1. TDC logic critical error

ALCORv1 TDC logic bug

- occurs at high rates (DCR > 500 kHz)
- generates corrupted data which saturates the ASIC output bandwidth
- requires a full reset to recover

➢ **Solved in ALCORv2**

Gain 1 - ALCOR V2

1 p.e.

ALCORv2 DCR "staircase" plot

2. EoC special words

Header, *frame*, *CRC* and *status* words are added to *event* words to provide information for data clustering, synchronization and verification

ALCORv1 can operate in *raw-data mode* (only event words) or in *full mode* (all special words are included)

➤ **ALCORv2** can also operate in an intermediate mode where only ***status* words** are **disabled**
➤ This helps to reduce data throughput (status words are >50% of special words)

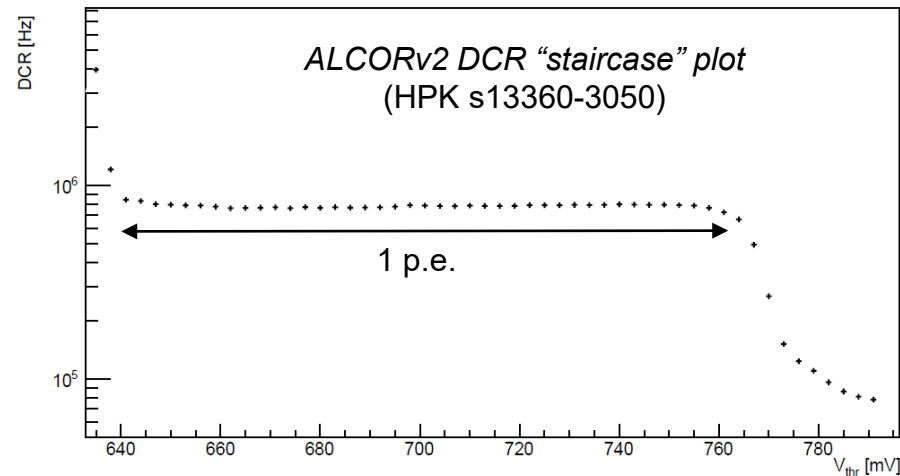| FIFO position	Data
1 (FPGA first received)	K28.0 (Frame header)
2	Frame number (16 bit)
3	Event words Column 0
..	Event words Column 1
n	K28.2 (Coarse Counter Rollover header)
n+1	K28.3 (Status header)
n+2	Status words Column 0 (x4)
n+6	Status words Column 1 (x4)
n+10	End of Column status word
n+11	K28.4 (Checksum header)
n+12	CRC value
n+13	K28.0 (New Frame header)

Table 5: Data stream with data events.
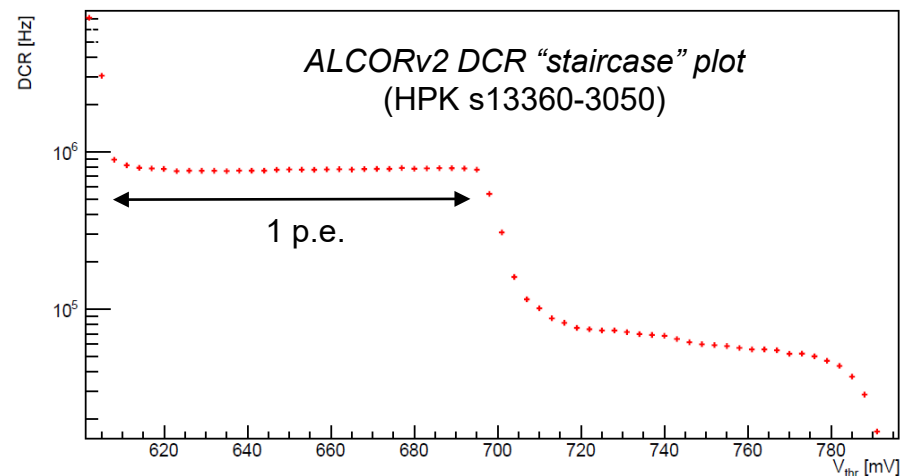
3. FE gain settings

ALCORv2 front-end implements two different gain settings best suited for single-photon applications

➢ to be tested with different SiPM models currently used within the EIC dRICH framework


Gain 0 - ALCOR V2

ALCORv2 DCR "staircase" plot
(HPK s13360-3050)

1 p.e.

Gain 1 - ALCOR V2

ALCORv2 DCR "staircase" plot
(HPK s13360-3050)

1 p.e.

4. On-chip test-pulse

ALCOR can read both input signal polarities, but ALCORv1 internal test-pulse can only inject signals for negative polarity

➤ On-chip test-pulse generation included in **ALCORv2** also for EIC SiPMs signal polarity (positive)

VTH scan (200 test-pulse)
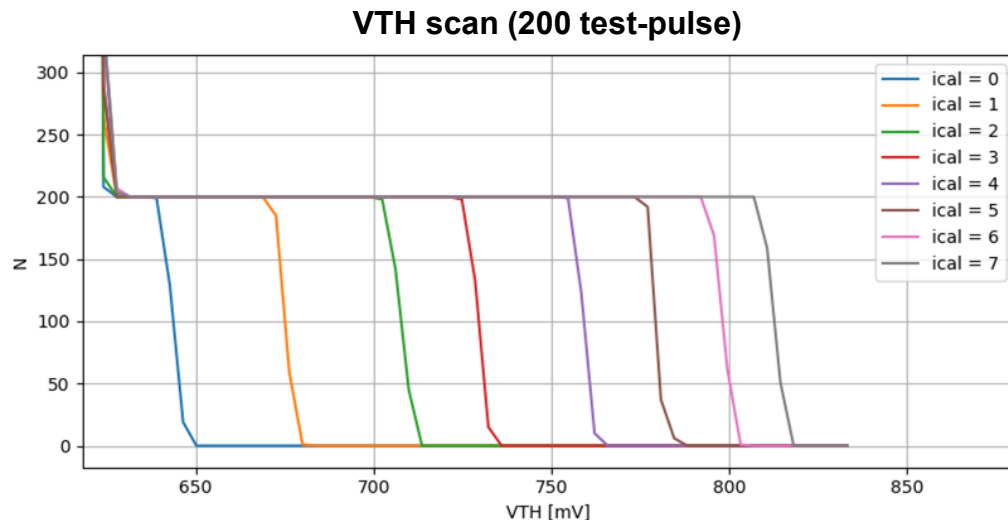
On-chip 3-bit DAC calibration circuit to define injected current magnitude