EICROC0 testing at BNL

Gabriele D'Amen (BNL),

Hijas Farook (UNM)

Yuji Goto (RIKEN)

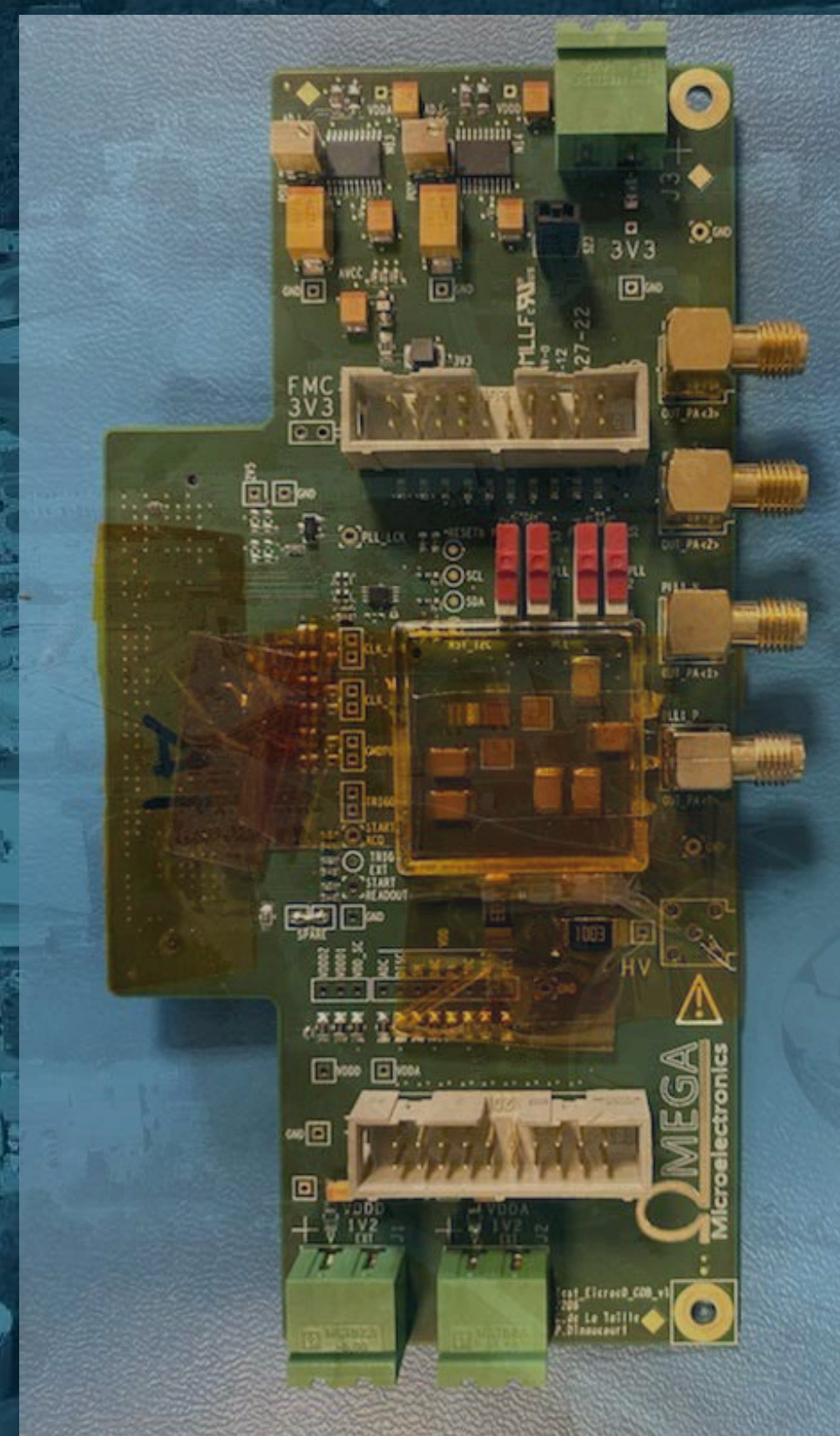Souvik Paul (SBU)

Prashanth Sanmuganathan (BNL)

Kenta Shigaki (Hiroshima)

Prithwish Tribedy (BNL)

Alessandro Tricoli (BNL),

Satoshi Yano (Hiroshima)
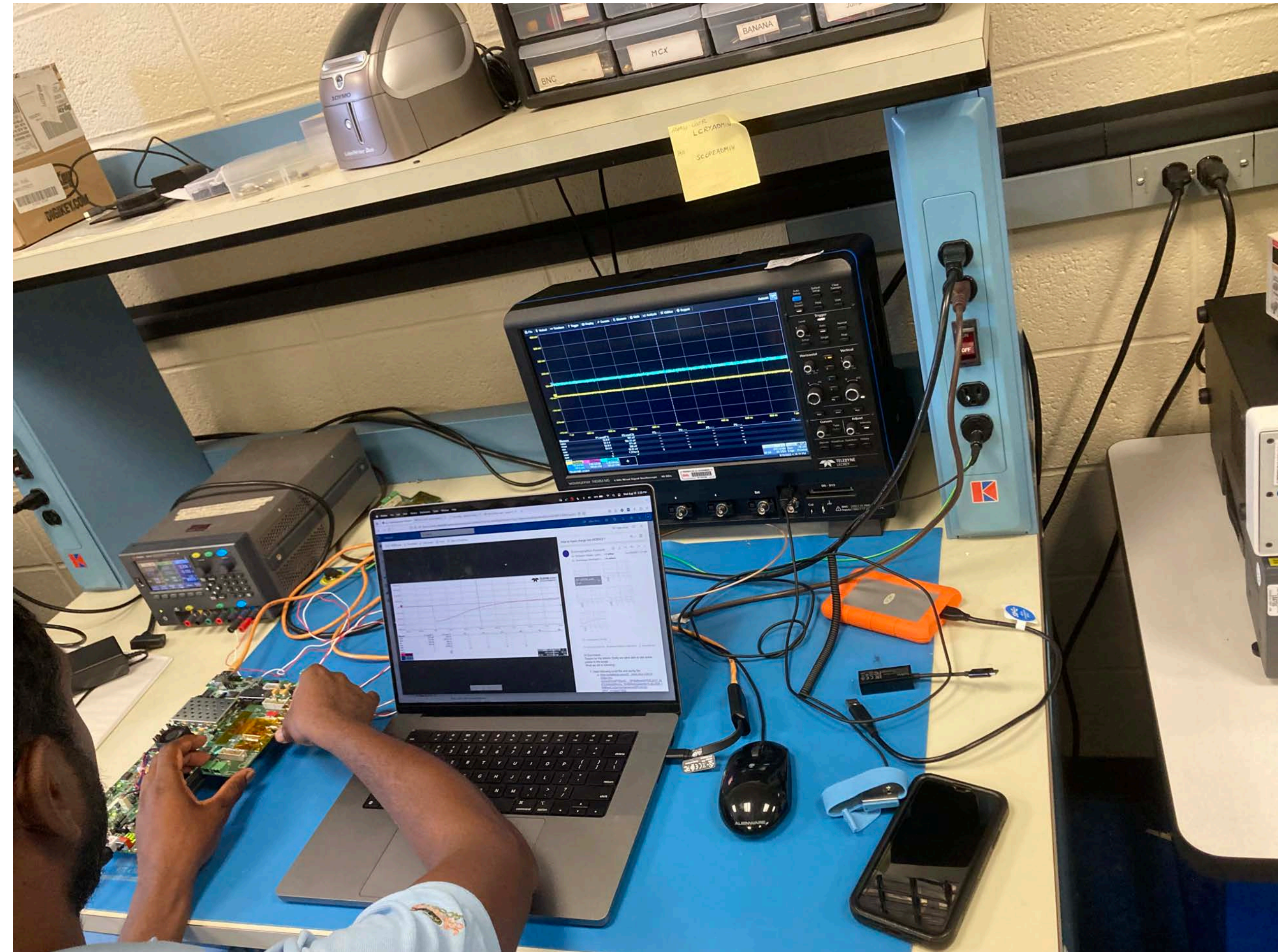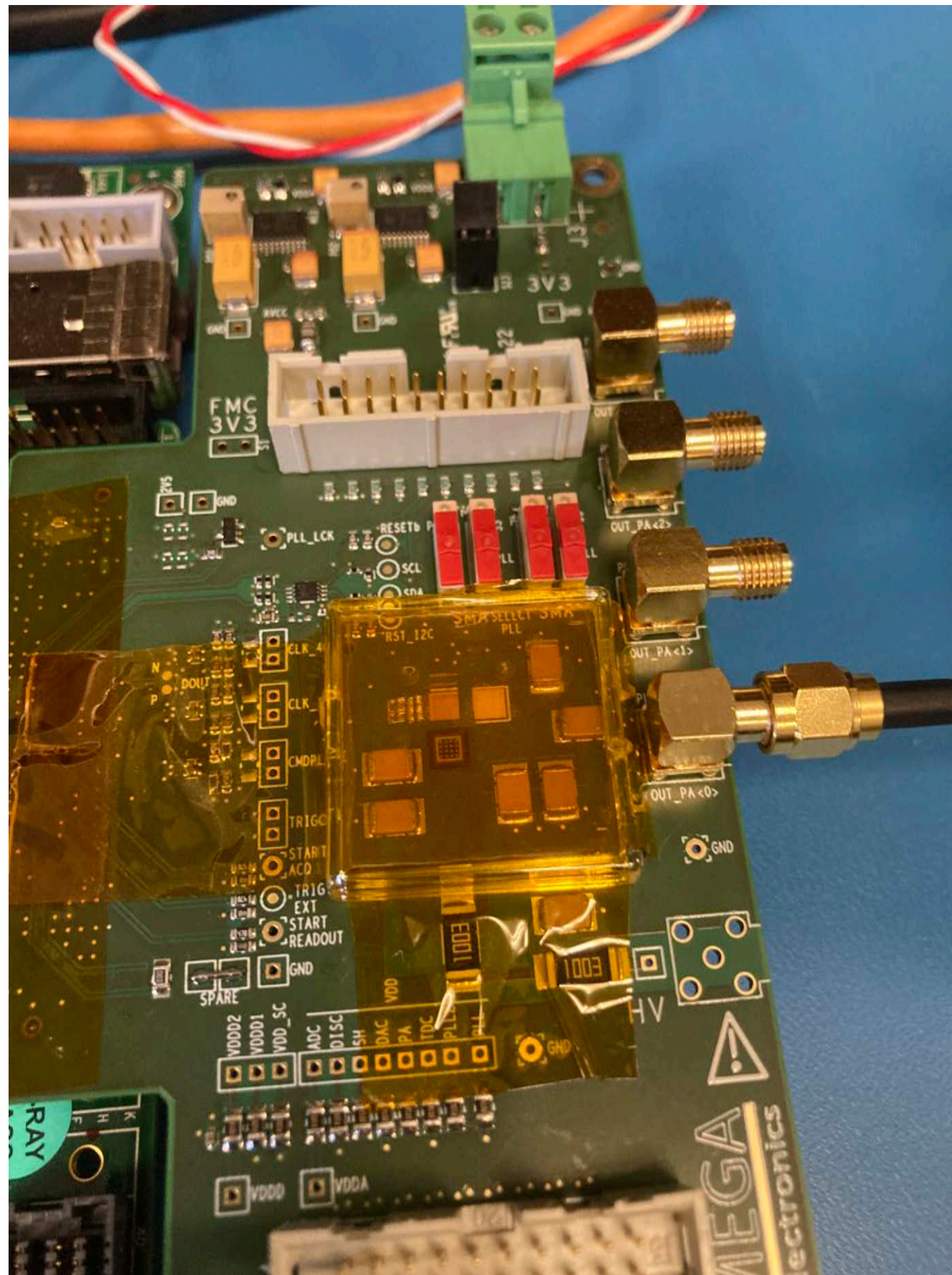
With a lot of help from Dominique, Laurent & team

Frist test: Pre-amplifier output

PCB board A1 and G1

All resisters are measured removing from the board, corrected as specified

For this study: we inject charge & study pre-amp output with a scope, reproduce results from Dominique's slides:

https://indico.bnl.gov/event/19528/contributions/76533/attachments/47836/81223/EICROC0_Progress_report_eRD112_20230_06_06.pdf

Updating the value of the resistors on PCB

PCB board A1 (only ASIC)

R5 = 150 ohm
R17 = 150 ohm
R52 = 30.1 kOhm
R54 = 4.22 kOhm
R57 = 30.1 kOhm
R58 = 4.22 kOhm
<u>M13 and M14 originally installed correctly.</u>
S23 installed, SPARE jumper installed.
ASIC wirebonded.

PCB board G1 (ASIC+sensor)

R5 = 150 ohm
R17 = 150 ohm
R52 = 30.1 kOhm
R54 = 4.22 kOhm
R57 = 30.1 kOhm
R58 = 4.22 kOhm
<u>**M13 only** was originally flipped, but has been corrected.</u>
S23 installed, SPARE jumper installed.
ASIC wirebonded.
SMA connectors were added for comparison testing.

We have tested all of the resistors out of the PCB network, and <u>they all match the correct nominal values</u>. In-network effective resistances remain the same as earlier testing. We have also applied corrections to the resistors, regulator IC, and jumpers

All resistors were updated, double-checked according to the instructions from the developers
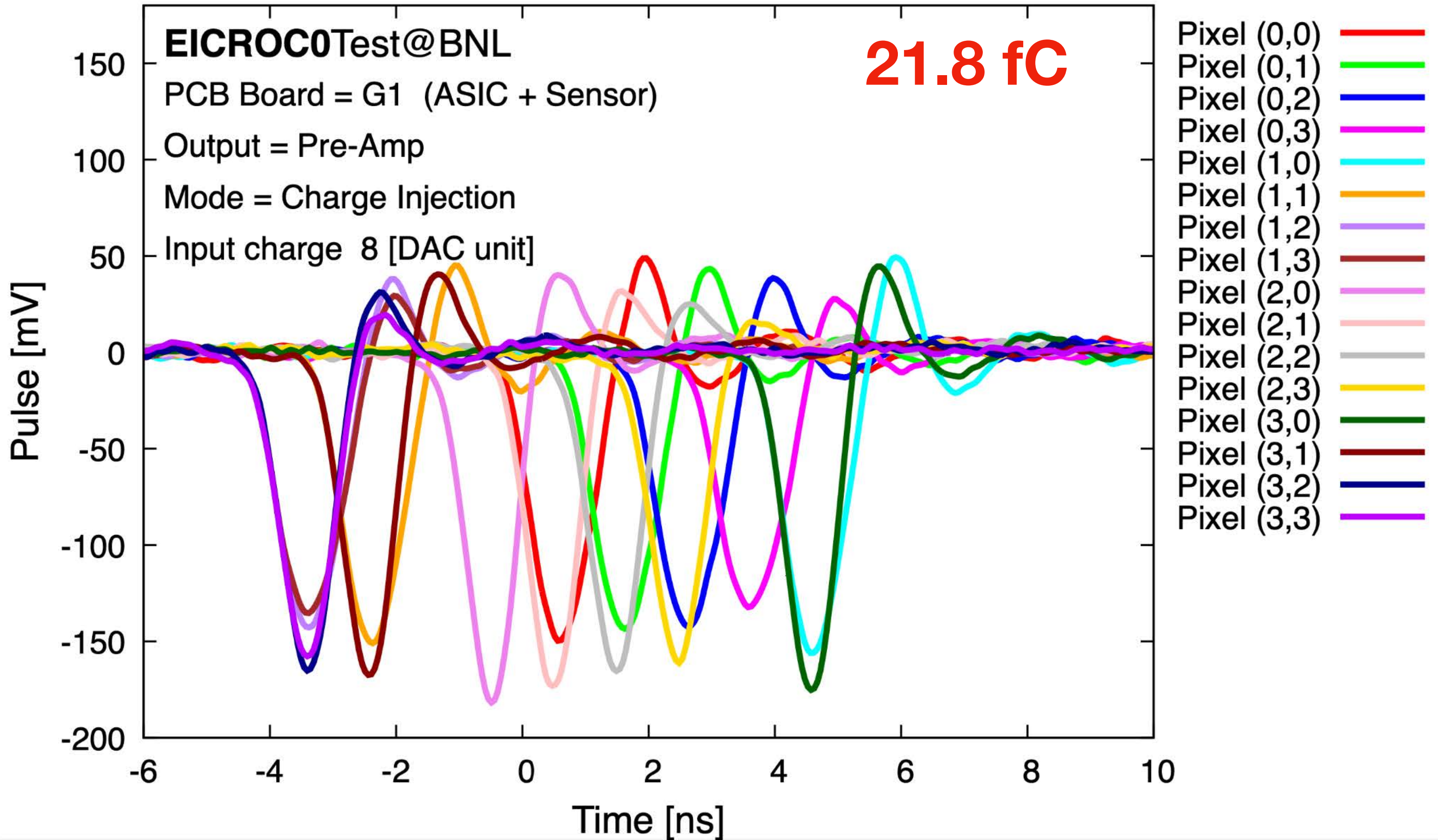
Pre-Amp output amplitudes: large charge

<P0>
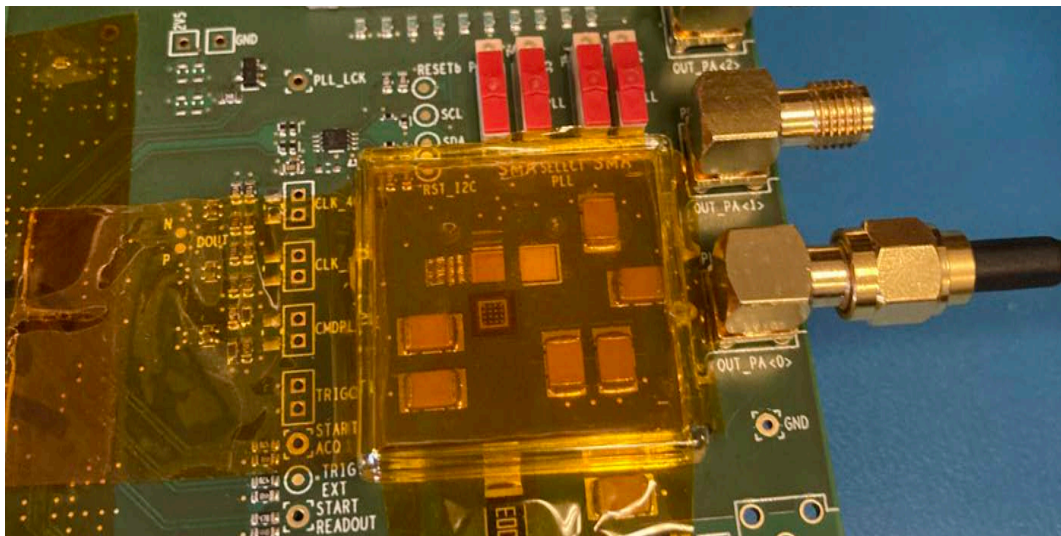
Pixel / Channel Mapping	Column 0	Column 1	Column 2	Column 3
Line 0	Pixel (0,0) #00	Pixel (1,0) #04	Pixel (2,0) #08	Pixel (3,0) #12
Line 1	Pixel (0,1) #01	Pixel (1,1) #05	Pixel (2,1) #09	Pixel (3,1) #13
Line 2	Pixel (0,2) #02	Pixel (1,2) #06	Pixel (2,2) #10	Pixel (3,2) #14
Line 3	Pixel (0,3) #03	Pixel (1,3) #07	Pixel (2,3) #11	Pixel (3,3) #15

We inject charge into each column

We select the pixel we read in the column by setting bit-4 of register EN_digprobe. Pixel (0,0) is only read in Column 0 and so on.

Input charge = 8 DAC = 21.8 fC

EICROC0Test@BNL
PCB Board = G1 (ASIC + Sensor)
Output = Pre-Amp
Mode = Charge Injection
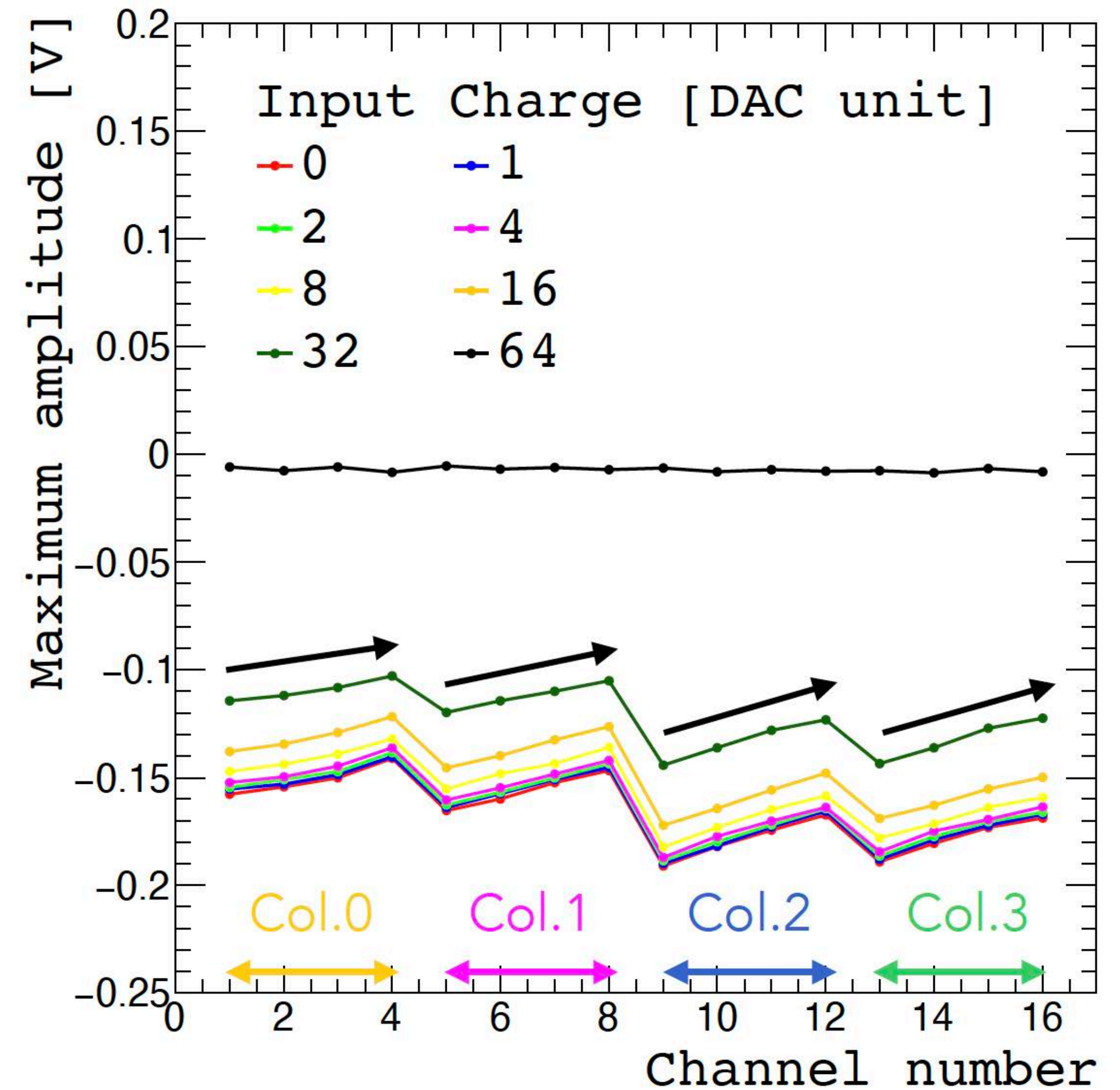Input charge 8 [DAC unit]

21.8 fC

All the pixels perform as per expectations

Column wise variation

In the same column, the larger pixel number
has a higher amplitude in all columns.

We need to understand why there is a
hierarchy in the maximum amplitude

Pre-Amp output amplitudes: small charge

Reg 0x20C dacb_pulser value	Tension [mV]	Charge [fC]
0	249,1	24,91
1	245,3	24,53
2	241,4	24,14
4	233,4	23,34
8	218,2	21,82
16	187,3	18,73
32	124,8	12,48
63	5,05	0,505

Input charge = 63 DAC =0.5 fC

0.5 fC

EICROC0Test@BNL

PCB Board = G1 (ASIC + Sensor)

Output = Pre-Amp

Mode = Charge Injection

Input charge 64 [DAC unit]

Pixel (1,0)
Pixel (1,1)
Pixel (1,2)
Pixel (1,3)

We get signals for the lowest charge injected, but the Pre-amplifier output is dominated by noise. Noise from remaining channels (columns) used as trigger
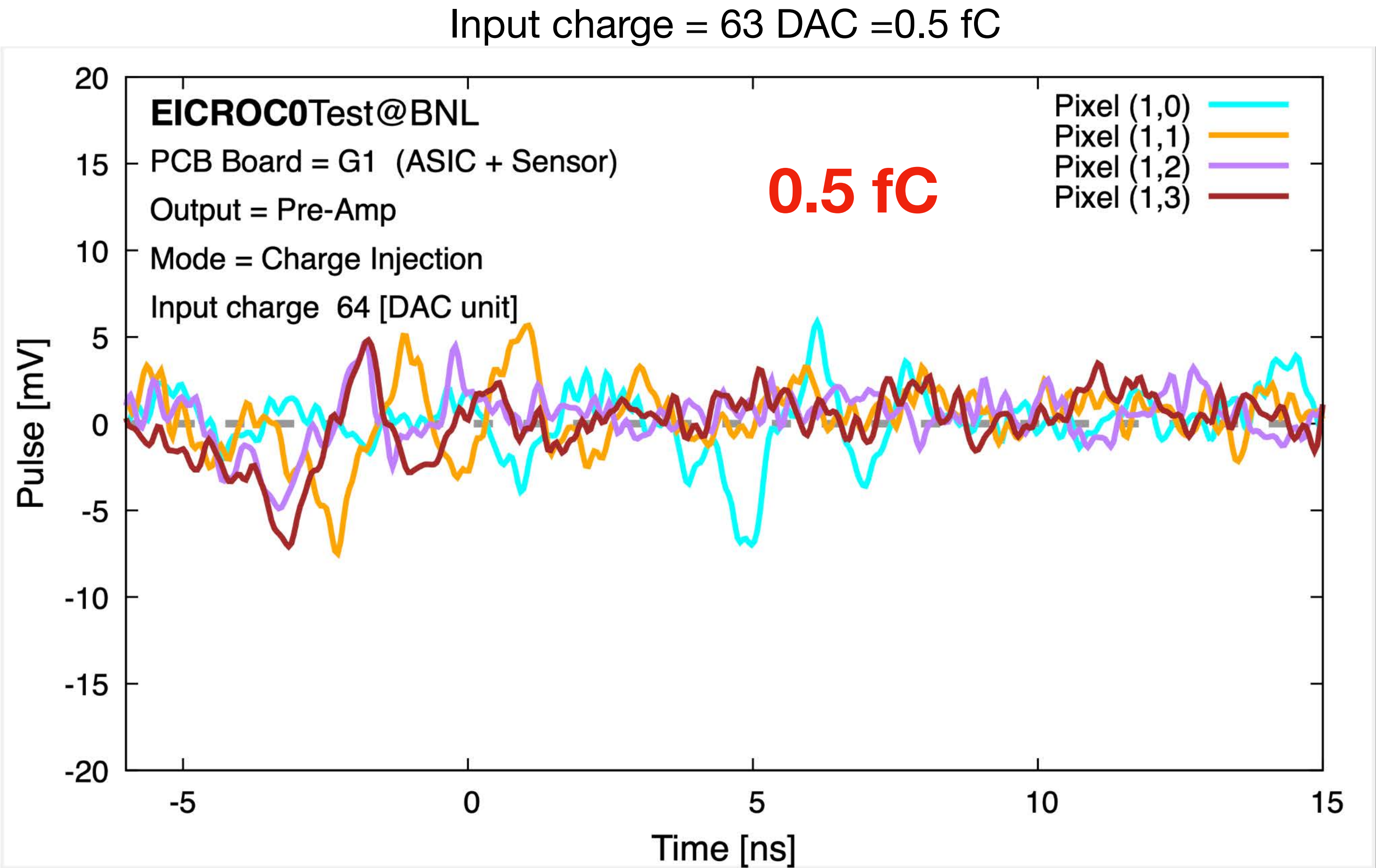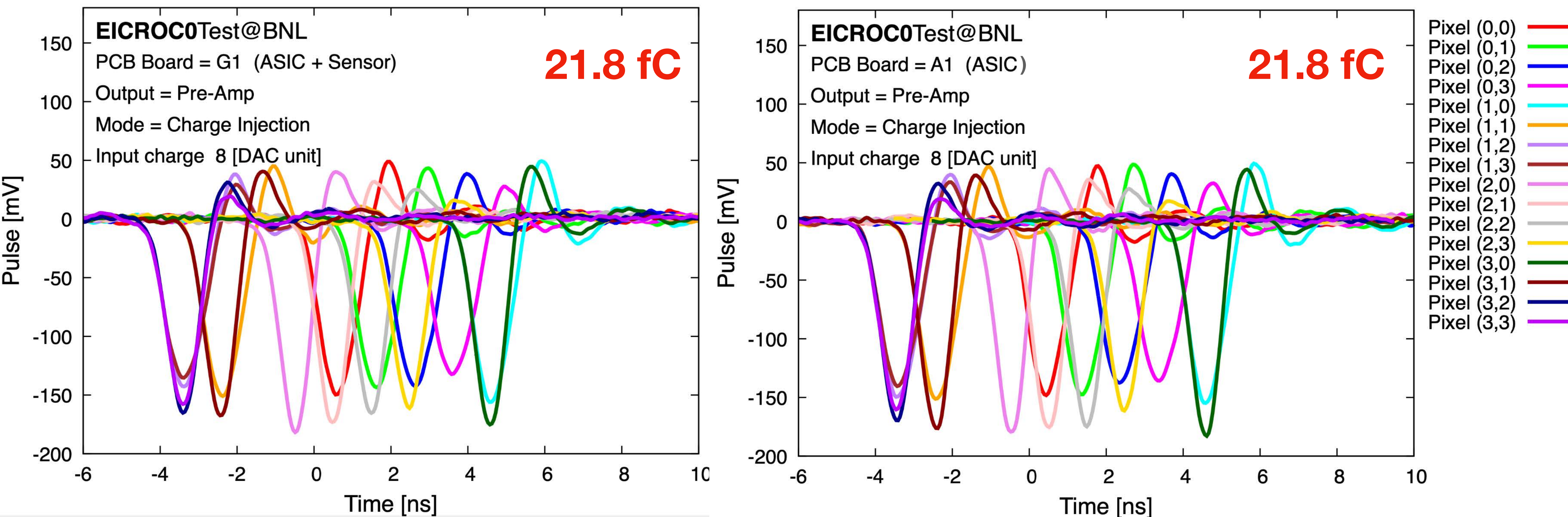
Noise dominated pulse for minimal injection

Cross checking with two different boards

Input charge = 8 DAC



Two PCB boards behave similarly

Absolute max. amplitude vs Injected charge

Reg 0x20C dacb_pulser value	Tension [mV]	Charge [fC]
0	249,1	24,91
1	245,3	24,53
2	241,4	24,14
4	233,4	23,34
8	218,2	21,82
16	187,3	18,73
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Q [fC] = C [fF] x U [mV]

C = 100 fF

Non-linear behaviour in general.

For a given injected charge, Columns 2 and 3 have greater absolute maximum amplitudes (of signal) in comparison to Columns 0 and 1.
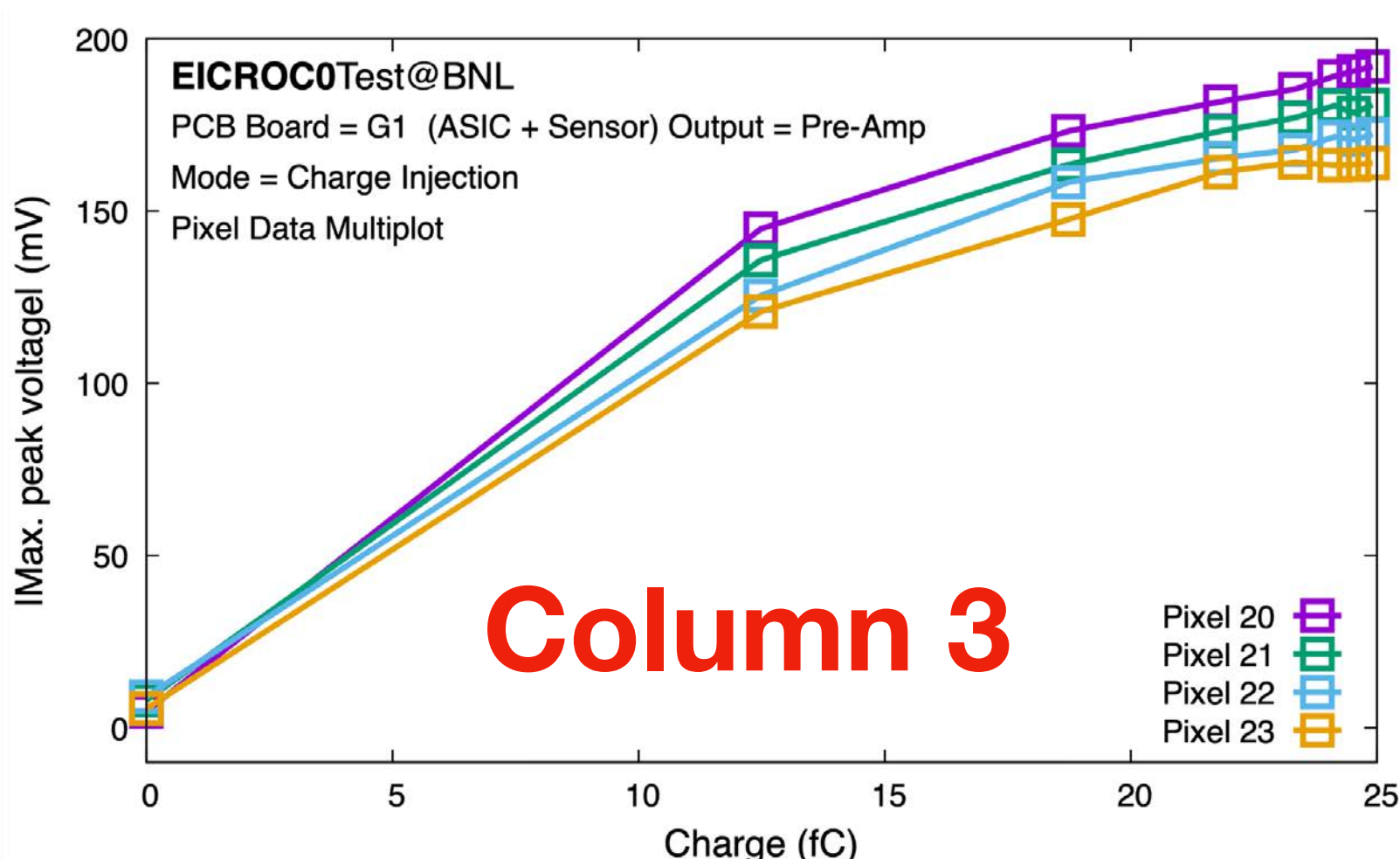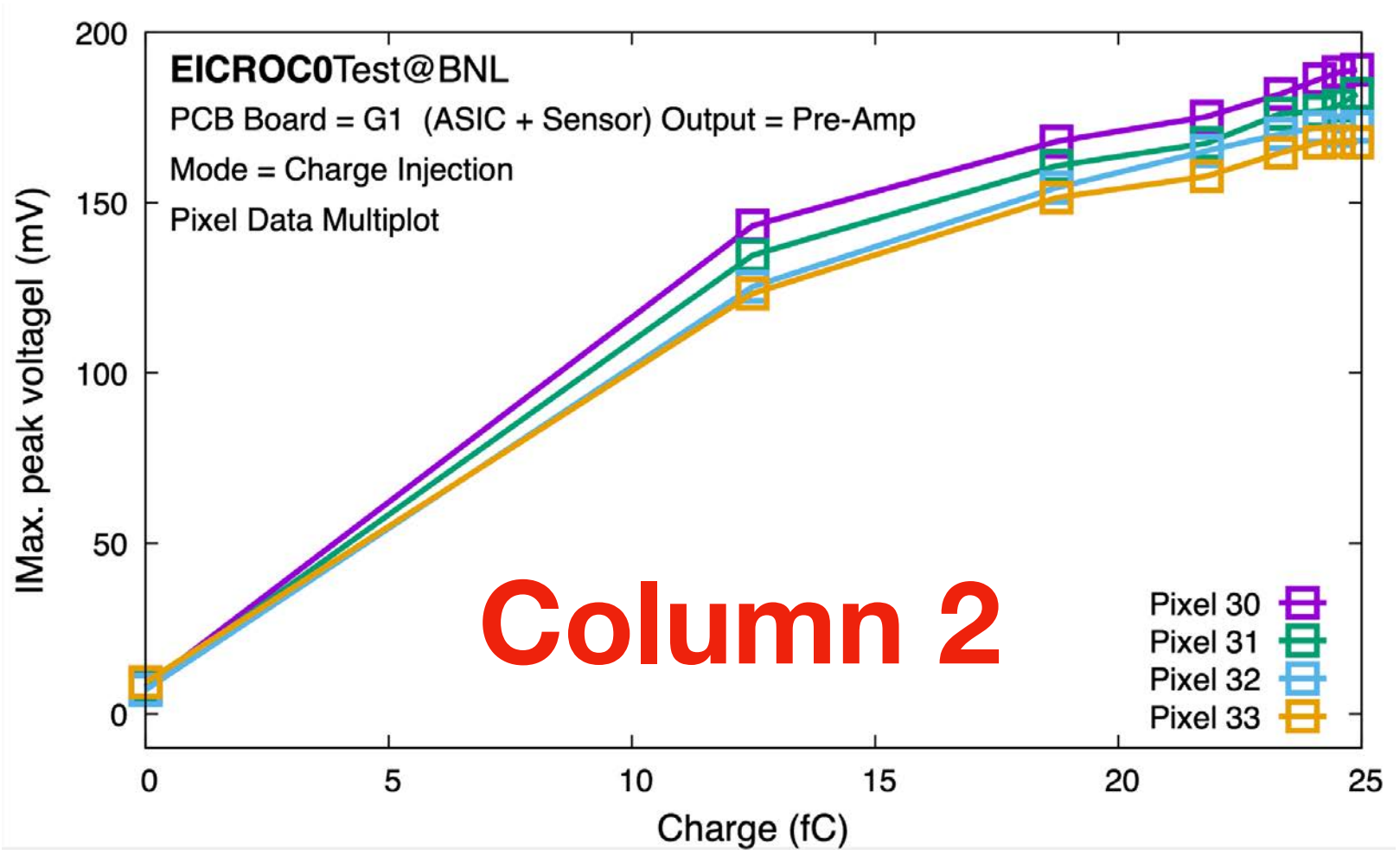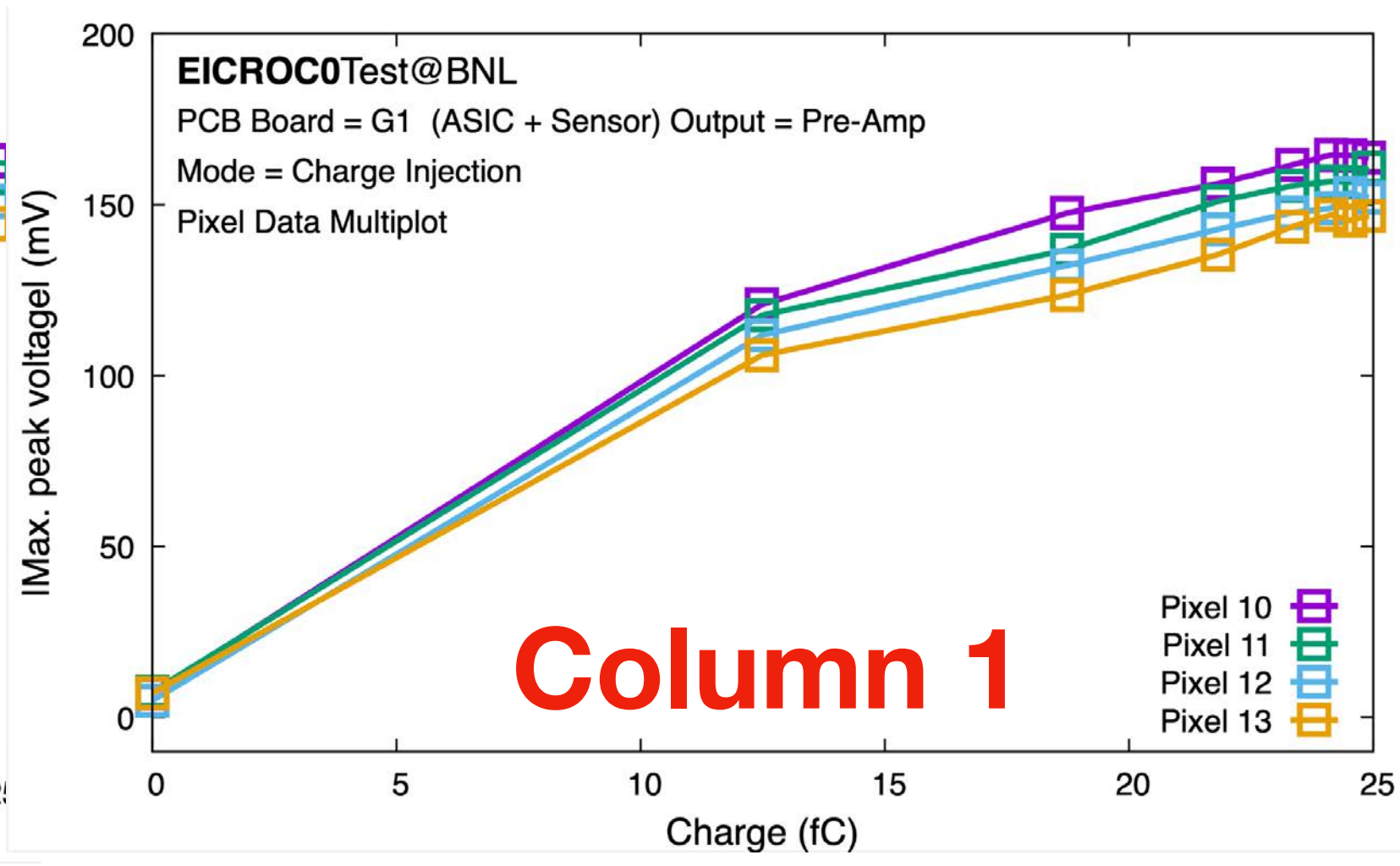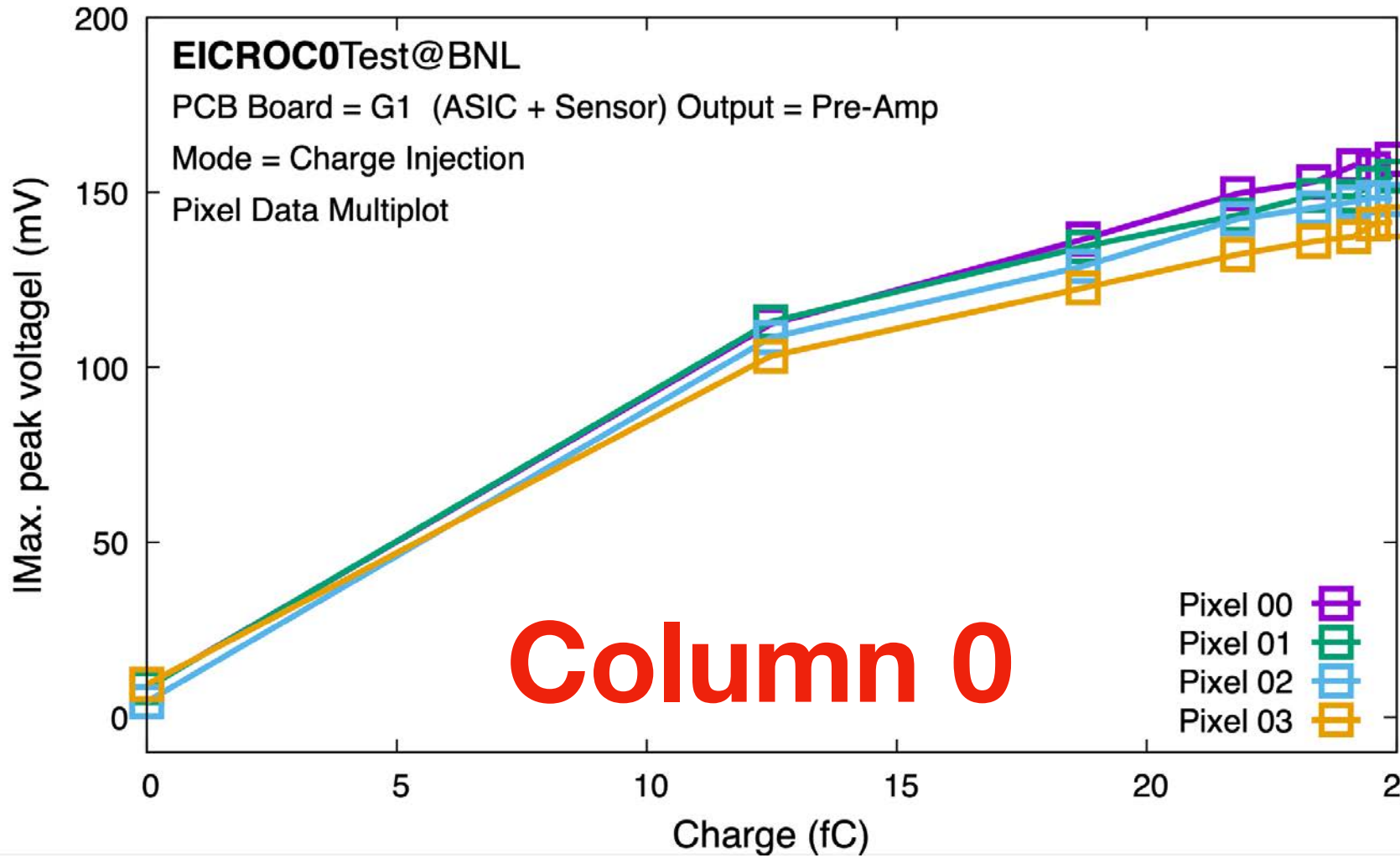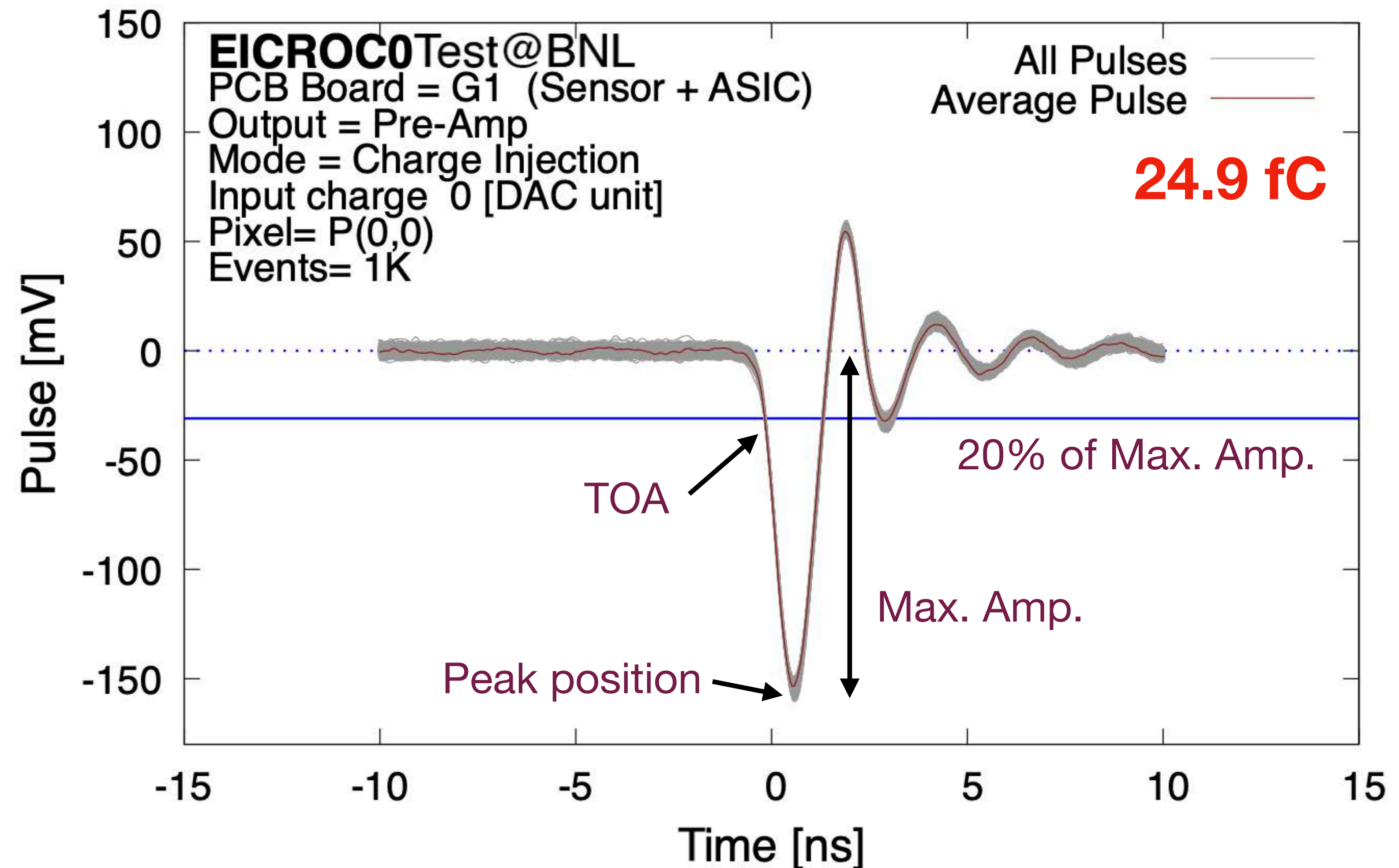

Correlated response as expected
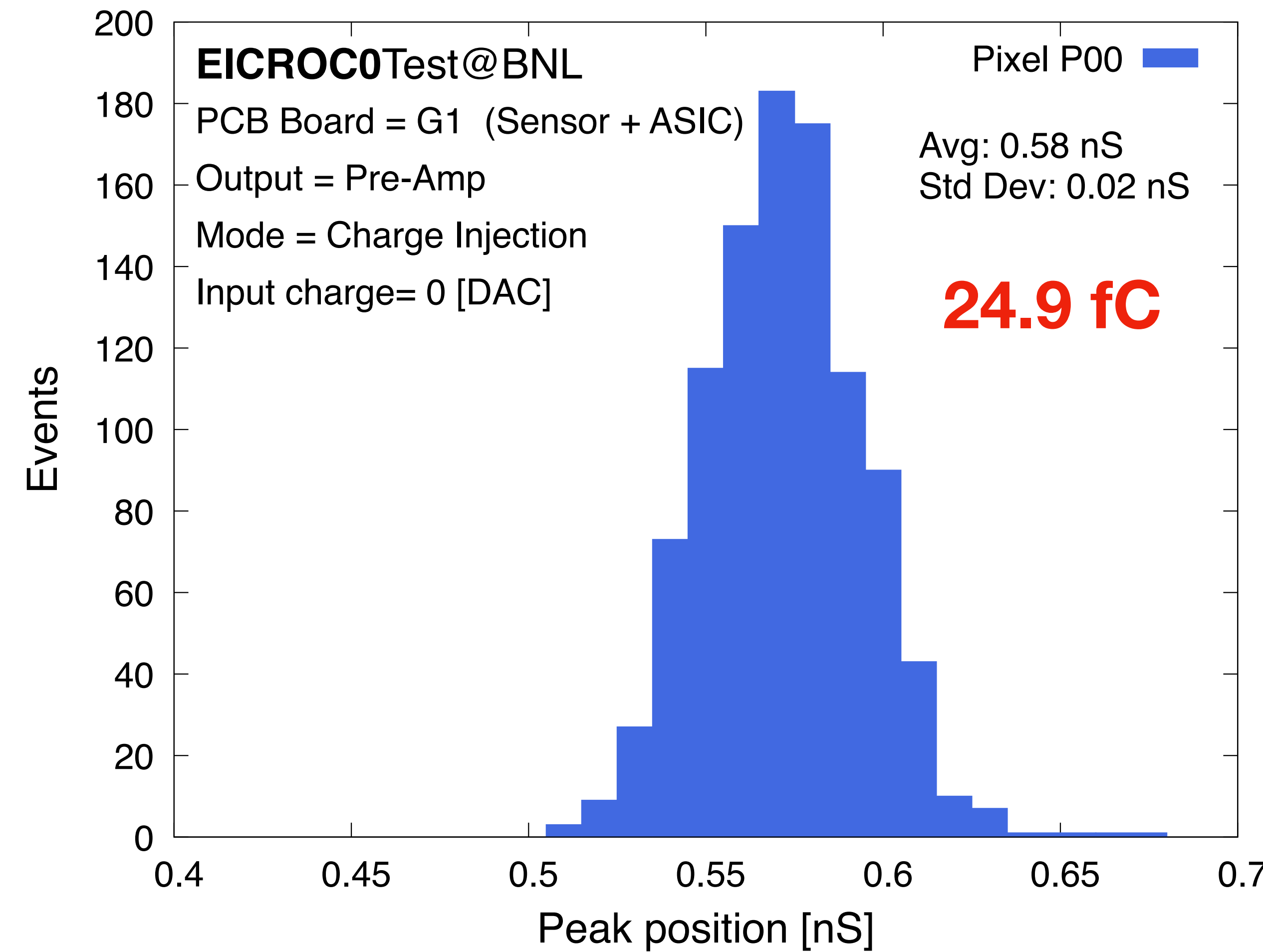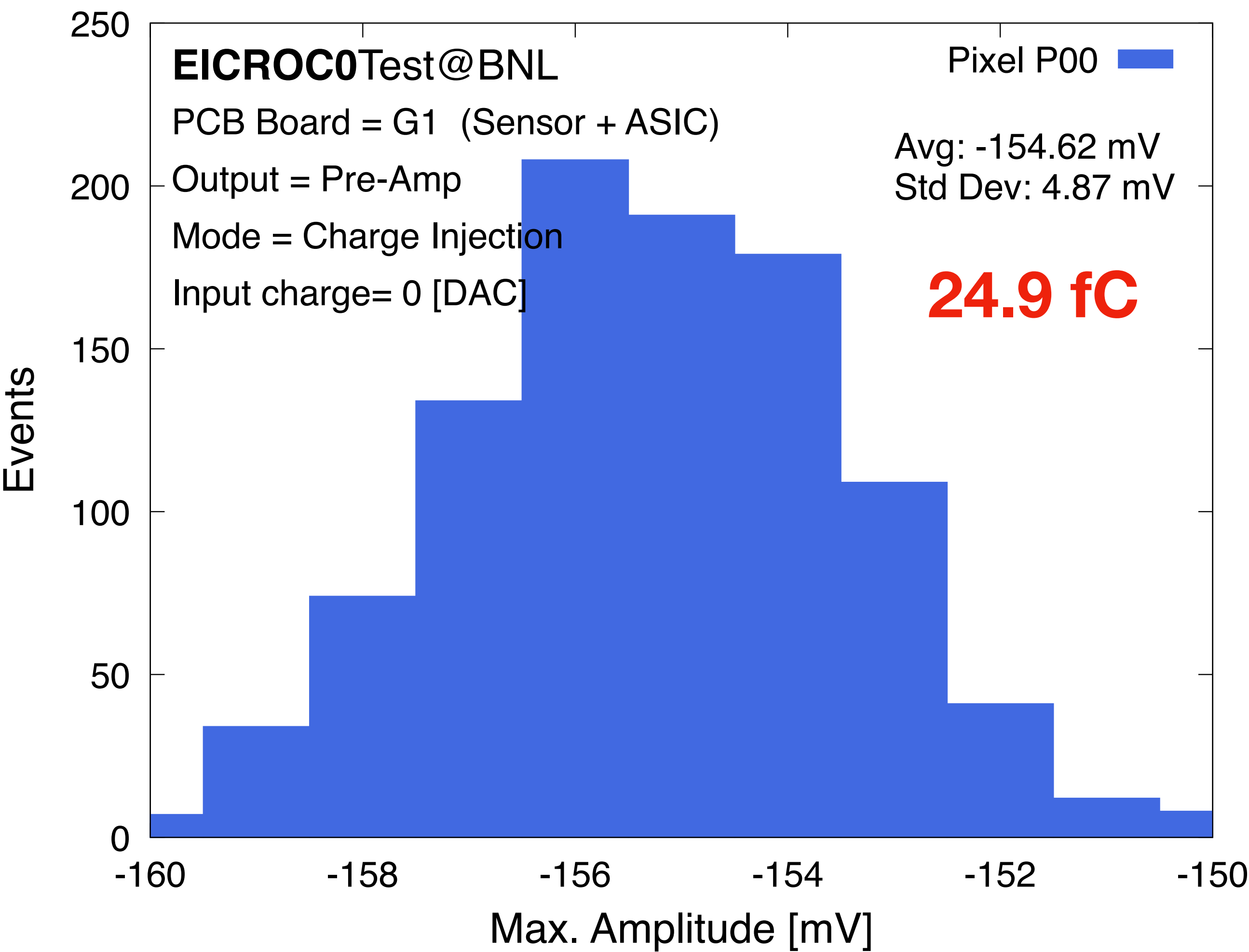
Average pulse shape & TOA

Time of arrival computed as threshold at 20 % of the |Max. Ampl.|

We collect 1K events to study the average behavior and pulse distributions
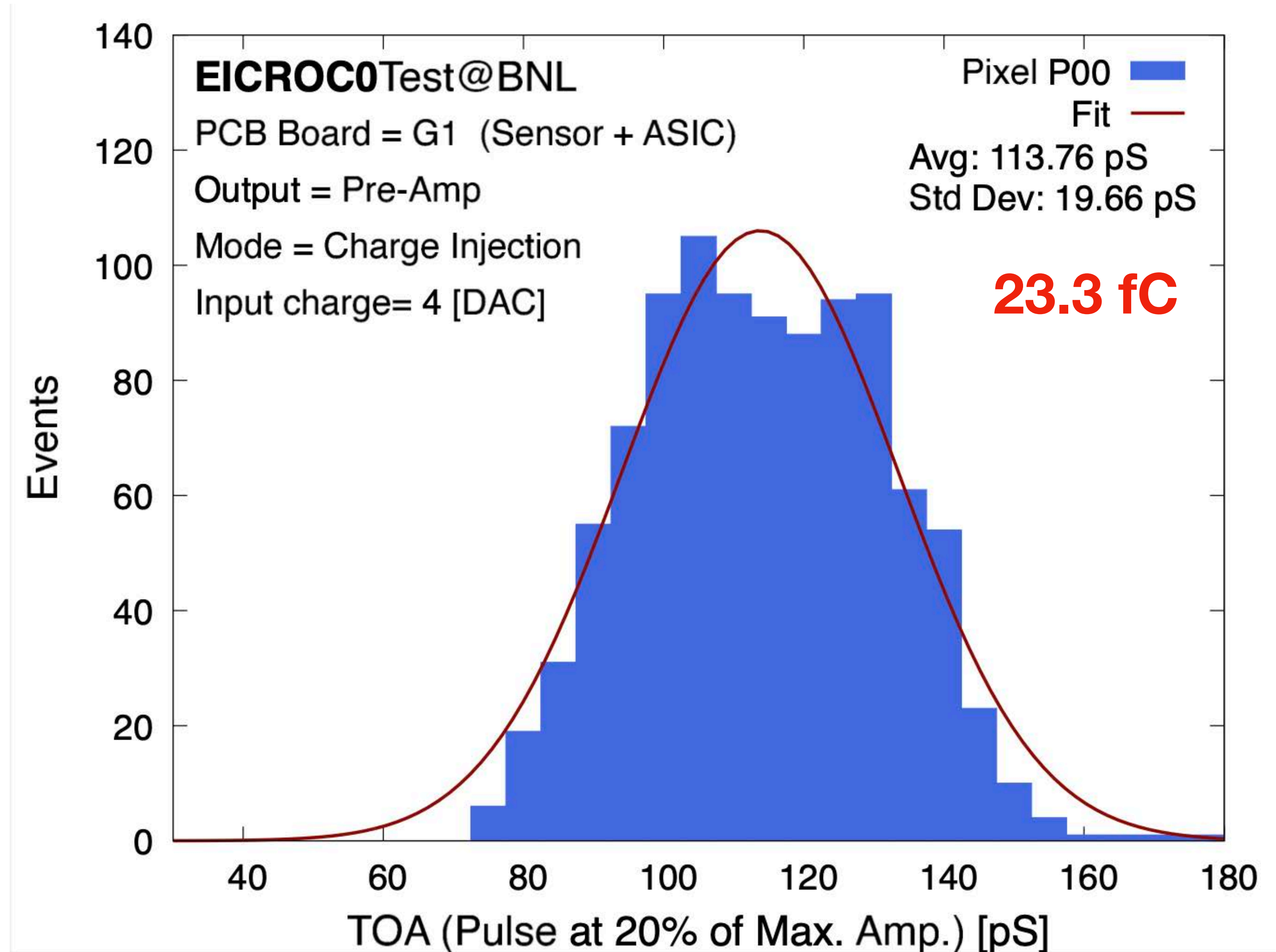
Study of the signal distributions

Peak amp. and position studies: More studies needed to understand the distribution

Jitter Investigation for Time of arrival

- This is a tentative study

- Jitter is equivalent to σ

- Mean Time of Arrival (ToA) sets the threshold for Constant Fraction Discriminator

We find a width of 20 pS for the TOA defined as time of 20% of the Max. Amp.

Summary

Procured EICROC0 ASIC PCB and bonded AC-LGAD + EICROC0 onto the PCB with BNL's instrumentation division

• Made necessary corrections to the PCB

• Acquired Xilinx development kit and set up a test stand at BNL

• Installed required software and firmware, currently modifying software for connections

• We have a fully operational test stand combining sensor, ASIC, and prototype board

• Performed some primary characterizations and replication of EICROCx developer's results
  • Read Pre-amp output with charge injection for all 16 pixels
  • Study Max. amps with injected charge
  • Tentative study of the distribution of amplitude and jitter

To Do:
  • Read the digitized output TDC/ADC, Pulse with clock ON/OFF
  • Characterization with sensor using a source