dRICH: interest for VTRX+

P. Antonioli on behalf of dRICH Collaboration

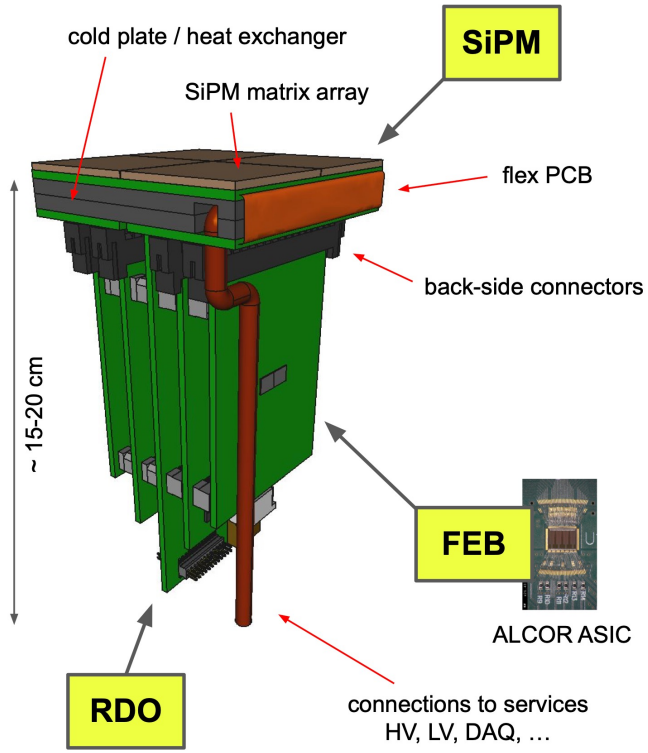
Why this update? / Quick summary

- Upon request of DAQ conveners
- Previously (orally since April, presentation given 1st June at this DAQ group) dRICH pointed out a “pre-order” for VTRX+ might be needed by ePIC given timing of massive HL-LHC production
- Here main focus is about why VTRX+ might be an interesting option for dRICH RDO

dRICH RDO recap within dRICH PDU

Photodetector unit

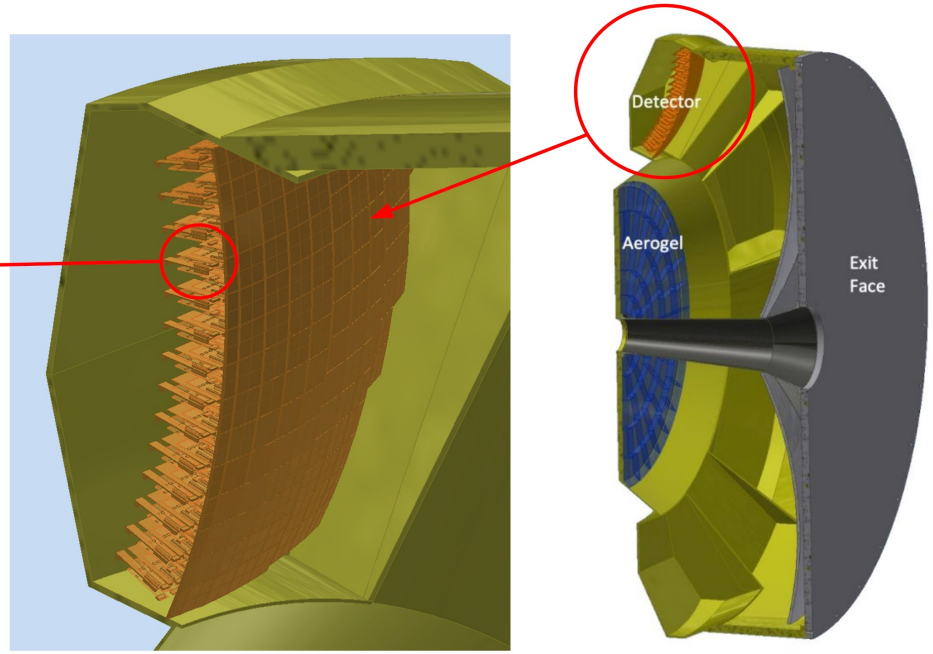
conceptual design of final layout



R. Preghenella [@Sep TIC meeting]

compact solution to minimise space

- cold plate and flex-PCB circuit
- uniform sensor cooling with no loss of active area
- all electronics and services on the back side



Shown at 14 Sep DAQ meeting

- The dRICH electronic - burger :

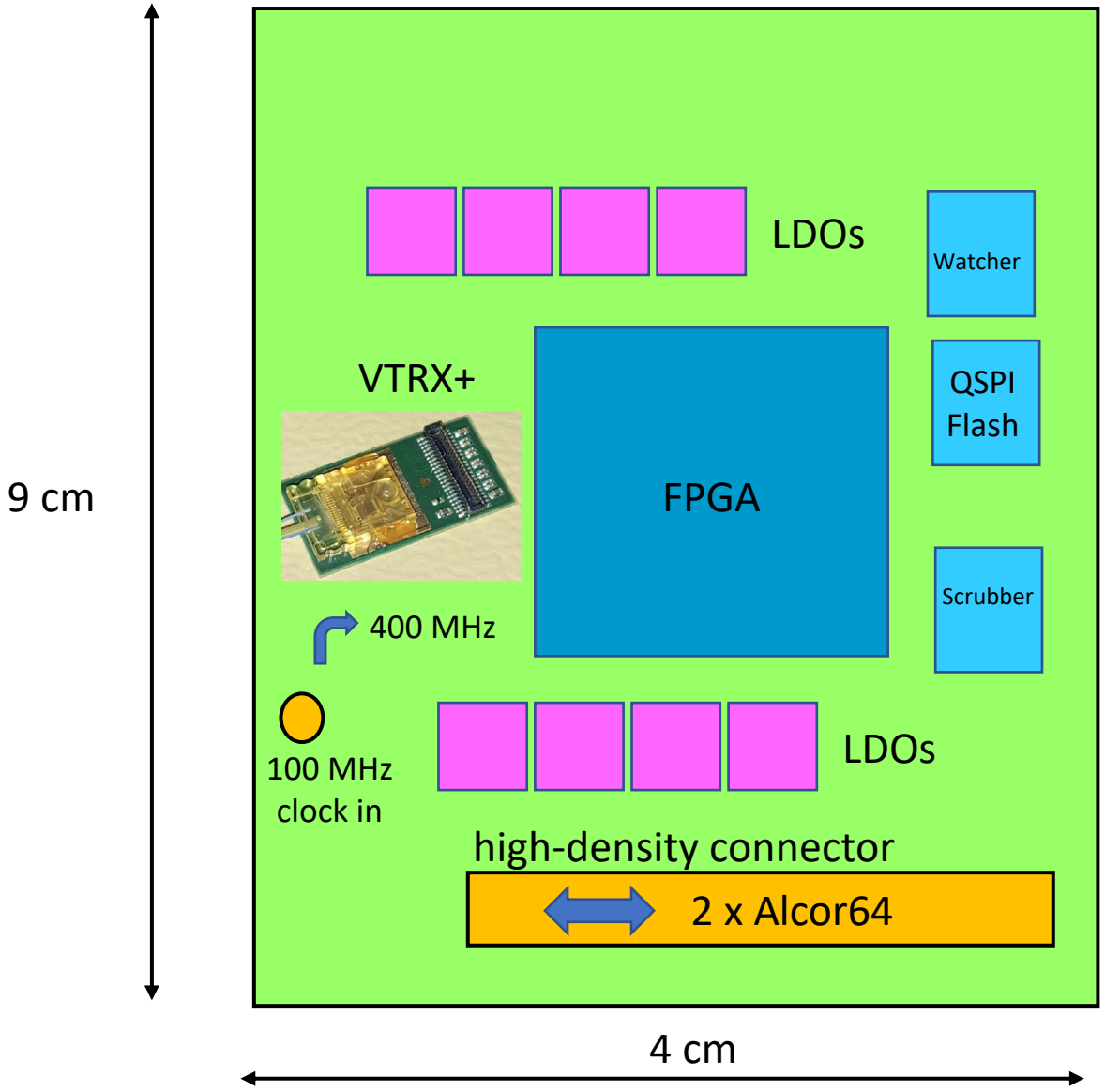
Main points for us:

1) RDO per PDU → 1242 RDO
2) space constraints

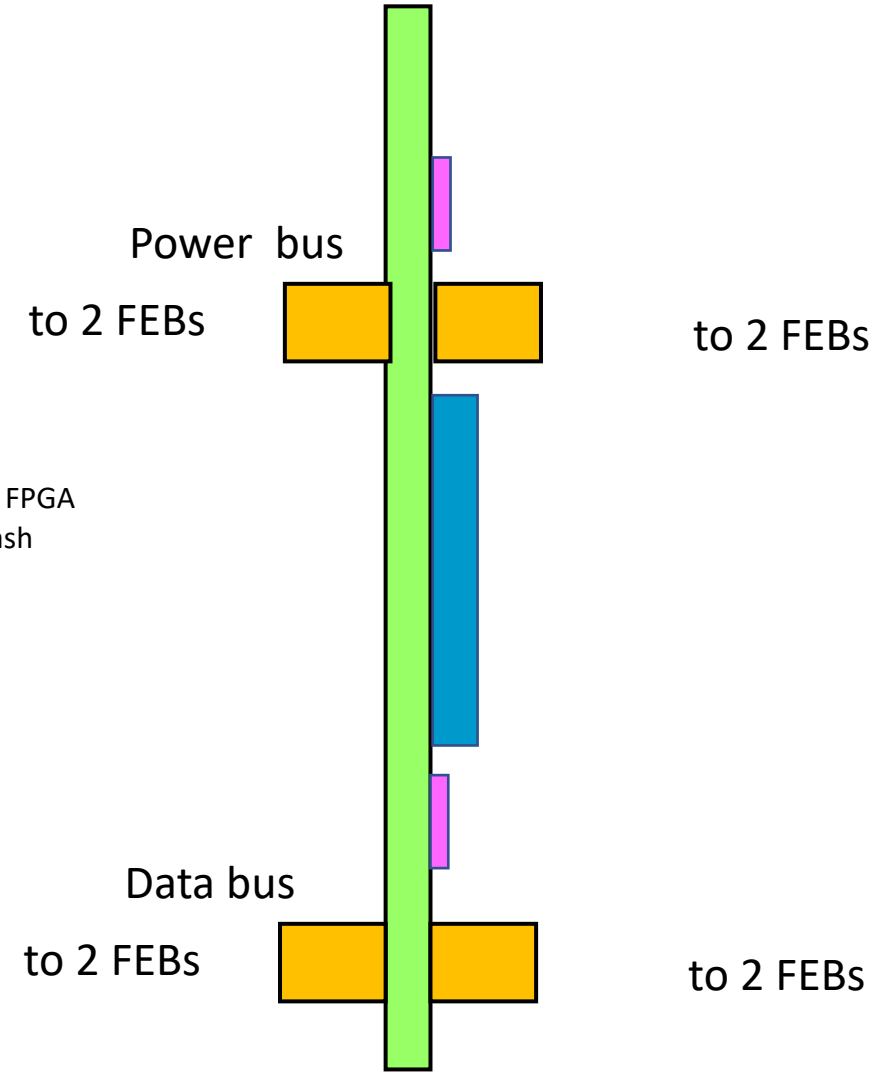
Current evaluation of dRICH RDO dimensions: **4 x 9 cm²**

What we have on such RDO?

front view



side view



(With Microsemi FPGA we avoid QSPI flash and scrubber)

not on scale, not a real placement !!!

Minimal list

List of components

1 HV connector: V bias 2 LV connectors: “analog” and “digital” optical link: 1 TX/1 RX	I/O toward control panel/etc
1 FPGA 3 LDOs for FPGA clock	On-board
connectors on both sides to route LV lines + Vbias to FEB connectors on both sides to route data lines to FEB	I/O toward FEB

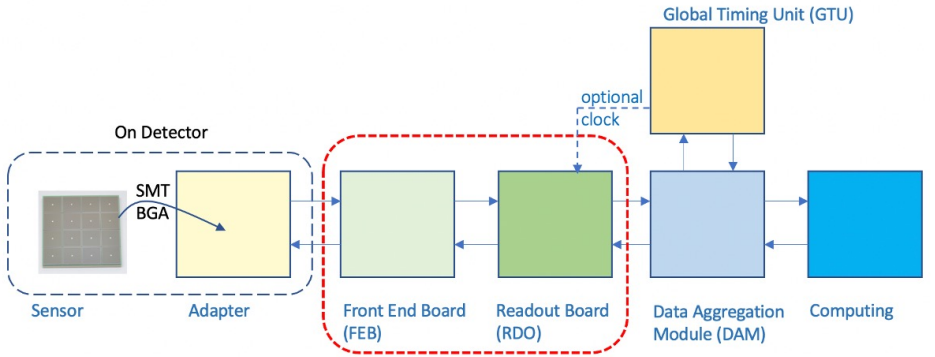
Design of full-fledged prototype scheduled for 2024
Asked funds to INFN and eRD109

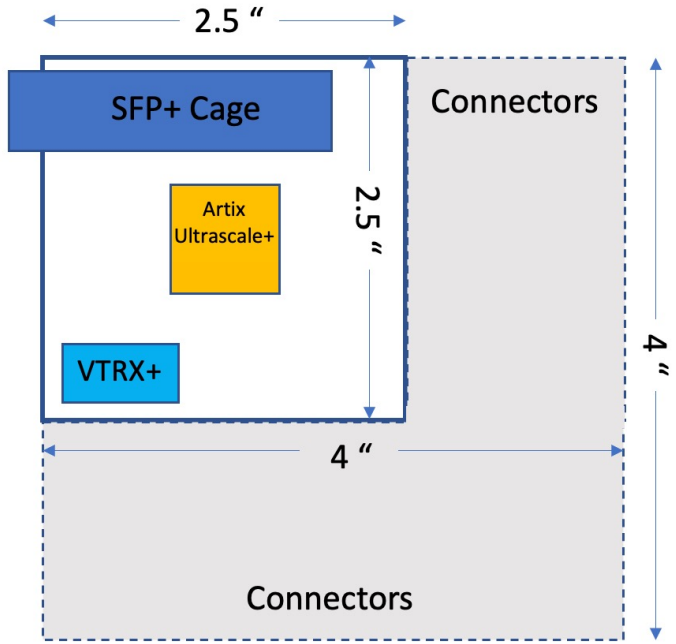
Note about specs on standard ePIC RDO

David Abbott at DAQ meeting 20th July

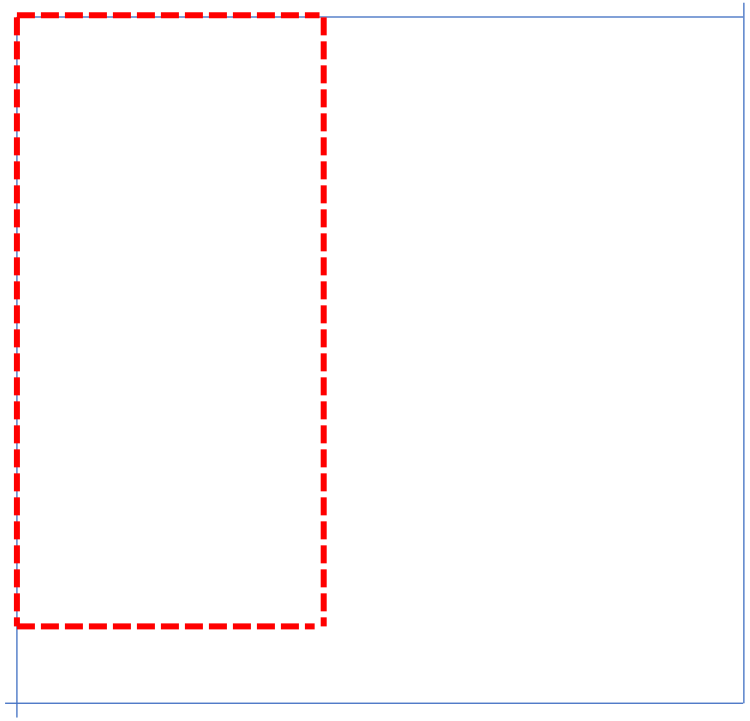
RDO Specifications/Guidance

- Nominally 2.5 in^2 for common RDO components including FPGA and optical link options (for example if it is integrated on the same PCB as the FEB). For standalone RDO, allow for up to 4 in^2 to provide space for copper-based connectors to FEBs.
- Power requirements: 3-5 Watts. Allow for at least two LV levels nominally 5V (for optics) and a lower voltage for FPGA power and ASIC signal management.
  - Consider using radiation tolerant switching voltage regulators (e.g. from CERN).
- Multiple optical link interfaces allow for flexible implementation of the RDO as either a standalone readout solution or use with the DAM boards. They can also be used for accepting an alternative low-jitter clock input.
  - Samtec Firefly connectors are also a potential option as they have a footprint similar to VTRX and also provide MTP options.





Optical link and RDO dimensions



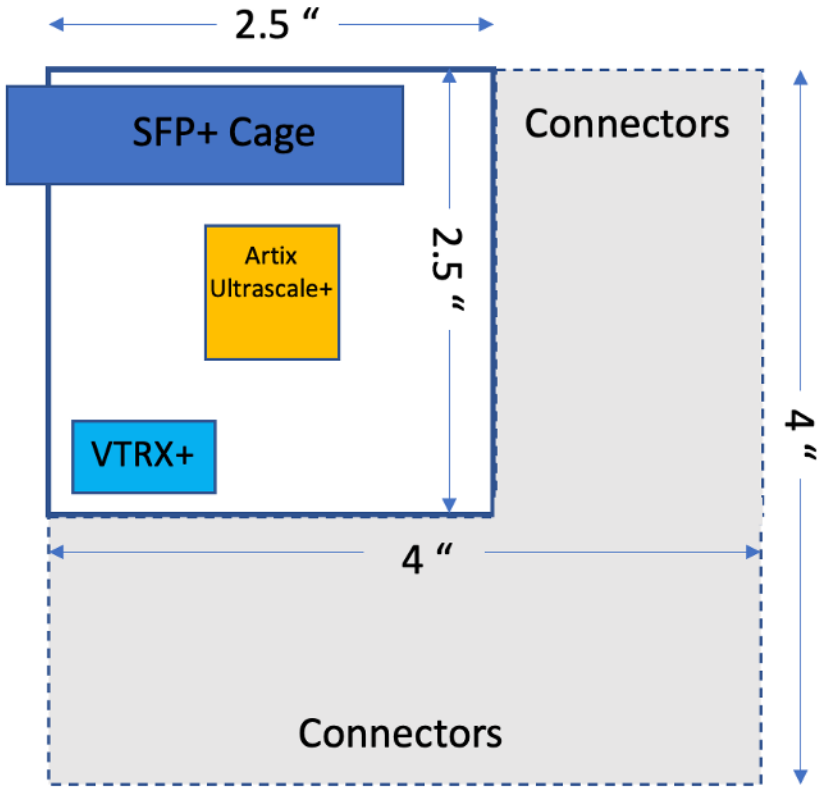


Table 1. Dimension Table for Drawing of SFP Transceiver

Designator	Dimension (mm)	Tolerance (mm)	Comments
A	13.7	± 0.1	Transceiver width, nosepiece or front that extends inside cage
B	8.6	± 0.1	Transceiver height, front, that extends inside cage
C	8.5	± 0.1	Transceiver height, rear
D	13.4	± 0.1	Transceiver width, rear
E	1.0	Maximum	Extension of front sides outside of cage, see Note 2 Figure 1B
F	2.3	Reference	Location of cage grounding springs from centerline, top
G	4.2	Reference	Location of side cage grounding springs from top
H	2.0	Maximum	Width of cage grounding springs
J	28.5	Minimum	Location of transition between nose piece and rear of transceiver
K	56.5	Reference	Transceiver overall length
L	1.1x45°	Minimum	Chamfer on bottom of housing
M	2.0	± 0.25	Height of rear shoulder from transceiver printed circuit board
N	2.25	± 0.1	Location of printed circuit board to bottom of transceiver
P	1.0	± 0.1	Thickness of printed circuit board
Q	9.2	± 0.1	Width of printed circuit board
R	0.7	Maximum	Width of skirt in rear of transceiver
S	45.0	± 0.2	Length from latch shoulder to rear of transceiver
T	34.6	± 0.3	Length from latch shoulder to bottom opening of transceiver
U	41.8	± 0.15	Length from latch shoulder to end of printed circuit board
V	2.6	± 0.05	Length from latch shoulder to shoulder of transceiver outside of cage (location of positive stop).
W	1.7	± 0.1	Clearance for actuator tines
X	9.0	Reference	Transceiver length extending outside of cage, see Note 2 Figure 1B
Y	2.0	Maximum	Maximum length of top and bottom of transceiver extending outside of cage, see Note 2 Figure 1B
Z	0.45	± 0.05	Height of latch boss
AA	8.6	Reference	Transceiver height, front, that extends inside cage
AB	2.6	Maximum	Length of latch boss (design optional)
AC	45°	± 3°	Entry angle of actuator
AD	0.3	Maximum	Radius on entry angle of actuator
AE	6.3	Reference	Width of cavity that contains the actuator
AF	2.6	± 0.05	Width of latch boss (design optional)
AG	0.40	Minimum	Maximum radius of front of latch boss, 2 places (design optional)

4” x 4 “ standard RDO

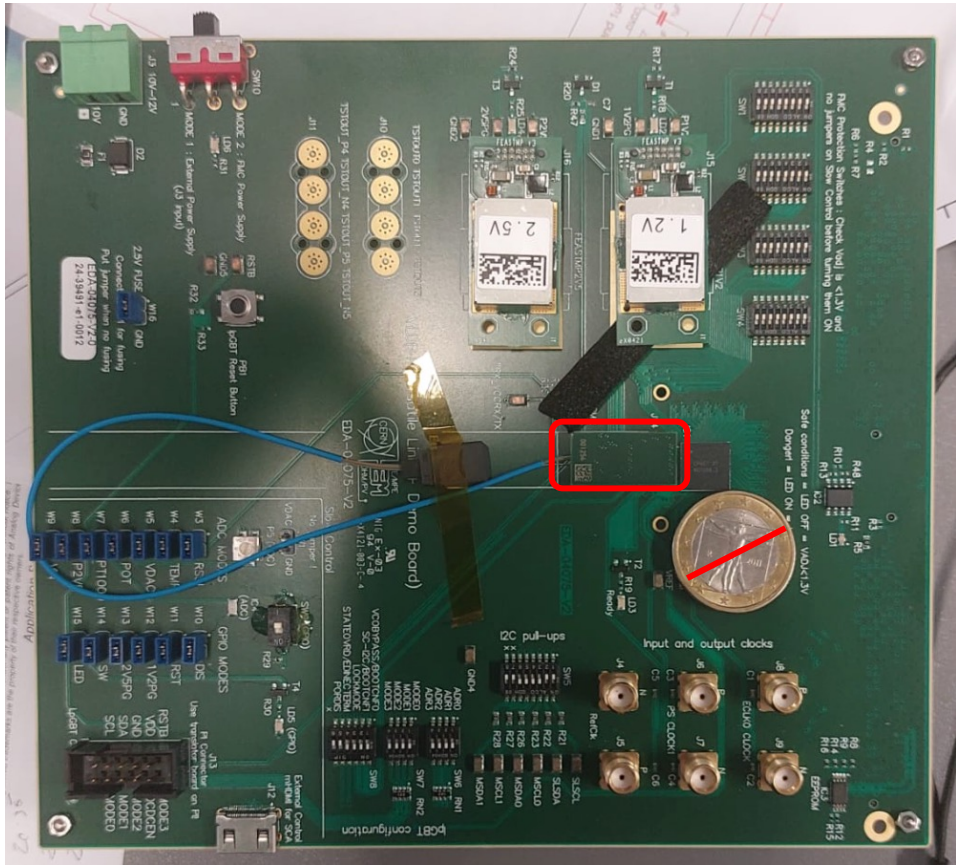
1.57” x 3.45” dRICH RDO

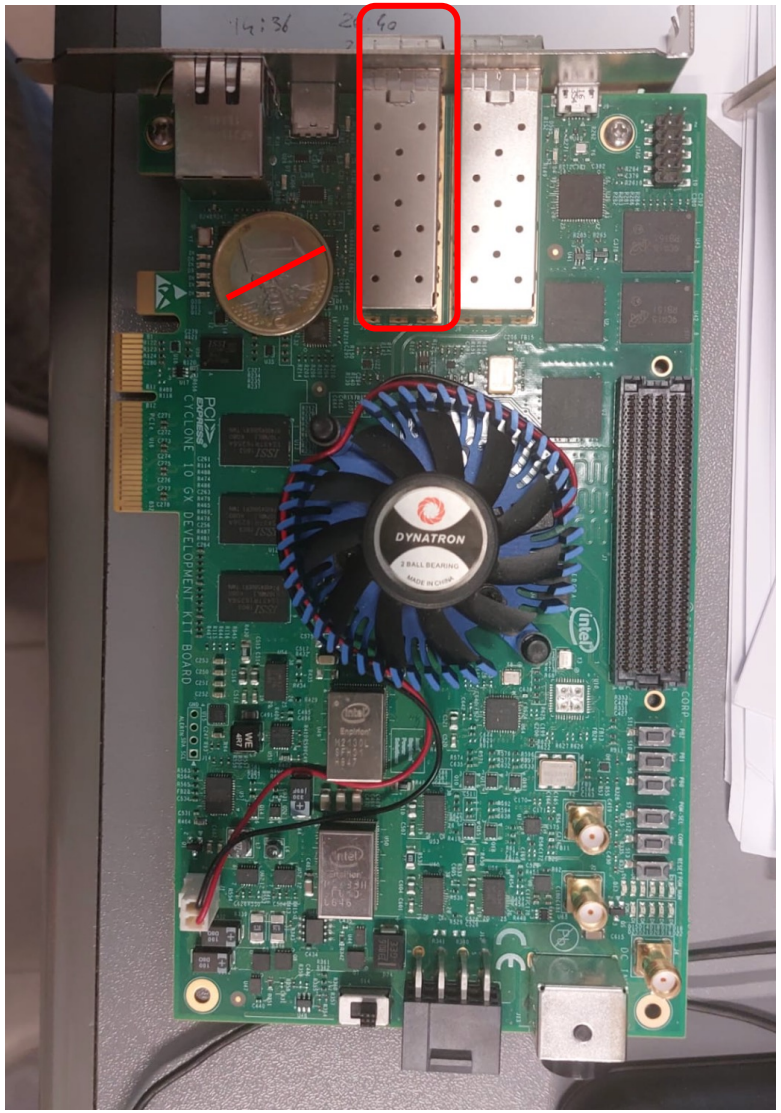
Obvious interest on trying to use a very compact optical link

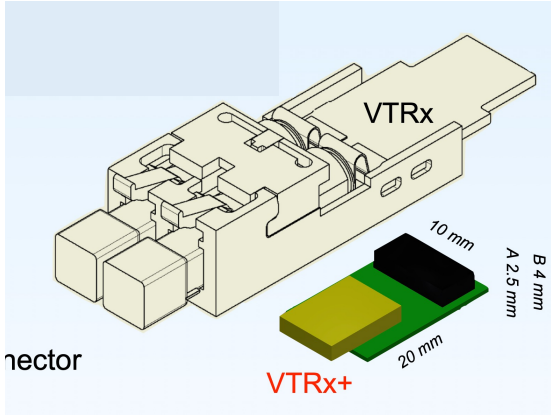
1 SFP takes a lot of space!

(just an image view)

VLDB+ CERN card (VTRX+ “demo board”)



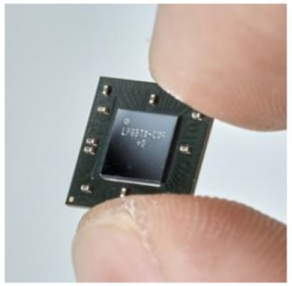


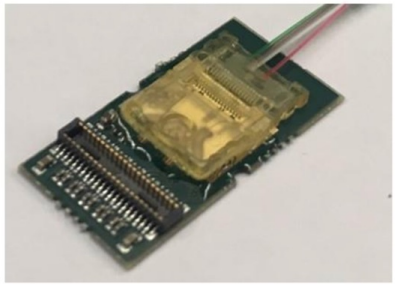


(from June presentation at DAQ group)

Optical transceiver: VTRX+

- **lpGBT and Versatile link +**
  - https://ep-ese.web.cern.ch/project/lpgbt-and-versatile-link
  - lpGBT
  - VTRX+
- **produced for LS3/Run4**
- **no iteration after that for mass production is planned (for now)**
  - performance assumed to be good for LS4/Run5
  - if this is not correct → we need to speak up now
  - future development effort goes to EP-RD WP6





Slide from A. Kluge, ALICE Electronics coordinator

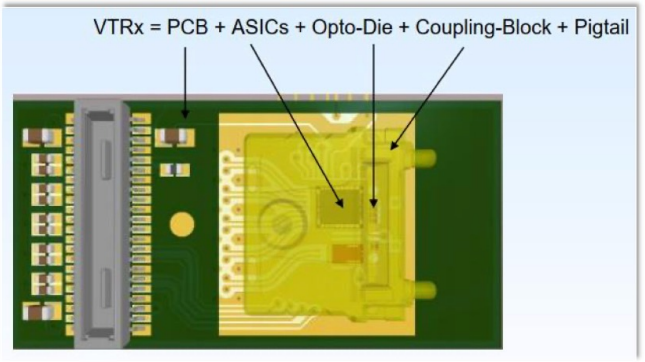
Note lpGBT not an option for EIC, but VTRX+ is a miniaturized opt. tranceiver (rad hard) that might be interesting

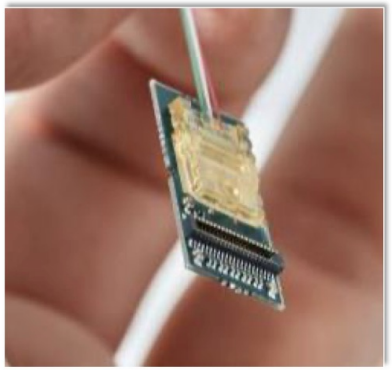
1/06/2023 ePIC DAQ WG RDO & DAQ - dRICH 10

(from June presentation at DAQ group)

VTRx+ Front-end Module

- **Versatile**
  - Up to 4 Tx + 1 Rx, configurable by masking channels
- **Miniaturised**
  - 20 x 10 x 2.5 mm
- **Pluggable**
  - Electrical connector
- **Data-rate**
  - Tx: up to 4×10 Gb/s, Rx: 2.5 Gb/s
- **Environment**
  - Temperature: -35 to + 60 °C
  - Total Dose: 100 Mrad
  - Total Fluence: $1x10^{15}$ n/cm² and $1x10^{15}$ hadrons/cm²
- **Status**
  - Pre-production ongoing
  - Solving problems with module assembly
  - Alignment of optical components
  - Ramping up to 2k modules/month in 2023





A. Kluge EP-ESE 10 May, 2023 6

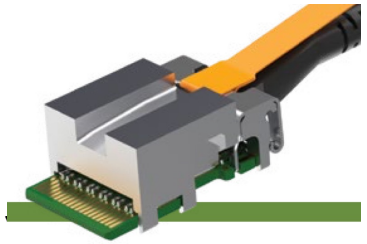
Slide from A. Kluge, ALICE Electronics coordinator

1/06/2023 ePIC DAQ WG

- **quantity and commitment to buy needs to be settled by end of 2023**
  as components need to be purchased

Additional considerations and doubts

- VTRX+ is a 4 TX + 1 RX transceiver. At dRICH we would use just 1 TX line → THIS IS POSSIBLE (and done @ LHC)
- VTRX+ is normally used paired with 1 to 4 lpGBT ASIC (RX is shared). We wouldn't need a lpGBT (what SVT will do?)
- VTRX+ can be used just as a transceiver directly connected to FPGA → THIS HAS TO BE VERIFIED (*)
- VTRX+ cost is O(100 EU) (source: a CERN colleague but not official quote, Jo knows more?)
- Radiation hardness would be a bonus for us
- Bandwidth limited at 10.25 Gb/s (not sure however if it comes from lpGBT or VTRX+)



An alternative solution suggested in this group was SAMTEC FireFly (Optical Micro Flyover system)
https://www.mouser.it/datasheet/2/527/ecuo-2854138.pdf
Preliminary checks show that it has 4 TX/RX + larger form factor + higher cost (328 EUR each)

If ePIC can "pre-order" VTRX+, dRICH would be interested to explore the VTRX+ option but we are in a difficult position (test/prototyping cycle still to be started + validate VTRX+ without lpGBT needed + COTS SFP might fit?) to be "assertive". On the other hand at the end of this year (apparently) we could loose access to VTRX+ for ever

The amount of VTRX+ for dRICH would be 1500 (1250 + spares…)

(*) receivers will provide the interface to FPGAs. The VL+ is designed to operate together with the lpGBT Serializer/Deserializer (SerDes) [1], although other SerDes types can be supported. The

J. Troska et al., PoS(TWEPP-17)048