OAK RIDGE National Laboratory

SVT Readout Considerations

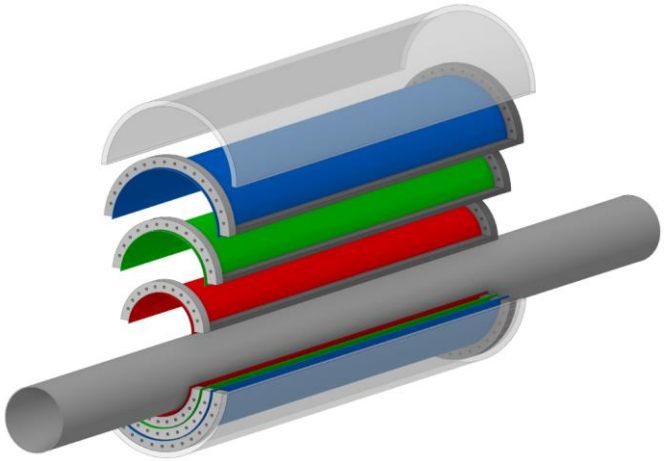
J. Schambach

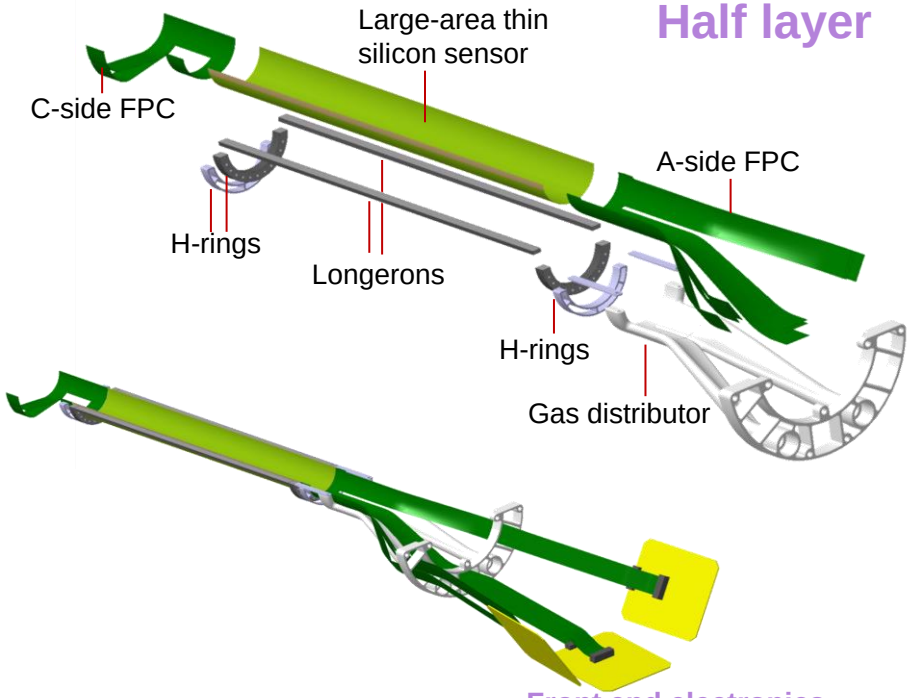
On behalf of the SVT Collaboration

ORNL is managed by UT-Battelle LLC for the US Department of Energy

U.S. DEPARTMENT OF ENERGY

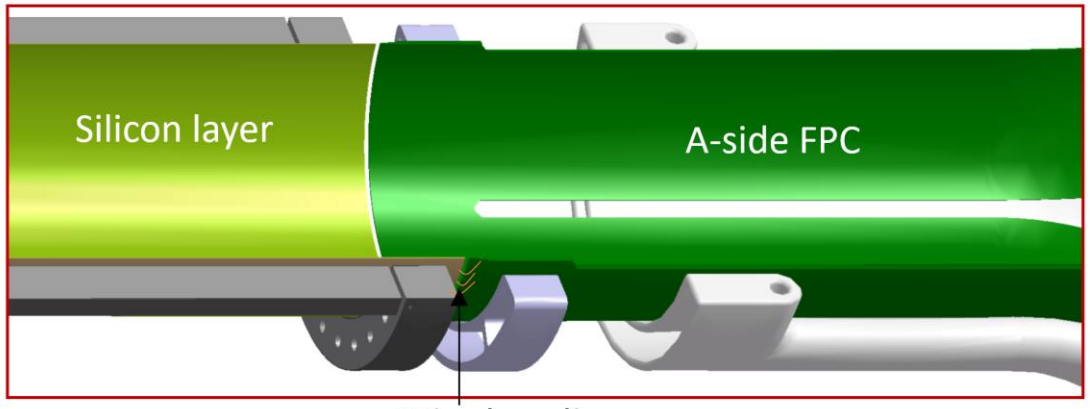
ITS-3 Design



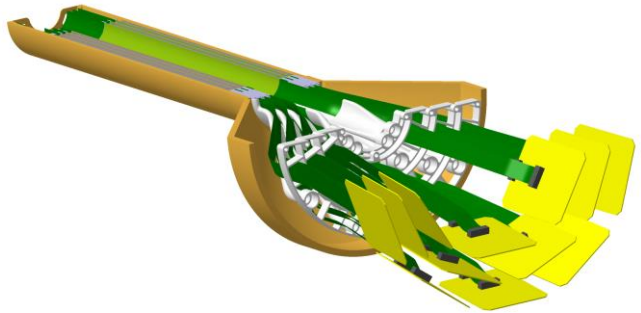


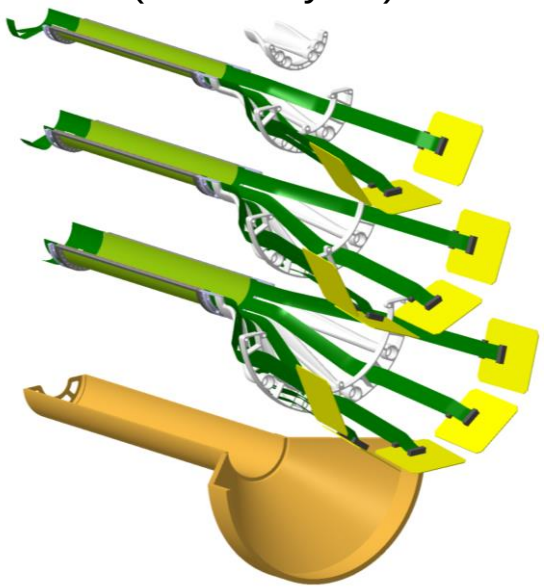
Half layer

Front end electronics
(cooled with a few water-cooling lines of the present ITS2)



Half detector
(3 Half-layers)





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“MOSAIX” Stitched Sensor (ER2)

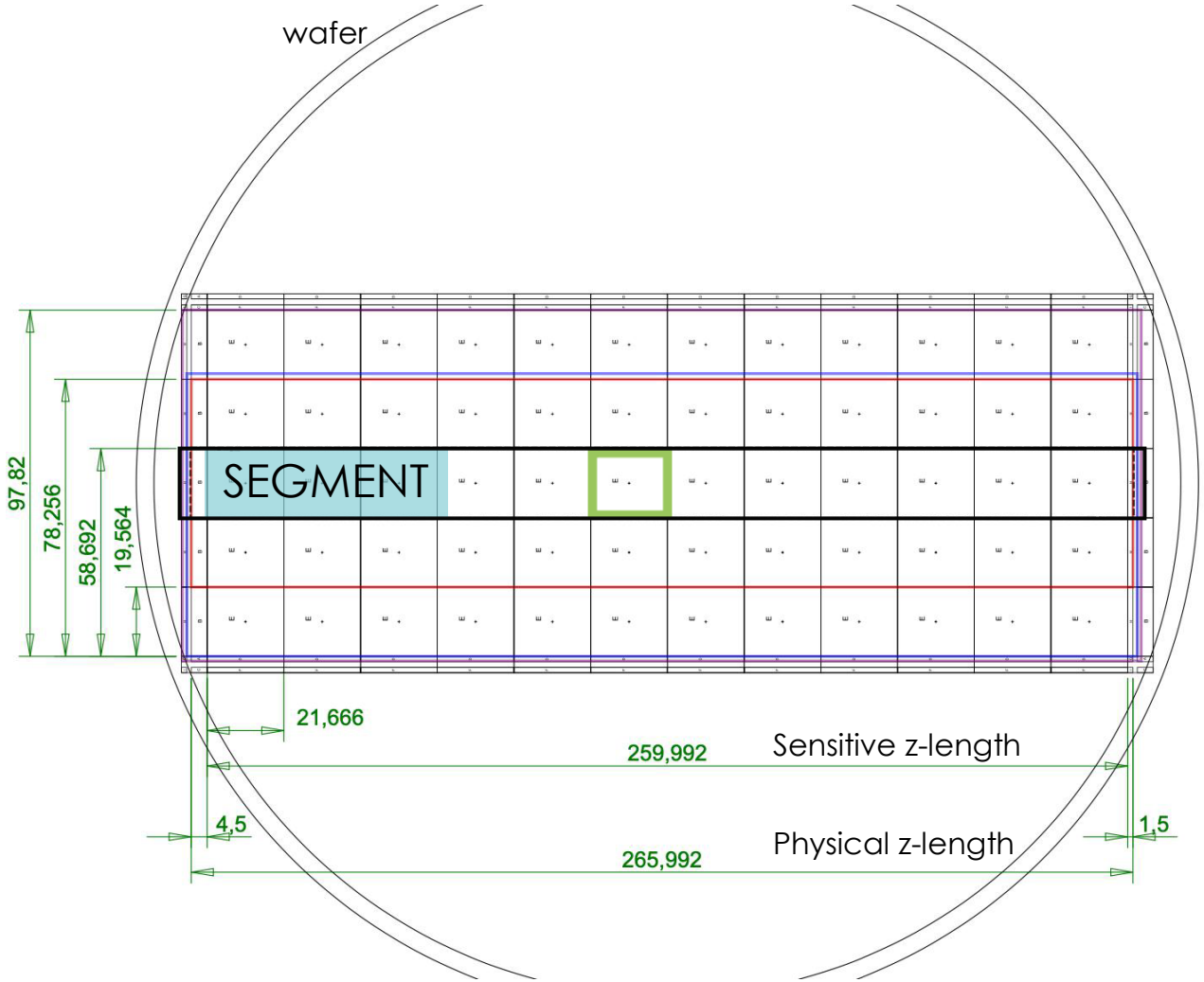
Layer 0: 12 x 3 repeated units+endcaps
Layer 1: 12 x 4 repeated units+endcaps
Layer 2: 12 x 5 repeated units+endcaps

Repeated (Stitched) Sensing Unit (RSU)

ITS-3

IB Layer Parameters	Layer 0	Layer 1	Layer 2
Sensor length [mm]		265.992	
Sensitive length [mm]		259.992	
Sensor azimuthal width [mm]	58.692	78.256	97.820
Radial position [mm]	19.0	25.2	31.5
Equatorial gap [mm]		1.0	

Table 3.2: Design dimensions of the sensor dies and radial position.



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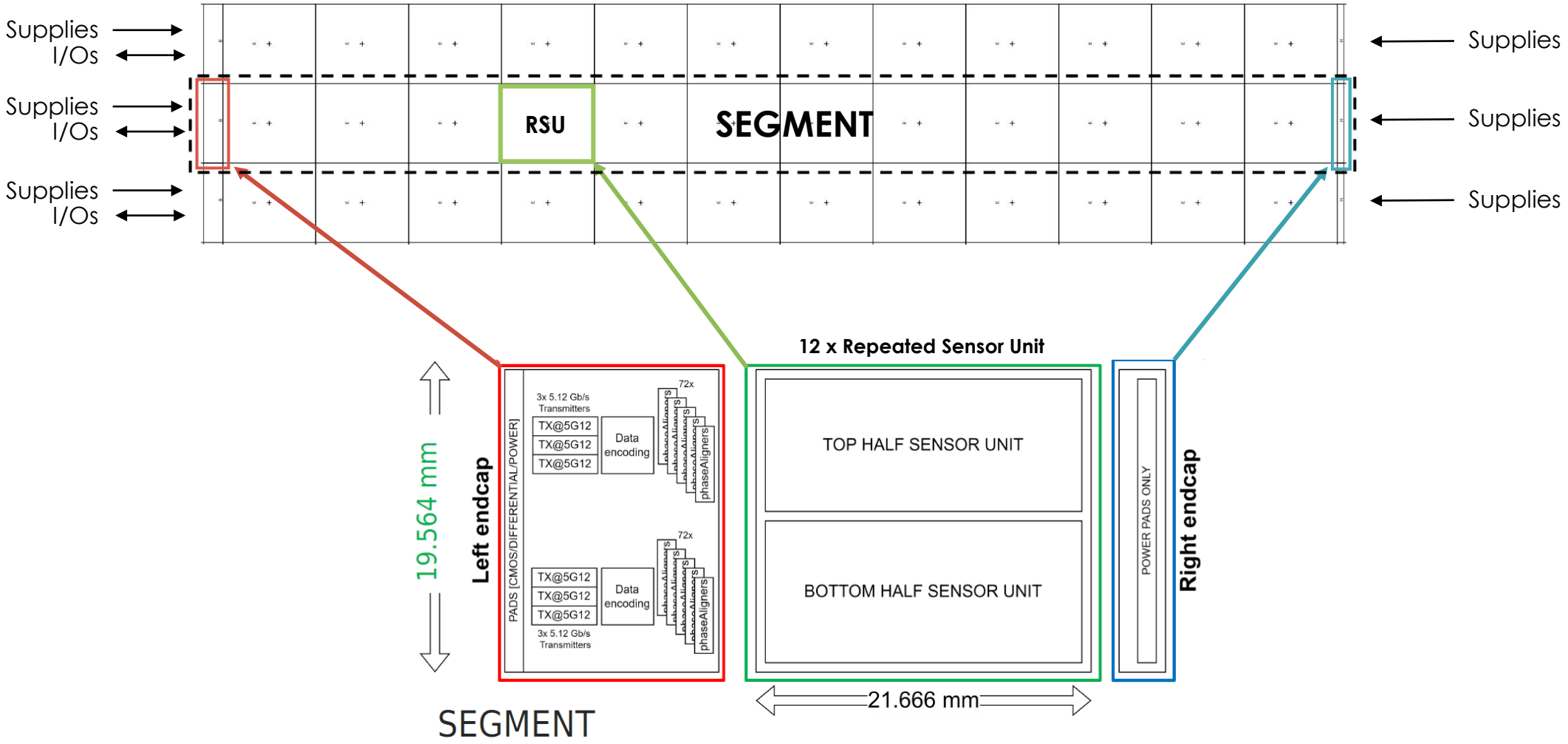
MOSAIX Stitched Sensor Detail



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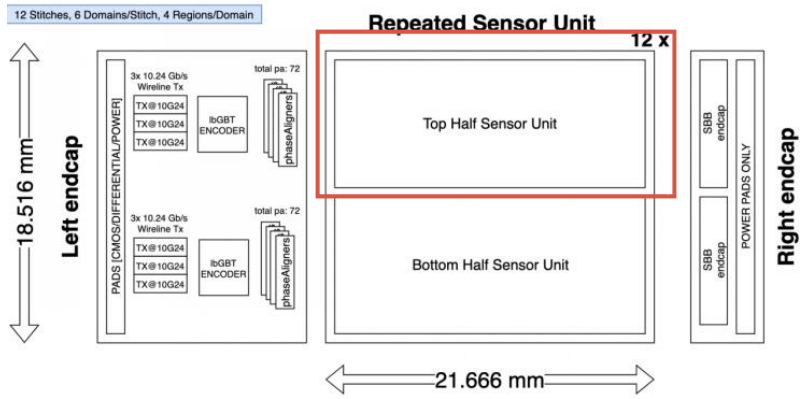
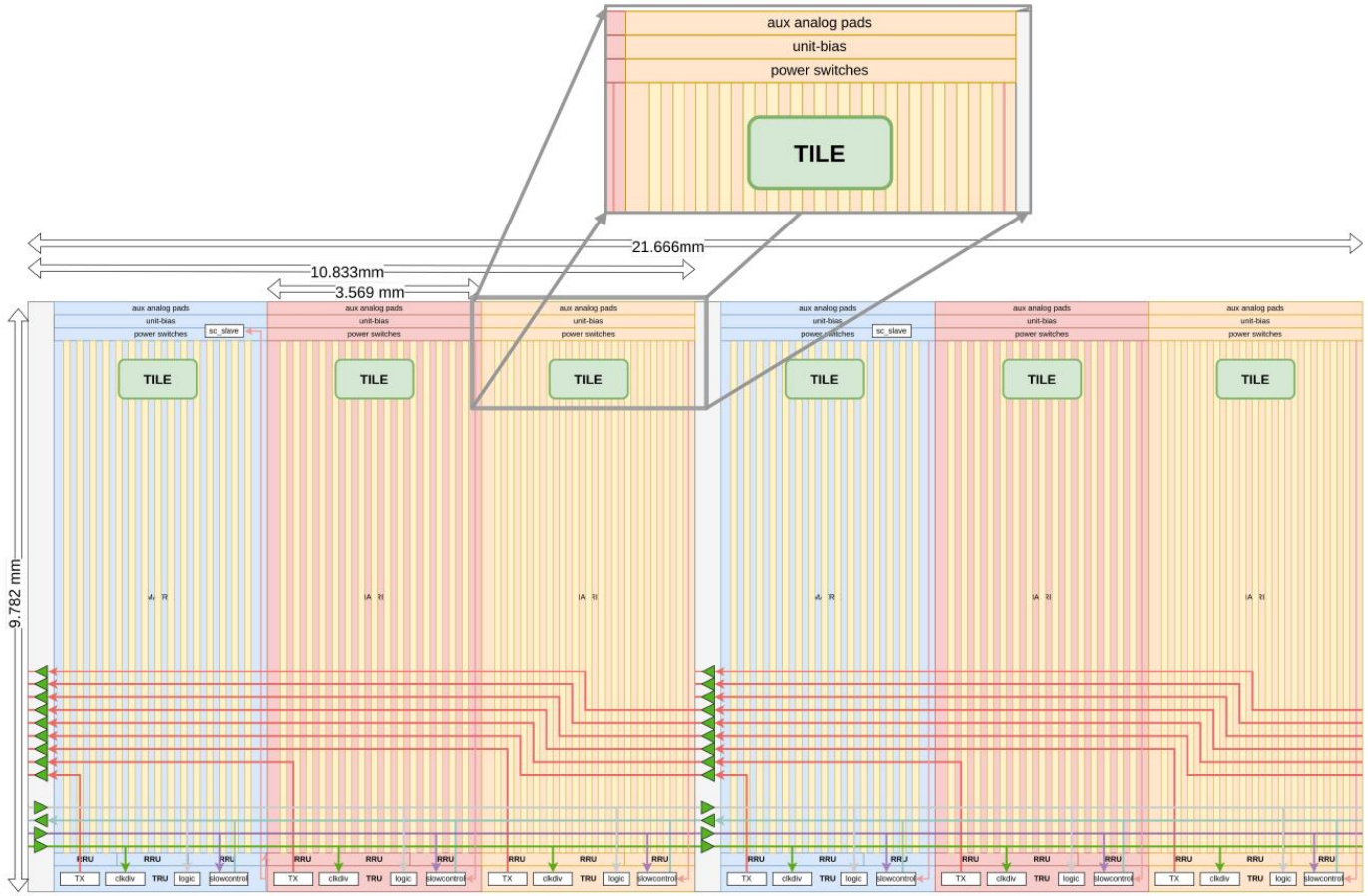
Half Repeated Sensor Unit

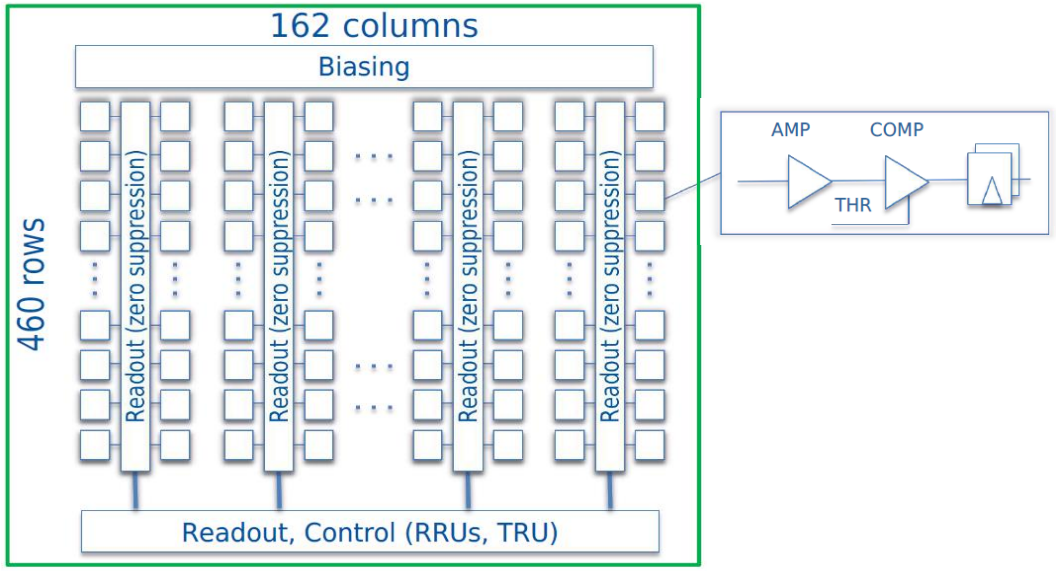




Each Half Unit is segmented in **Tiles** (Domains)

Each **tile** acts as an
independent sensor
Separate Local Power
Configuration
Readout Link (160 Mb/s)
Each **Tile** data output has
direct connection to the **left endcap**

Domain Architecture



20.8 mm x 22.8 mm pixel pitch(*)
Continuously active front-end (40 nW typ.)
Global shutter
Zero-suppressed matrix readout
Continuous readout mode
Integration time: 2 / 5 / 10µs

(*) **Baseline: 20.8 mm * 22.8 mm**
Abs. Max: 22.5 mm * 25 mm

In pixel:

- Amplification
- Discrimination
- Hit integration register and readout register
- Test charge injection
- **Digital pulsing**
- Masking

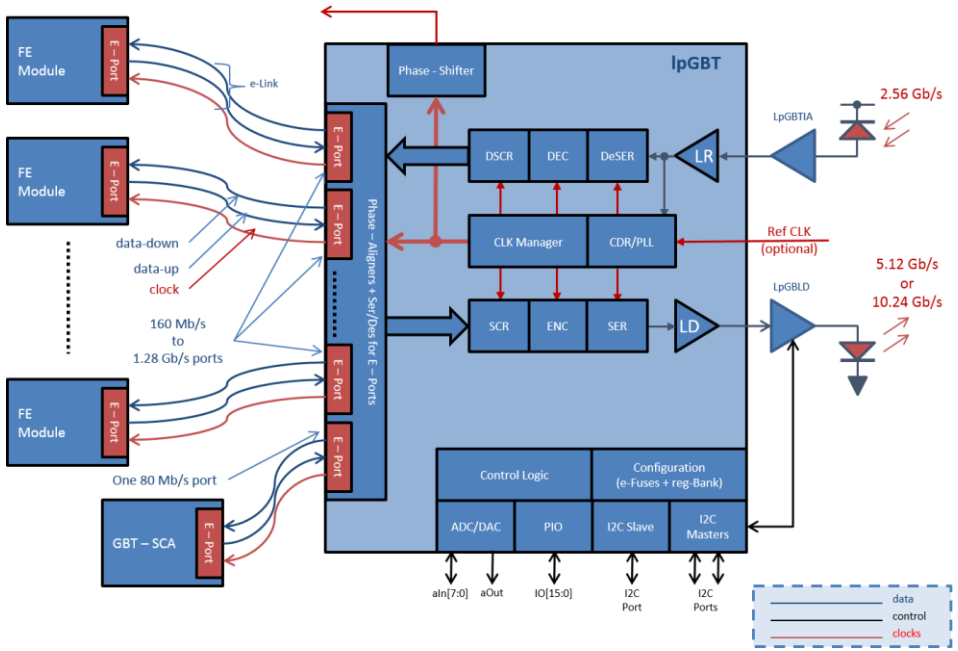
Digital pixel designed with low-leakage, high reliability std cells

460 x 162 pixels / domain
894,200 pixels per RSU
144 domains / segment
10.73 Mpixels / segment

Left Endcap: Use **lpGBT** for Data Transmission

Communicates with

- The counting room
  - Optical fibre links
- The FE modules / ASICs
  - Electrical links (eLinks)
- The Number and Bandwidth of eLinks is programmable
- For Down eLinks
  - Bandwidth: 80/160/320 Mbps
  - Count: 16/8/4
- For Up eLinks



Input eLinks (uplink)												
uplink bandwidth [Gbps]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mbps]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

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lpGBT Data Format

Uplink Format (5.12 or 10.24 Gbps)

- **5.12Gbps / FEC5**:
  - **Header(2bit)**: Used by the lpGBT to align the frame.
  - **Slow control (4bit)**: IC (2bit) and EC (2bit).
  - **User bandwith (112bit)**: From lpGBT e-links.
  - **FEC (10bit)**: Can correct up to 5 consecutives errors.

- **5.12Gbps / FEC12**:
  - **Header(2bit)**: Used by the lpGBT to align the frame.
  - **Slow control (4bit)**: IC (2bit) and EC (2bit).
  - **User bandwith (98bit)**: From lpGBT e-links (2bit unconnected).
  - **FEC (24bit)**: Can correct up to 5 consecutives errors.

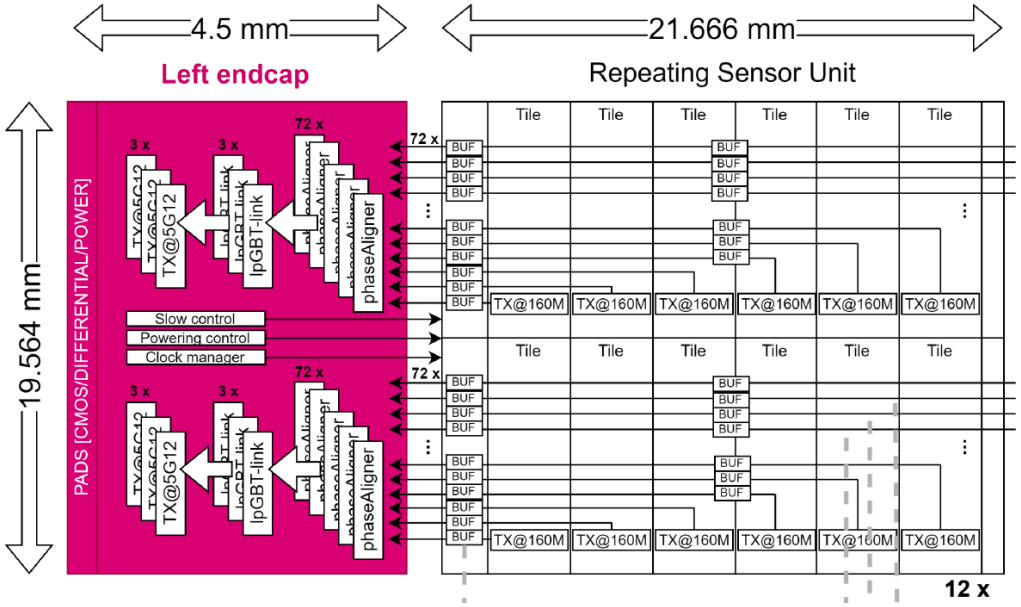
- **10.24Gbps / FEC5**:
  - **Header(2bit)**: Used by the lpGBT to align the frame.
  - **Slow control (4bit)**: IC (2bit) and EC (2bit).
  - **User bandwith (230bit)**: From lpGBT e-links (6bit unconnected).
  - **FEC (20bit)**: Can correct up to 5 consecutives errors.

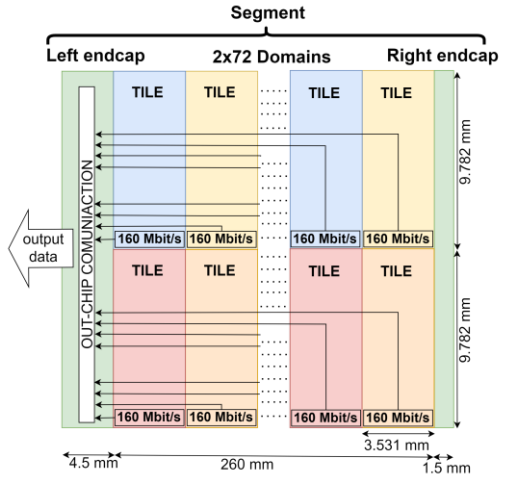
- **10.24Gbps / FEC12**:
  - **Header(2bit)**: Used by the lpGBT to align the frame.
  - **Slow control (4bit)**: IC (2bit) and EC (2bit).
  - **User bandwith (202bit)**: From lpGBT e-links (10bit unconnected).
  - **FEC (48bit)**: Can correct up to 5 consecutives errors.

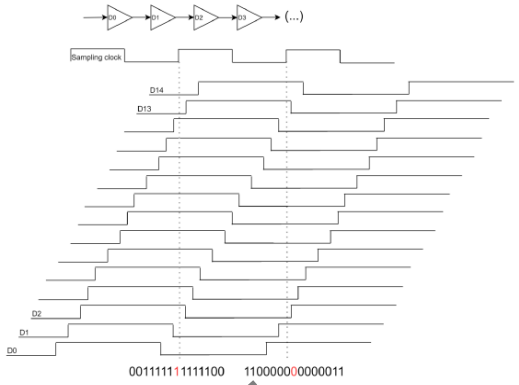
Downlink Format (2.56 Gbps)

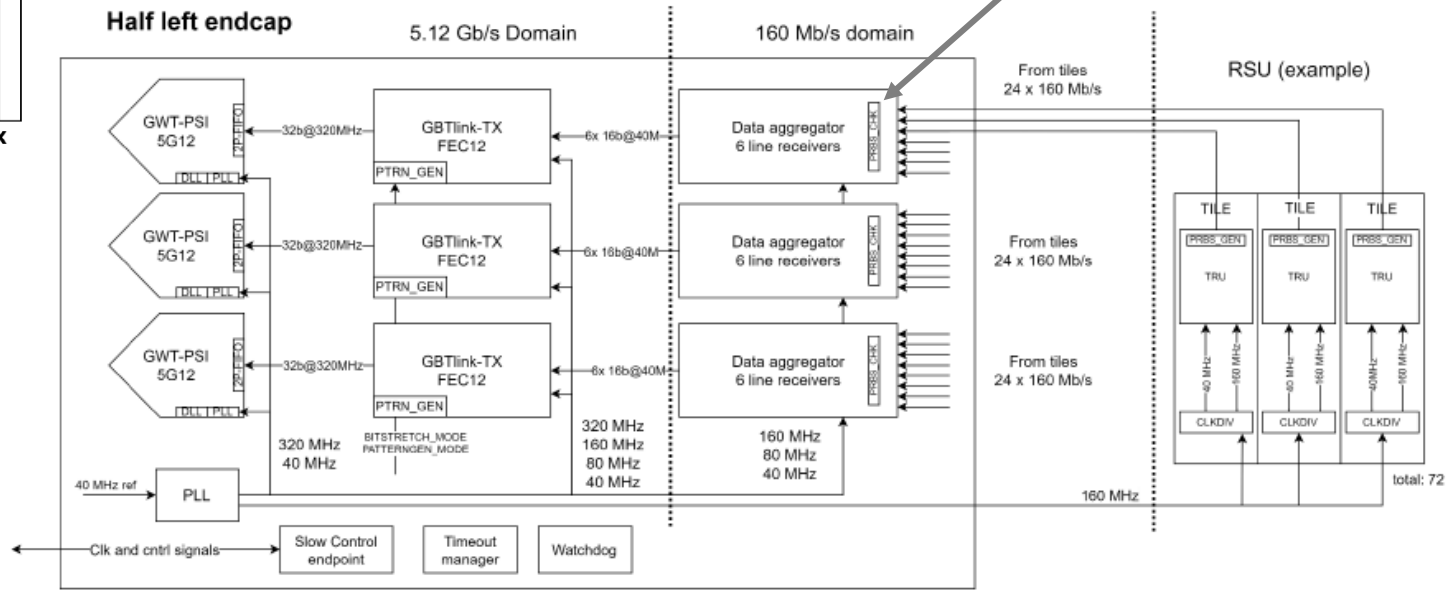
- **Header (4bit)**: Used by the lpGBT to align the frame.
- **User data (32bit)**: sent to lpGBT e-links.
- **EC (2bit)**: used for the external slow control (e.g.: GBT-SCA).
- **IC (2bit)**: used for the internal slow control of the lpGBT (register configuration).
- **FEC (24bit)**: used to recover from transmission error (can correct up to 12 consecutives errors).

Data Flow – From Tiles to Left Endcap









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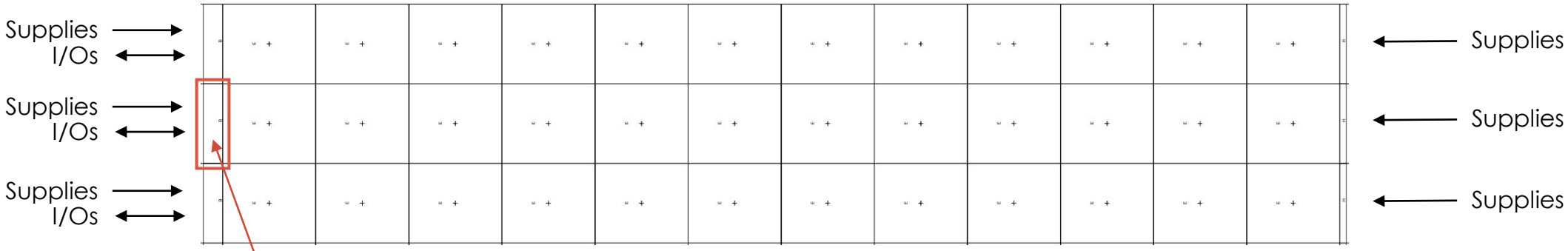
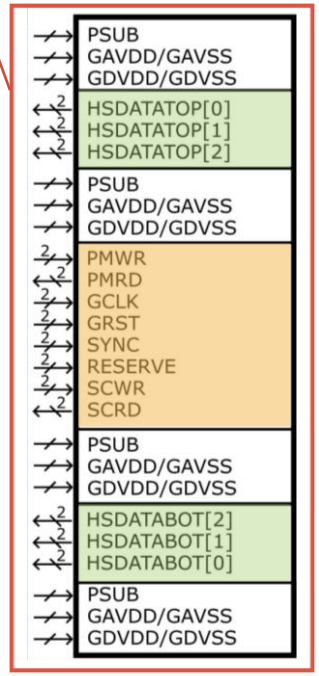
Supplies and I/Os





All I/Os are differential

6x 5.12 Gb/s data outputs

1x clock at 320 MHz

2x slow control at 2.5 Mbps

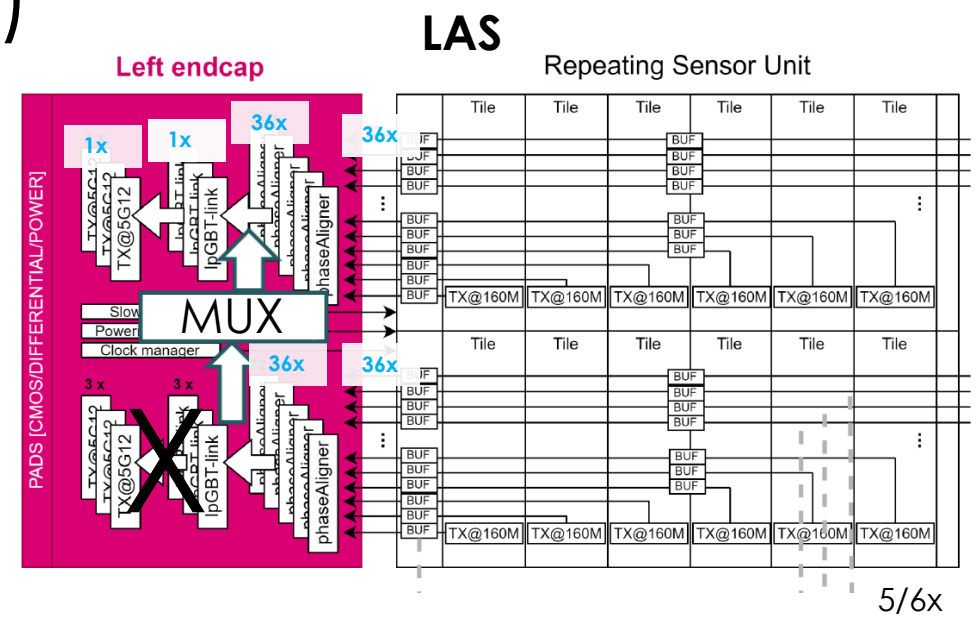
Global analog and digital supplies per *segment*

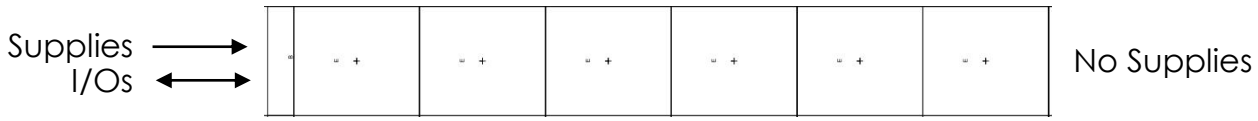
On-chip supply segmentation and control

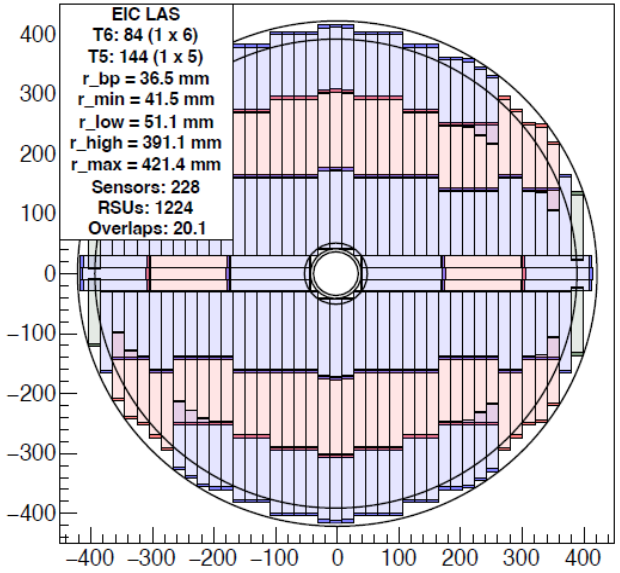
Reverse biasing of substrate (PSUB)

ePIC SVT: "Large Area Sensor" (LAS)

- **Inner Barrel** (Layers 0,1,2) will reuse ITS3-like sensors as is
  - **Layer 0:** 4 sensors in r-phi, 3 segments of 12 RSU
  - **Layer 1:** 4 sensors in r-phi, 4 segments of 12 RSU
  - **Layer 2:** 8 sensors in r-phi, 5 segments of 12 RSU
- EIC **variant** for the **Outer Barrel** (Layers 3,4) and **Endcap Disks**
  - "Large Area Sensor" (LAS)
  - Will be stitched, but not to wafer scale
  - Likely 1 Segment of 5 or 6 RSU (no need for right endcap)
  - Hope is to multiplex Domain data lines to 1 High-Speed output
  - More conventional carbon composite mechanical support with integrated cooling







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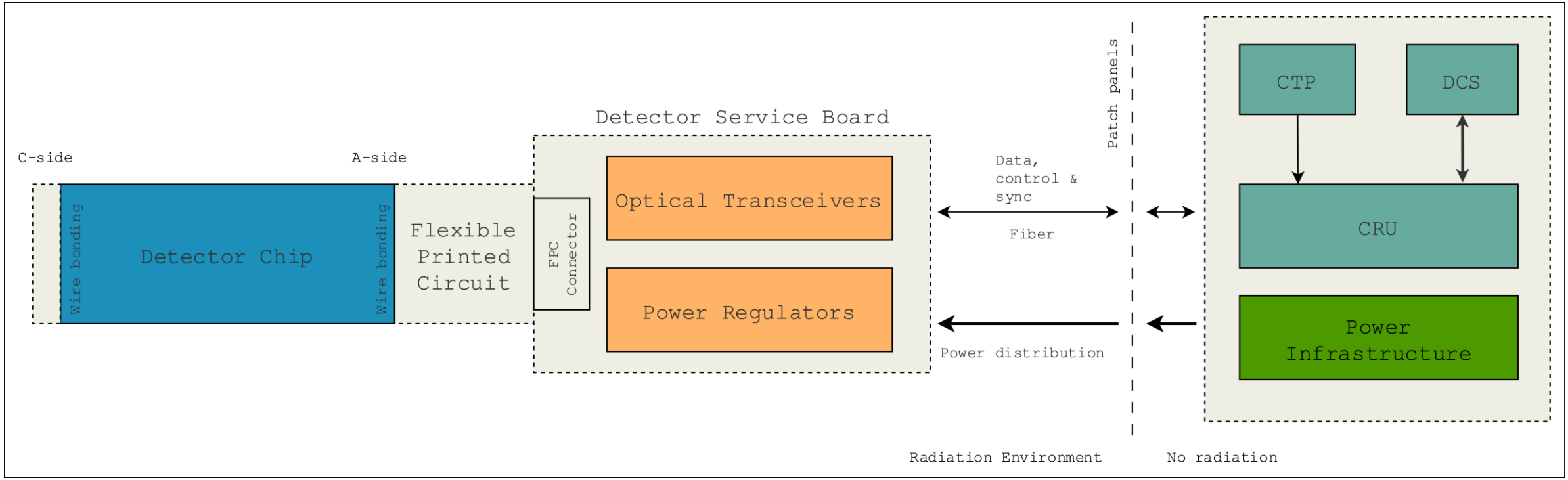
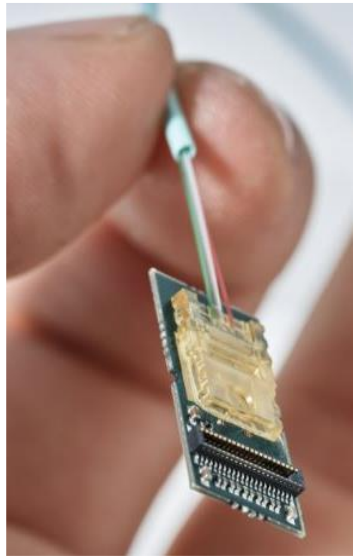
SVT by the Numbers

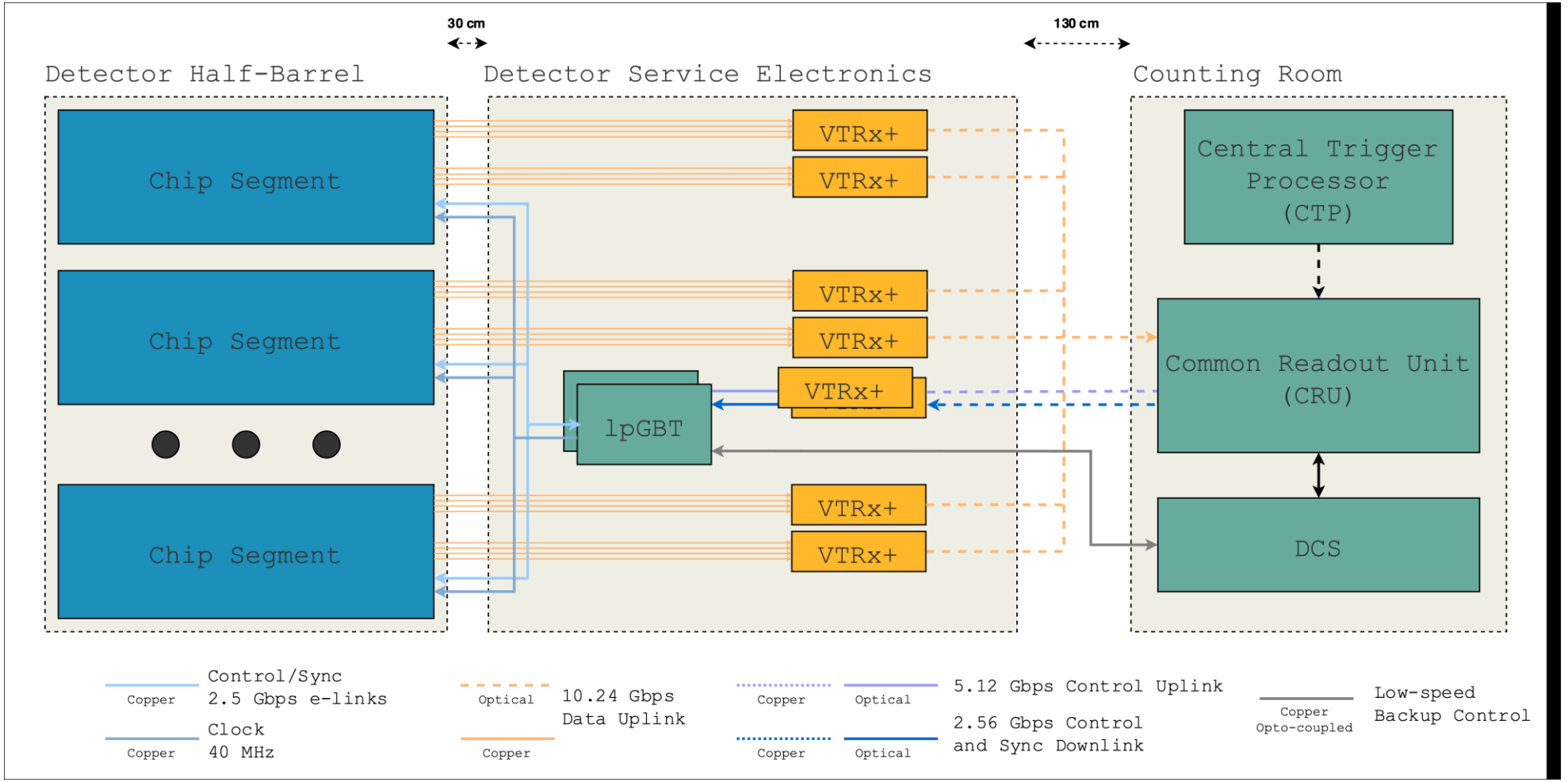
	width (mm)	length (mm)		# pixels per reticle								
RSU size	19.564	21.666		894,240								
Pixel size	0.0200	0.0225										
Barrel					Sensor							
Layer Index	**radius (mm)**	**z (mm)**		**Area (mm^2)**	**RSUs in width**	**RSUs in length**	**# of sensors in r-phi**	**# of sensors in z**	**# pixels**	**# sensors**	**Notes**	**# Readout Links**
0	36	270		61,073	3	12	4	1	128,770,560	4	bent ITS3	72
1	48	270		81,430	4	12	4	1	171,694,080	4	bent ITS3	96
2	120	270		203,575	5	12	8	1	429,235,200	8	bent ITS3	240
3	270	540		916,088	1	5	87	5	1,944,972,000	435	1x5 LAS	435
4	420	840		2,216,706	1	5	135	8	4,828,896,000	1080	1x5 LAS	1080
e-endcap												
Disk index	**z (mm)**	**inner r (mm)**	**outer r (mm)**									
1	-250	36.76	240	176,710	1	5			375,580,800	84	1x5 LAS	84
2	-450	36.76	415	536,815	1	5			1,135,684,800	254	1x5 LAS	254
3	-650	36.76	421.4	553,632	1	5			1,171,454,400	262	1x5 LAS	262
4	-900	40.0614	421.4	552,835	1	5			1,166,983,200	261	1x5 LAS	261
5	-1150	46.3529	421.4	551,127	1	5			1,166,983,200	261	1x5 LAS	261
h-endcap												
Disk index												
1	250	36.76	240	176,710	1	5			375,580,800	84	1x5 LAS	84
2	450	36.76	415	536,815	1	5			1,135,684,800	254	1x5 LAS	254
3	700	38.52	421.4	553,216	1	5			1,171,454,400	262	1x5 LAS	262
4	1000	53.43	421.4	548,909	1	5			1,158,040,800	259	1x5 LAS	259
5	1350	70.14	421.4	542,422	1	5			1,144,627,200	256	1x5 LAS	256
TOTAL				**8,208,062**					**17,505,642,240**	**3768**		**4160**

Off Detector Electronics – Simplified Overview



Detector Electronics – Data & Control





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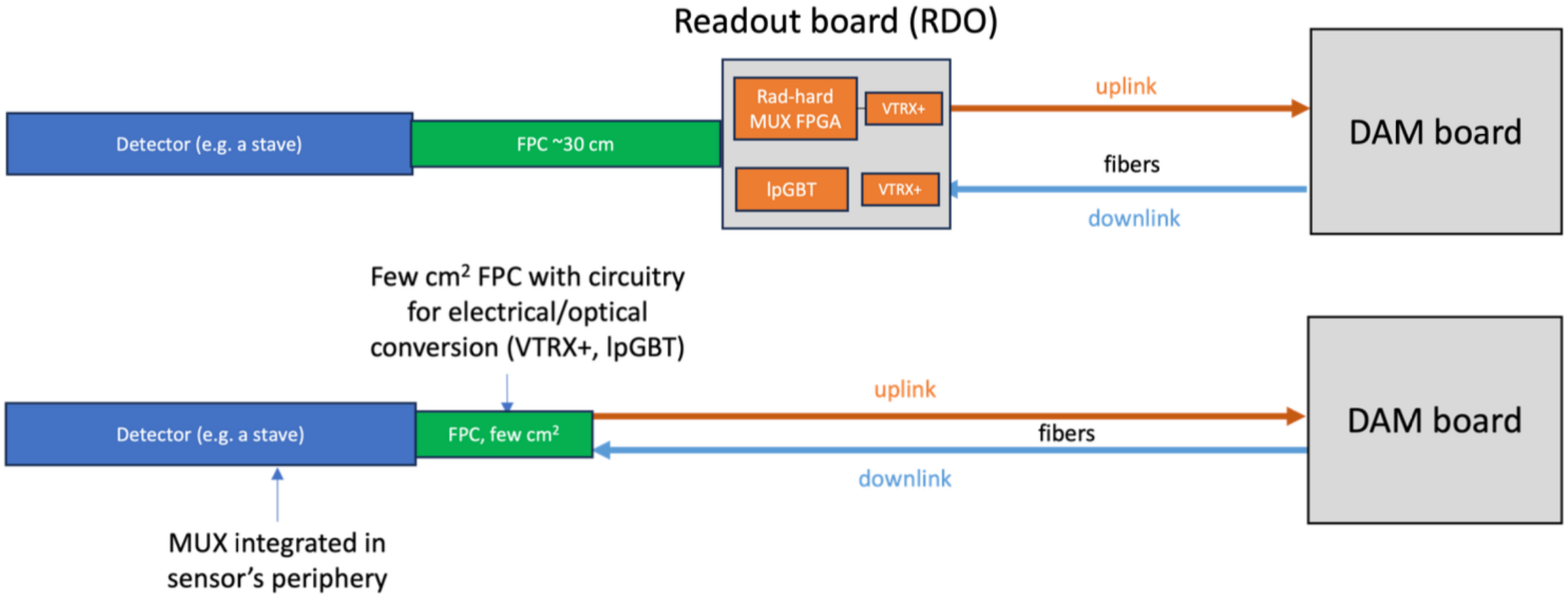
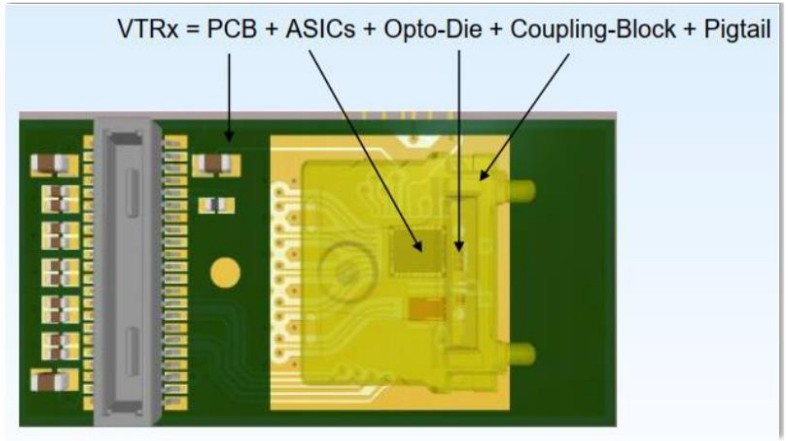
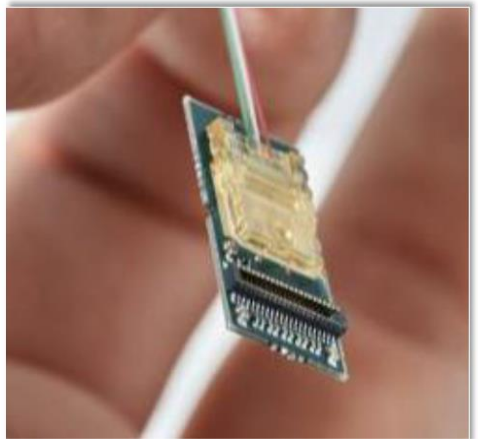
SVT Readout (inspired by ITS3 Readout)

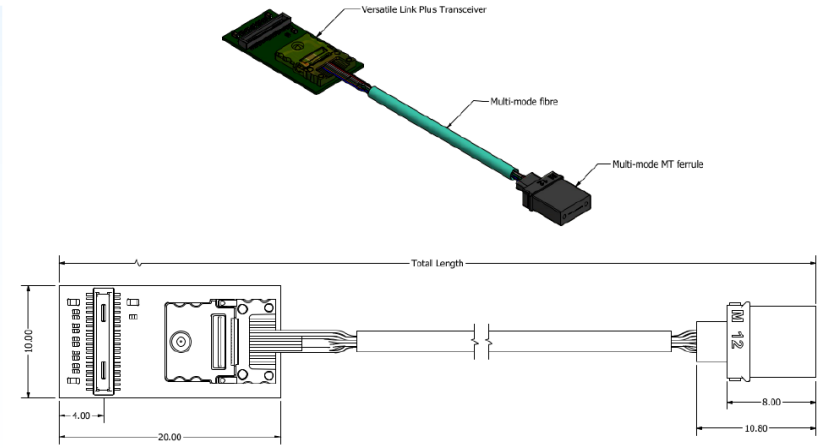


VTRx+ Front-end Module

- **Versatile**
  - Up to 4 Tx + 1 Rx, configurable by masking channels
- **Miniaturised**
  - 20 x 10 x 2.5 mm
- **Pluggable**
  - Electrical connector
- **Data-rate**
  - Tx: up to 4×10 Gb/s, Rx: 2.5 Gb/s
- **Environment**
  - Temperature: -35 to + 60 °C
  - Total Dose: 100 Mrad
  - Total Fluence: $1x10^{15}$ n/cm^2 and $1x10^{15}$ hadrons/cm^2
- **Status**
  - Pre-production ongoing
  - Solving problems with module assembly
    - Alignment of optical components
  - Ramping up to 2k modules/month in 2023







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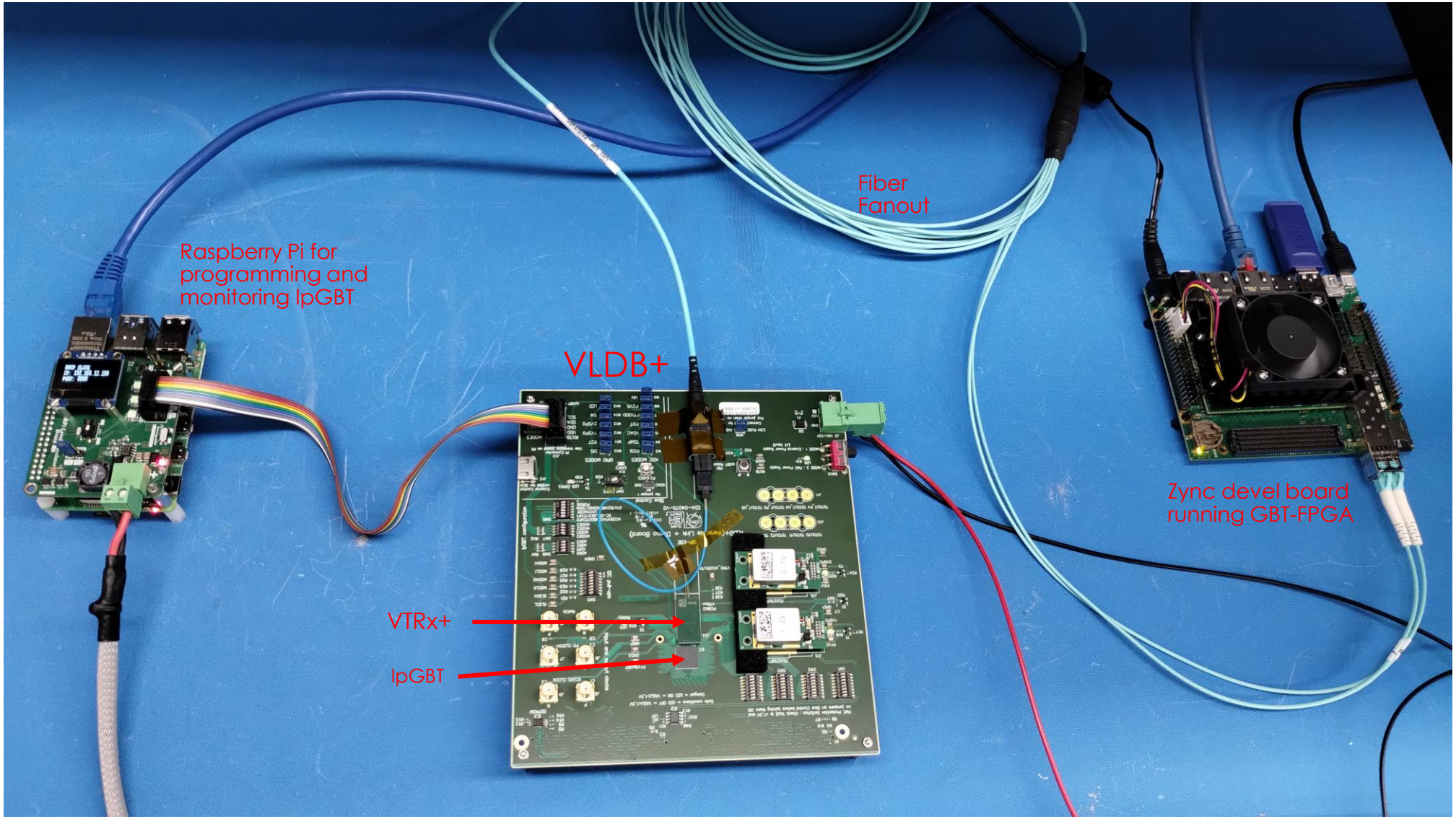
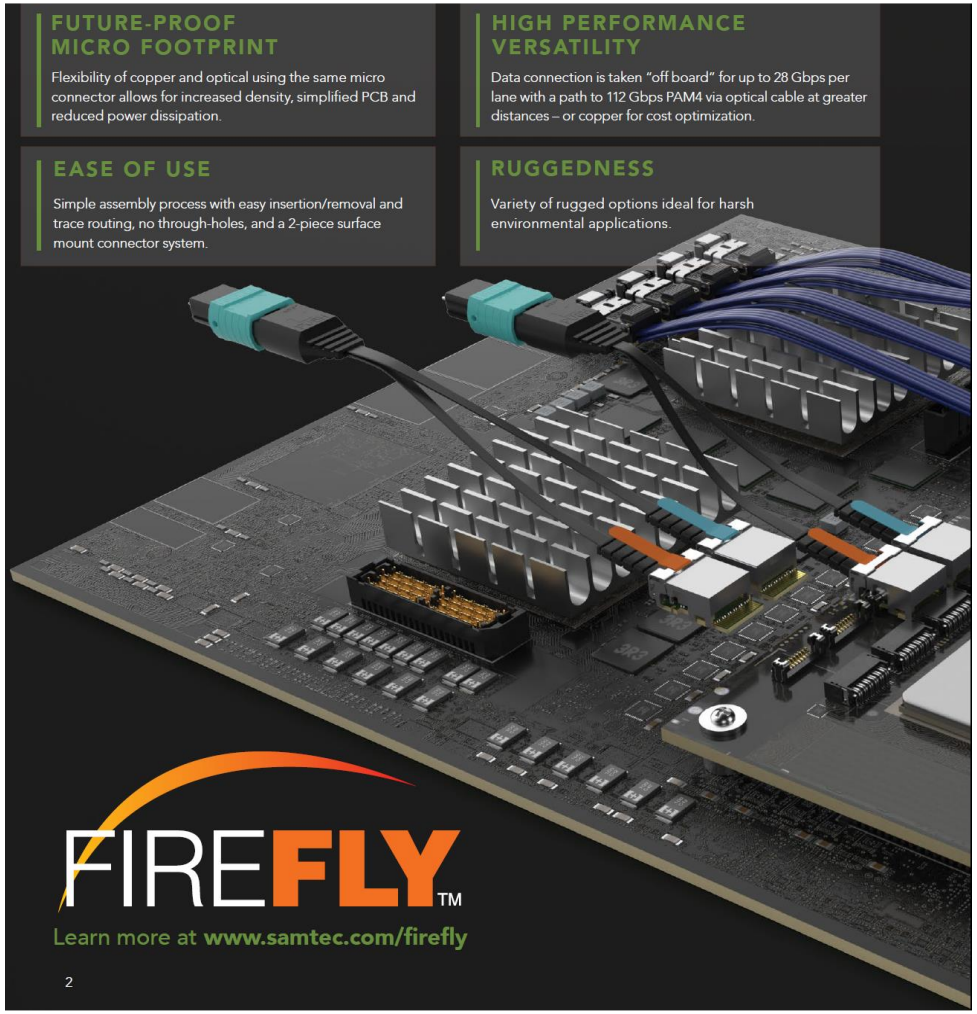
VLDB+ Test Setup at ORNL



High-Speed Interconnect Alternative



Data connection is taken "off board," simplifying board layout and enhancing signal integrity from IC to faceplate

- Up to 28 Gbps per channel via optical cable for greater reach
- Industry leading miniature footprint allows for higher density close to the data source
- Simple to use system with easy insertion/removal and trace routing, no through-holes, and a surface mount connector system
- Supports data center, HPC and FPGA protocols, including 10/40/100 GbE Ethernet, InfiniBand™, Fibre Channel and Aurora

14 Gbps	x4 x12	25 Gbps	x4 x12
16 Gbps	x12	28 Gbps	x4

ECUO	WIDTH	DATA RATE	CABLE LENGTH	0	HEAT SINK	1	FIBER TYPE	END 2 OPTIONS*
	–B04 = 4 Tx + 4 Rx **–T12** = 12 Tx **–R12** = 12 Rx **–Y12** = 12 Tx + 12 Rx **–U12** = 12 Channel AOC (Unidirectional)	**–14** = 14 Gbps per lane **–16** = 16.1 Gbps per lane (N/A –B04) **–25** = 25.7 Gbps per lane **–28** = 28.1 Gbps per lane (–B04 only)	**–"XXX"** = Overall Length in Centimeters		**–1**= Flat **–2** = Pin-fin (–14 & –16 only) **–3** = Flat with groove **–4** = PCIe® Pin-fin (–14 & –16 only) **–5** = 1.75 cm tall Pin-fin (–B04 only)		**–4** = Aqua loose tube with Boot **–5** = Jacketed ribbon with boot **–6** = Jacketed ribbon **–7** = Black loose tube with boot **–8** = Black loose tube	-Y12 requires -2X end option (Leave blank for -U12) **12 Fibers** **–01** = MTP® Male **–02** = MTP® Female **–07** = MXC® Internal Plug **–0E** = MPO Plus®, Male, bayonet **24 Fibers** **–21** = MTP® Male **–22** = MTP® Female **–27** = MXC® Internal Plug **–2E** = MPO Plus®, Male, bayonet

* These are standard options. See page 5 for other end options available.

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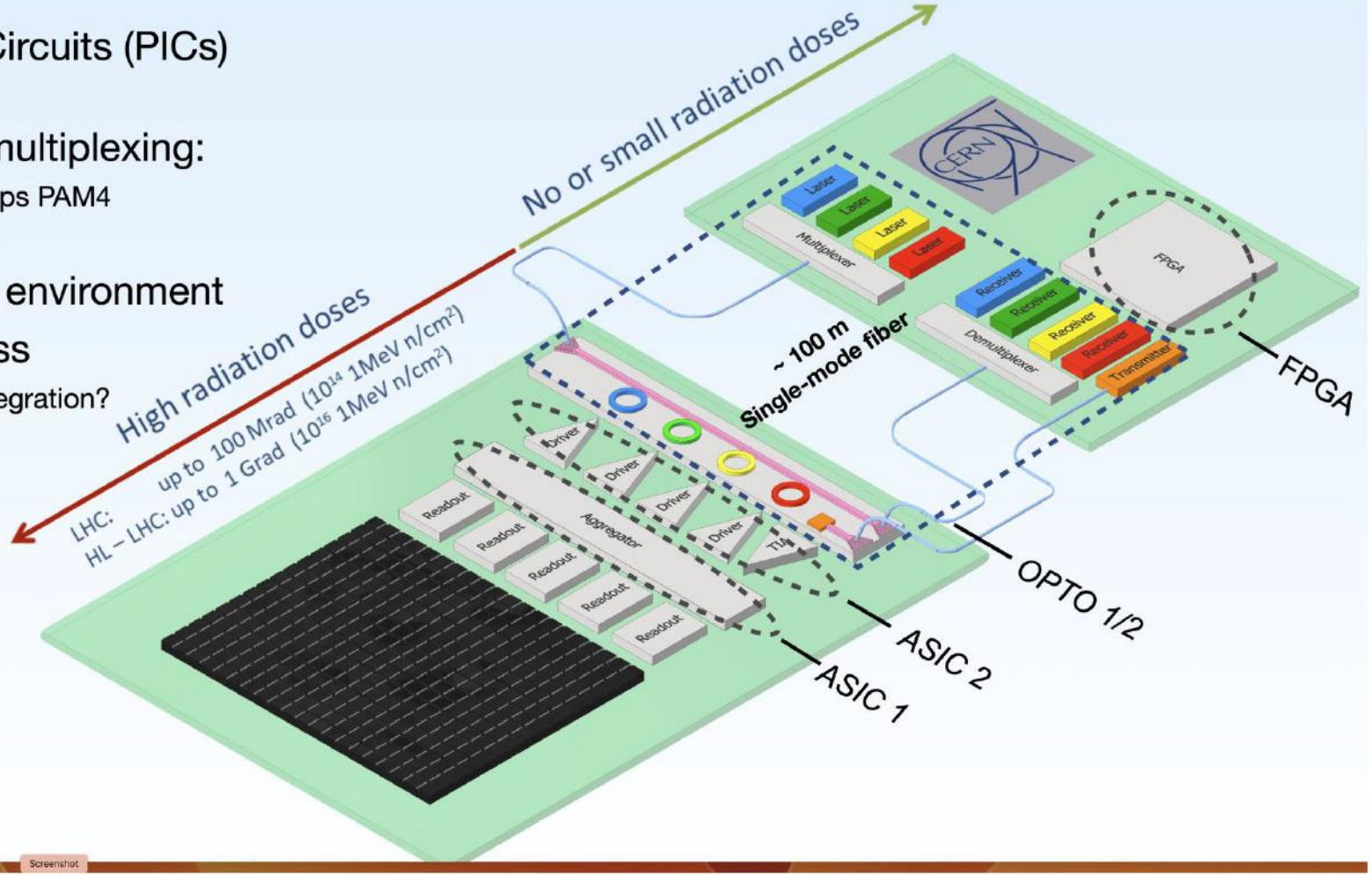
Future Developments: CERN EP RD WP6

WP6 Project breakdown

EP-ESE
Electronic Systems for Experiments

- Photonic Integrated Circuits (PICs)
  - RadHard "promise"
- Wavelength division multiplexing:
  - Lane: 25 Gbps NRZ / 50 Gbps PAM4
  - Fibre: 100 Gbps / 200 Gbps
- Laser out of radiation environment
- Low power / Low mass
  - How far can we push FE integration?



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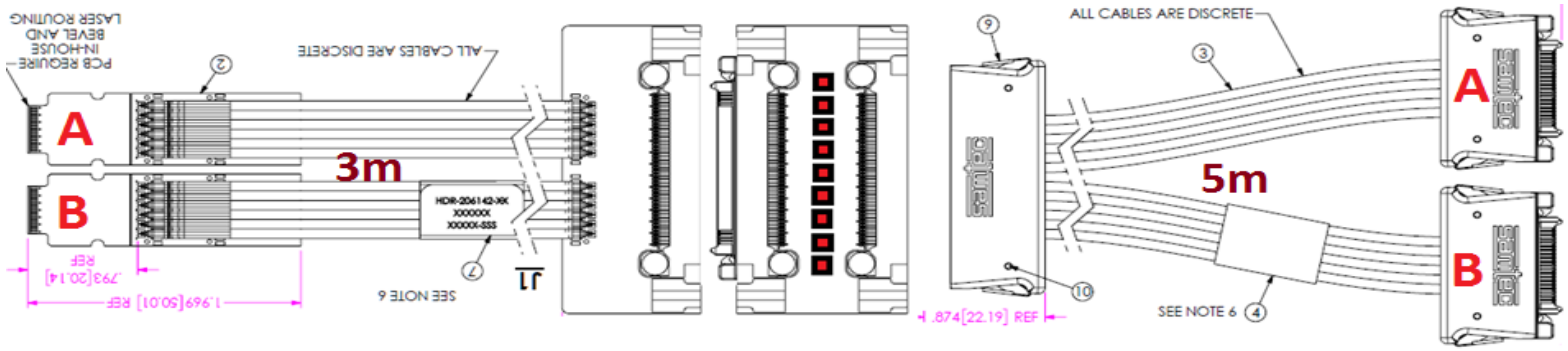
Radiation Tolerant FPGA: Microchip PolarFire

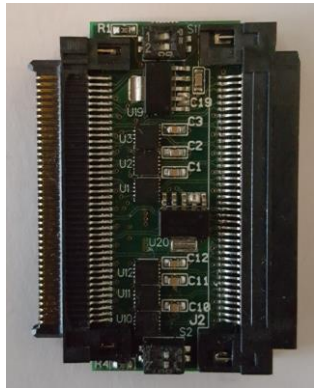
		MPF050	MPF100	MPF200	MPF300	MPF500
FPGA Fabric	Logic Elements (4LUT + DFF)	48K	109K	192K	300K	481K
	Math Blocks (18 × 18 MACC)	150	336	588	924	1480
	LSRAM Blocks (20 Kb)	160	352	616)	952	1520
	uSRAM Blocks (64 × 12)	450	1008	1764	2772	4440
	Total RAM (Mb)	3.6	7.6	13.3	20.6	33
	uPROM (Kb)	216	297	297	459	513
	User DLLs/PLLs	8	8 each	8 each	8 each	8 each
High-Speed I/O	250 Mbps–12.7 Gbps Transceiver Lanes	4	8	16	16	24
	PCIe® Gen 2 Endpoints/Root Ports	2	2	2	2	2
Total I/O	Total User I/O	176	296	364	512	584

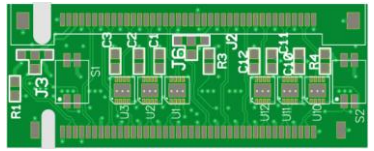
Alternative: Cable with Re-transmit Buffer

* Courtesy: M. Rossevij, Utrecht University



layers: 4
Size Bare PCB: 45 x 19 mm
Eurocircuits: technologieklasse=6C, controlled impedance





18 Buffers: DS25BR100

Tested in panda to 5 kGy with 30 Mev protons

https://indico.gsi.de/event/6943/contributions/31378/attachments/22501/28250/Motzko.pdf

2 x Local Regulator: TL1963A

1,5A, max 340mV drop

Tested by Caterina Deplano for radiation

https://indico.nikhef.nl/event/2270/contribution/0/material/slides/1.docx

Buffers are DC coupled (might need AC coupling in future)
Proto has 9 DS25BR100 (driver)+9 DS25BR120 (transceiver)

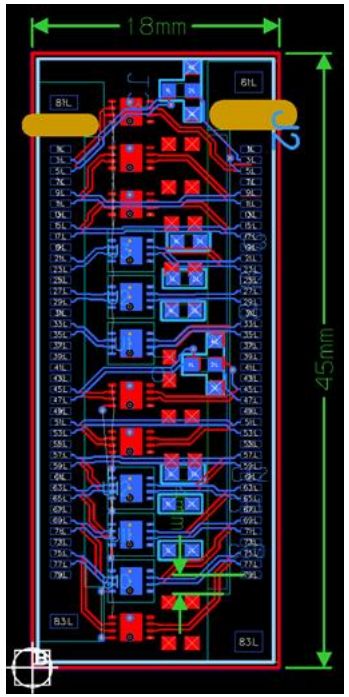
Buffer	DFE	Rate
No	Off	<2 Gbps
	On	2.5 Gbps
Yes	Off	>3.125 Gbps (6.25 Gbps)
	On	

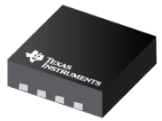
OAK RIDGE National Laboratory

Repeater Board

Numbers on the repeater board
- 12(bot) + 6(top) Buffers (DS25BRxx0)
- Power: 2 Watt (18*115mW) (1W/ITS2-stave)
- Current: 630 mA (18*35mA)
- 4-layer PCB
- 18 x 45 mm

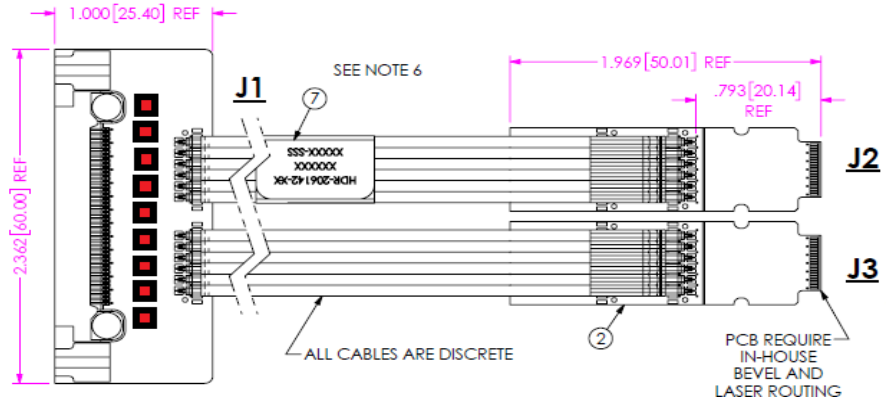
Open issues
- Check space envelope
- Check thermal envelope
  - for ITS3 only IB is upgraded, corresponds to 48 ITS2 staves (≈50W total)
- Power delivery (next slide)
- AC coupling
  - ITS2: staves are decoupled from RU by AC coupling on transitionboard
  - Proposal: For now, no AC coupling on repeater-board proto-type





Transceiver Integration Option

3.125Gbps 3,3V	#links	Current (mA)	Power (mW)	Size (mm²)	Price
DS25BR100	1	35 (35)	115 (115)	3x3 (9)	$2 (2)
DS25CP102	2	77 (38)	254 (127)	4x4 (8)	$4 (2)
DS25BR440	4	162 (40)	534 (133)	6x6 (9)	$4 (1)



DS25BR100 Tested in panda to 5 kGy with 30 Mev protons:
https://indico.gsi.de/event/6943/contributions/31378/attachments/22501/28250/Motzko.pdf