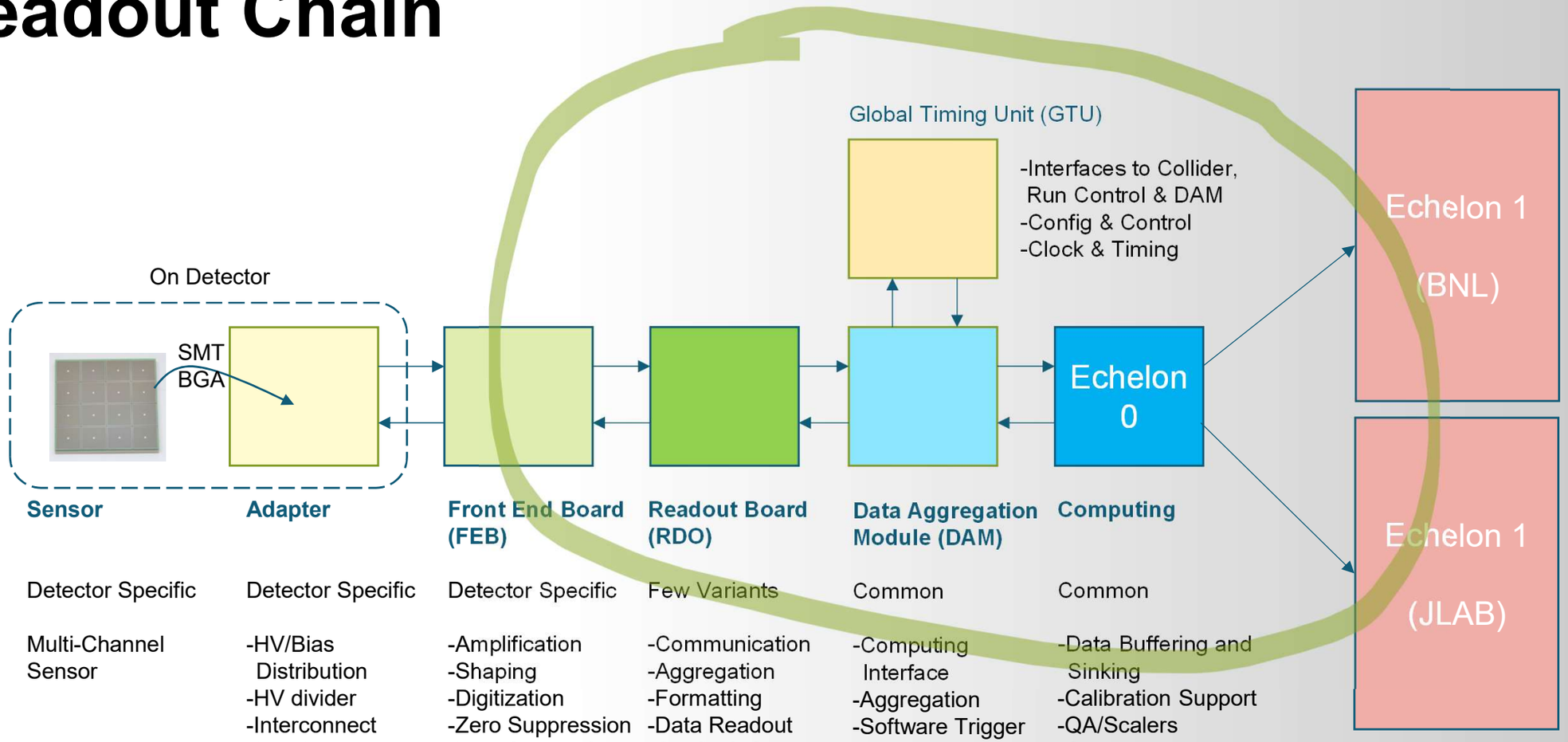
Data Rates and Data Reduction Requirements

- Goals of ePIC DAQ
  - “zero” global deadtime
  - “zero” bias readout
    - This means (in decreasing order of importance):
      - Include all possible signal (Because we want to analyze all collisions AND because ***we want to have the capability of using the most sophisticated event selection criteria available***)
        - Implies that the reconstruction needs a well-organized event selection & labelling step before analyzing data
      - Include background (***Because some apparent background may be signal*** AND because ***backgrounds affect the detectors in ways that we may be able to correct for, with study*** AND because ***prompt characterization of backgrounds can help the collider give us what we need***)
        - Implies that the reconstruction needs a background elimination step before analyzing clean data
      - Include noise (Because ***we may be able to distinguish signal from noise better than some simple DAQ algorithm, with study***)
        - Implies that the reconstruction need a noise elimination step before reconstructing cleanest possible data
- Subject to reality
  - Potential electronics limitations
    - ASIC / FEB digitization and serialization limits
    - RDO limitations (~10Gb/sec per RDO)
  - Data volume limitations (~100Gb/sec to compute facilities)
- ePIC DAQ will need technical capabilities for:
  - Software Triggering & Hardware Triggering (Of a sort)
  - Tagging of events (LEDs, pedestal calculation, charge injections etc)
  - Flow control (application of deadtime to ensure data coherency needs)
  - Prescaling (application of arbitrary deadtimes for some subset of detectors)

ePIC Readout Chain

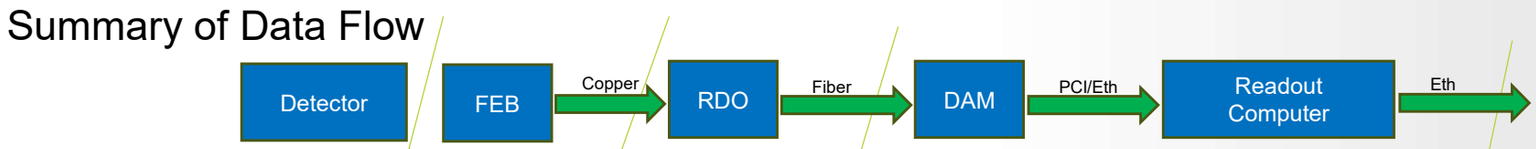


Name	Sensor	Adapter	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Design	Detector Specific	Detector Specific	Detector Specific	Few Variants	Common	Common
Function	Multi-Channel Sensor	-HV/Bias Distribution -HV divider -Interconnect Routing	-Amplification -Shaping -Digitization -Zero Suppression -Bias Control & Monitoring	-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock & Timing	-Computing Interface -Aggregation -Software Trigger -Config & Control -Clock & Timing	-Data Buffering and Sinking -Calibration Support -QA/Scalers -Collider Feedback -Event ID/Building -Software Trigger -Monitoring
Attributes	MAPS, AC-LGAD MPGD, MCP-PMT SiPM, LAPPD	-Sensor Specific -Passive	-ASIC/ADC -Discrete -Serial Link	-FPGA -Fiber Link	-Large FPGA -PCIe -Ethernet	-COTS -Ethernet

Summary of Channel Counts and Data Flow

Detector Group	Channels					RDO	Fiber (single)	DAM	Data Volume (RDO) (Gb/s)	Data Volume (To Tape) (Gb/s)
	MAPS	AC-LGAD	SiPM/PMT	MPGD	HRPPD/ MCP-PMT					
Tracking (MAPS)	16B					n/a	3158	35	26	26
Tracking (MPGD)				202k		118	236	5	1	1
Calorimeters	500M		104k			451	902	14	502 →	28
Far Forward		1.4M	253k			247	624	10	15	8
Far Backward	66M	60k	2k			38	518	14	150 →	1
PID (TOF)		7.8M				500	1500	14	31 →	1
PID Cherenkov			320k		140k	1283	2583	32	1275 →	32
TOTAL	16.9B	10.4M	679k	202k	140k	2637	9521	124	2,000	96

Summary of Data Flow



100% Occupancy	27.5-1760 Pb/sec

Aggregate	2.0 Tb/sec
Noise	1.6 Tb /sec
Signal from Physics + Background	400 Gb / sec

Aggregate	2.0 Tb/sec
Per RDO (Avg)	0.7 Gb/sec

Aggregate	96 Gb/sec
Collision Signal	38 Gb/sec
Synchrotron Rad	.01 Gb/sec
Electron Beam	22 Gb/sec
Hadron Beam	4 Gb/sec
Noise	32 Gb/sec

New numbers coming out with improvements:

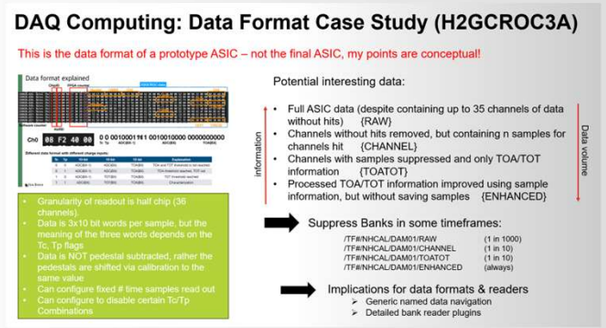
- Correct Thresholds
- Simulation Properties
- Updated Collider Lattice
- Distributions of hits within detectors
- More realistic ASIC behavior
- Better understanding of software triggering scheme

See Elke's talk and ePIC background group wiki

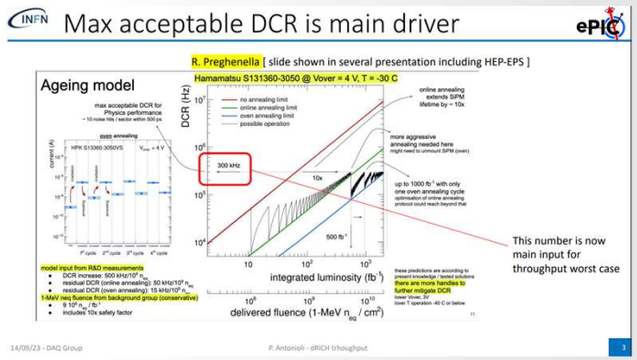
For now, these are last summer's numbers

Data Reduction Descriptions

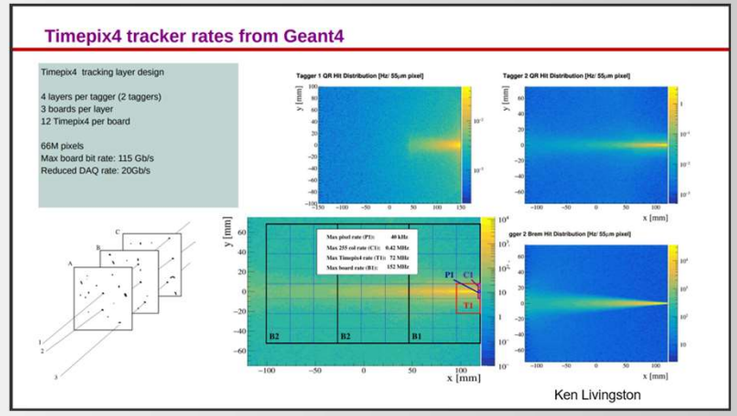
- Calorimeters / TOF
  - ➢ ASIC behavior (e.g. reads out data for channels with no hits)
- TOF / Calorimeters / MPGDs
  - ➢ Feature finding reduction due to charge sharing, sampled time durations
- dRICH
  - ➢ Time window relative to bunch crossing
  - ➢ SiPM Annealing
  - ➢ Software trigger
- Far Backward (Lumi Detectors)
  - ➢ Rate = 81ch * 10bit * 100MHz ~ 80 Gb/s
    - o Summarize deposited energy each bunch crossing (~1Gb/s)
    - o (or) Histogram deposited energy per channel for all 1160 bunches over ~100 bunch rotations
- Far Backward Low Q trackers
  - ➢ Software Collision Trigger
  - ➢ Prescale acceptable (arbitrary deadtimes…)



ASIC behavior



dRICH



Low Q Tracker

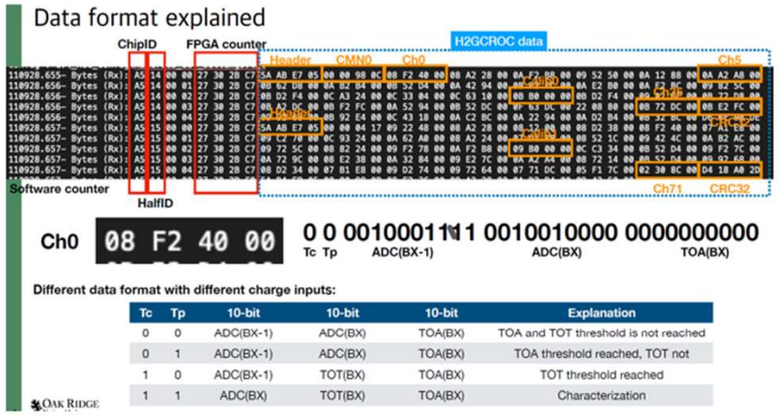
Data Reduction Descriptions

- Calor
  - ASI hits
- TOF
  - Fea san
- dRIC
  - Tim
  - SiP
  - Sof
- Far B
  - Ra
    - S (1
    - (c 1
- Far B
  - Sof
  - Pre

DAQ Computing: Data Format Case Study (H2GCROC3A)

This is the data format of a prototype ASIC – not the final ASIC, my points are conceptual!

(Info from Norbert Novitzki)



- Granularity of readout is half chip (36 channels).
- Data is 3x10 bit words per sample, but the meaning of the three words depends on the Tc, Tp flags
- Data is NOT pedestal subtracted, rather the pedestals are shifted via calibration to the same value
- Can configure fixed # time samples read out
- Can configure to disable certain Tc/Tp Combinations

Potential interesting data:

information

- Full ASIC data (despite containing up to 35 channels of data without hits) {RAW}
- Channels without hits removed, but containing n samples for channels hit {CHANNEL}
- Channels with samples suppressed and only TOA/TOT information {TOATOT}
- Processed TOA/TOT information improved using sample information, but without saving samples {ENHANCED}

Data volume

➡ Suppress Banks in some timeframes:

/TF#/NHCAL/DAM01/RAW	(1 in 1000)
/TF#/NHCAL/DAM01/CHANNEL	(1 in 10)
/TF#/NHCAL/DAM01/TOATOT	(1 in 10)
/TF#/NHCAL/DAM01/ENHANCED	(always)

➡ Implications for data formats & readers

- Generic named data navigation
- Detailed bank reader plugins

Data Reduction Descriptions

- Cal
  - A
    h
- TO
  - F
    s
- dR
  - T
  - S
  - S
- Far
  - F
    C
    C
- Far
  - S
  - F

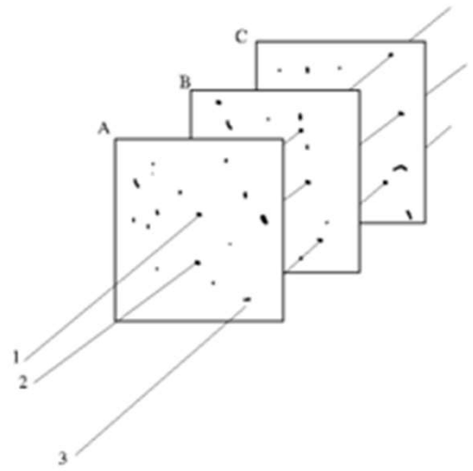
Timepix4 tracker rates from Geant4

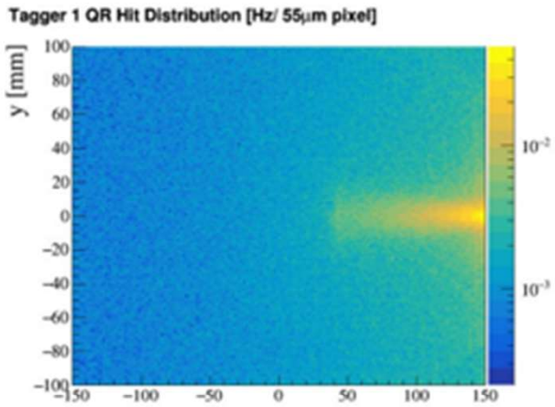
Low Q Tracker

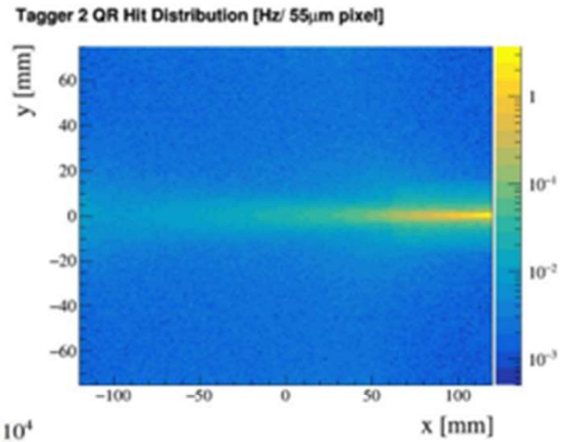
Timepix4 tracking layer design

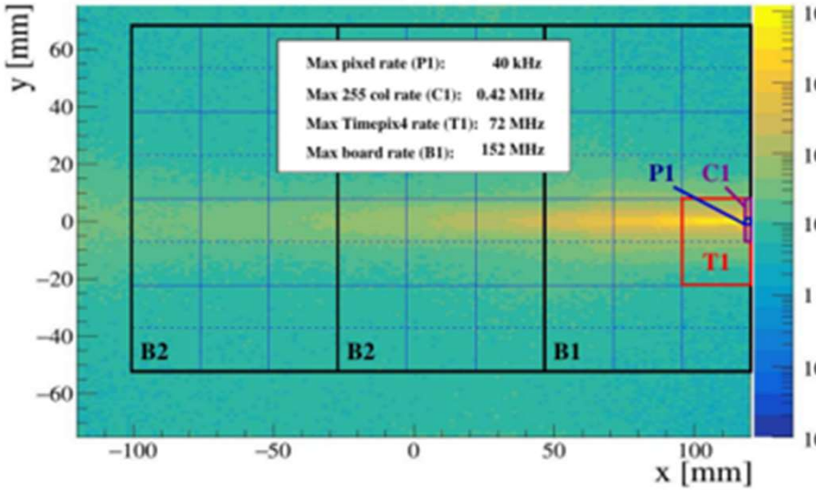
4 layers per tagger (2 taggers)
3 boards per layer
12 Timepix4 per board

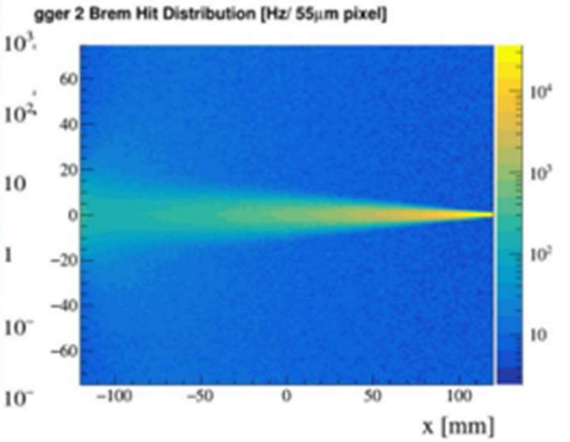
66M pixels
Max board bit rate: 115 Gb/s
Reduced DAQ rate: 20Gb/s











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Data Reduction Descriptions

- Calor
  - ASI hits
- TOF /
  - Fea sam
- dRICI
  - Tim
  - SiP
  - Soft
- Far B
  - Ra
    - S (~
    - (11
- Far B
  - Soft
  - Pre

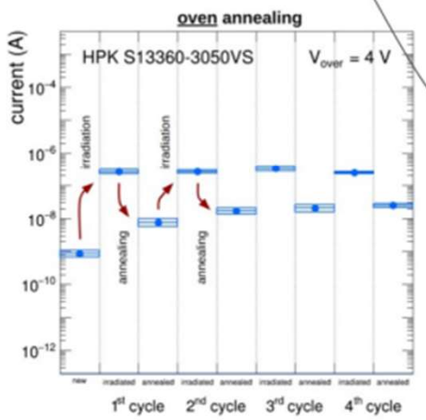
Max acceptable DCR is main driver

dRICH

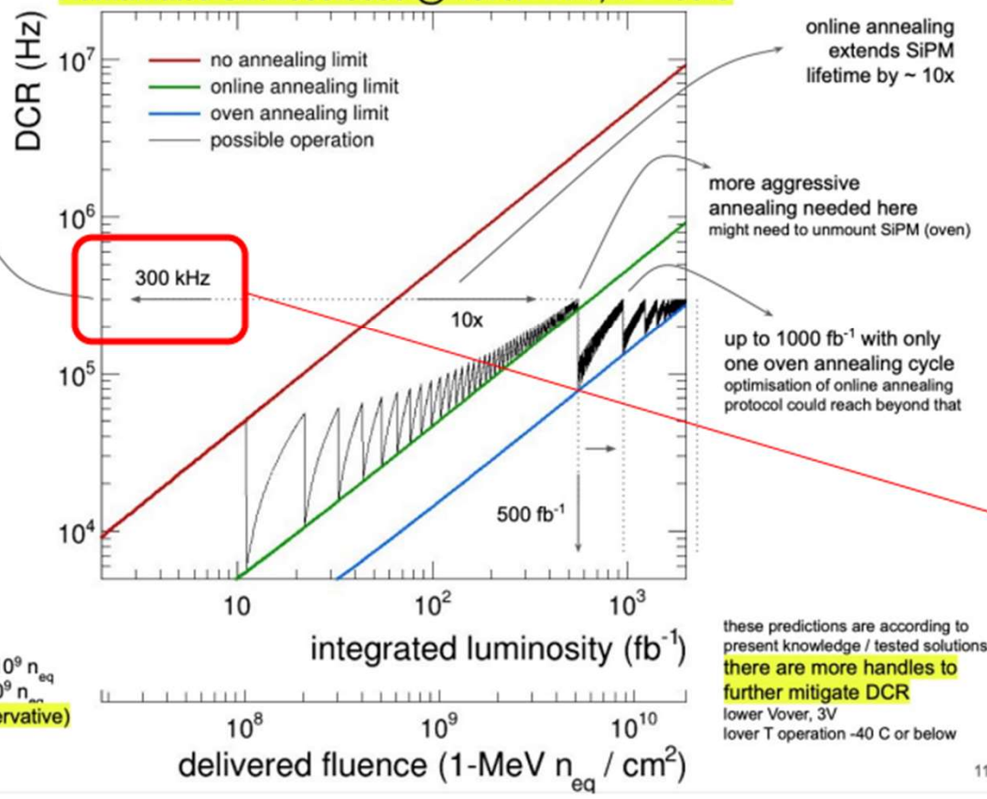
R. Preghenella [slide shown in several presentation including HEP-EPS]

Ageing model

max acceptable DCR for Physics performance
~ 10 noise hits / sector within 500 ps



Hamamatsu S131360-3050 @ Vover = 4 V, T = -30 C



online annealing extends SiPM lifetime by ~ 10x

more aggressive annealing needed here
might need to unmount SiPM (oven)

up to 1000 fb^{-1} with only one oven annealing cycle
optimisation of online annealing protocol could reach beyond that

these predictions are according to present knowledge / tested solutions
there are more handles to further mitigate DCR
lower Vover, 3V
lover T operation -40 C or below

model input from R&D measurements
- DCR increase: 500 kHz/10^9 n_{eq}
- residual DCR (online annealing): 50 kHz/10^9 n_{eq}
- residual DCR (oven annealing): 15 kHz/10^9 n_{eq}

1-MeV neq fluence from background group (conservative)
- 9 10^6 n_{eq} / fb^{-1}
- includes 10x safety factor

11

This number is now main input for throughput worst case

14/09/23 - DAQ Group | P. Antonioli - dRICH throughput | 3

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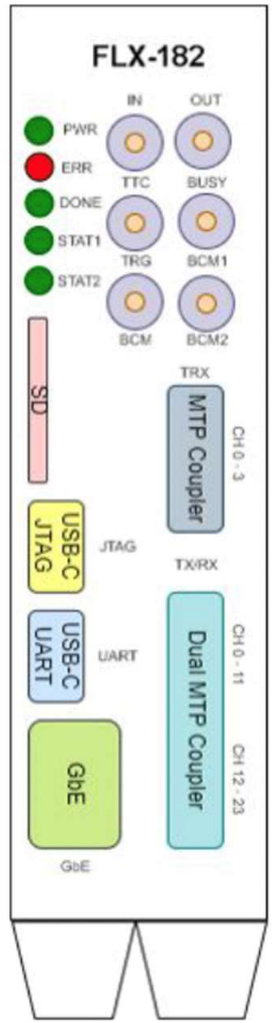
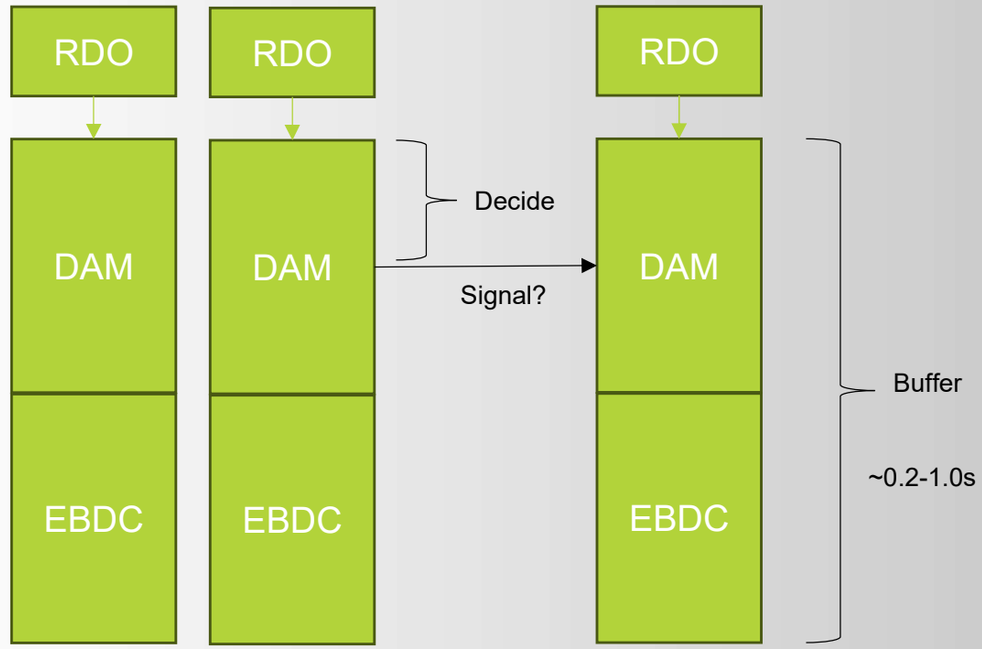
Triggering To Do

- Technical Issues
  - How is the communication handled?
- Trigger Issues
  - What are the algorithms, and what detectors go into the algorithms?
  - dRICH
    - ➢Does not need to be collision trigger. Trigger only needs to ensure that there is a real hit in the detector
  - Low Q Tracker
    - ➢Collision Trigger expected
    - ➢Could use prescale instead
- Collision detector detector?
  - Do we need one?
  - Can we construct one?
  - What would it look like?





Decision Signal not yet specified

- 100Gb Ethernet (switched)?
- Dedicated “Trigger” FELIX Boards?
- Hardware/Software Signals routed through GTU?

Data Reduction To Do List for TDR

Discussion…

EPIC Detector Scale and Technology Summary:

1/10/2023

Detector System	Channels	RDO	Gb/s (RDO)	Gb/s (Tape)	DAM Boards	Readout Technology	Notes
Si Tracking: Inner Barrel (IB) Outer Barrel (OB) Backward Disks (EE) Forward Disks (HE)	16B pixels	136* 440* 410* 410*	26	26	4* 11* 10* 10*	ITS-3 sensors ITS-2 staves / w improvements	RDO corresponds to number of VTRX+ Assuming each VTRX+ populates only a single TX/RX pair. If data volume is high, they can support 4 TX fibers which would increase FELIX counts
MPGD tracking: Electron Endcap Hadron Endcap Inner Barrel Outer Barrel	16k 16k 30k 140k	8 8 30 72	1	0.2	1 1 1 2	uRWELL / SALSA uRWELL / SALSA MicroMegas / SALSA uRWELL / SALSA	64 Channels/Salsa, up to 8 Salsa / FEB&RDO 256 ch/FEB for MM 512 ch/FEB for uRWELL
Forward Calorimeters: LFHCAL HCAL insert ECAL W/SciFi Barrel Calorimeters: HCAL ECAL SciFi/PB ECAL ASTROPIX Backward Calorimeters: NHCAL ECAL (PWO)	63,280 8k 16,000 7680 5,760 500M pixels 3,256 2852	74 9 64 9 32 230 18 15	502	28	2 1 2 1 1 5 1 1	SiPM / HG2CROC SiPM / HG2CROC SiPM / Discrete SiPM / HG2CROC SiPM / HG2CROC Astropix SiPM / HG2CROC SiPM / Discrete	Assume HGCROC 56 ch * 16 ASIC/RDO = 896 ch/RDO 32 ch/FEB, 16 FEB/RDO estimate, 8 FEB/RDO conserve. HCAL 1536x5 *HCAL insert not in baseline Assume similar structure to its-2 but with sensors with 250k pixels for RDO calculation. 24 ch/feb, 8 RDO estimate, 23 RDO conservative
Far Forward: B0: Crystal Calorimeter 4 AC-LGAD layer 2 Roman Pots 2 Off Momentum ZDC: Crystal Calorimeter 20 Silicon pad layer 3/1 Silicon pad layers HCAL	135 606,208 524,288 292,032 756 60,480 134,640 57,600	1 30 64 36 1 28 59 28	15	8	1 1 2 1 1 1 2 1	SiPM AC-LGAG / EICROC AC-LGAD / EICROC AC-LGAD / EICROC APD HGCROC as per ALICE FoCal-E HGCROC as per ALICE FoCal-E SiPM	 4 layer x 37 module x 4 EICROC x 1024 ch 2 stations x 2 layer x 32 module x 4 EICROC x 1024 ch 2 stations x 2 layer x 18 module x 4 EICROC x 1024 ch 20 Low granularity layers 3 High granularity layers + Veto Layer 3 blocks
Far Backward: Low Q Tagger 1 & 2 Low Q Tagger 1+2 Cal 2 x Lumi PS Calorimeter Lumi PS tracker High Rate Lumi Cal	66M pixels 144 1750/48 60k 81	24 1 1 10 2	150	1	10 1 1 1 1	Timepix4 SiPM (SiPM/HG2CROC) or(PMT/FLASH) AC-LGAD: FCFD or EICROC (strip) SiPM	2 tagger x 4 layer x 3 board x 12 timepix4 x (448x512) pix (up to 20 TX fiber / RDO due to high rate)
PID-TOF: Barrel Endcap	2.2M 5.6 M	288 212	31	1	8 6	AC-LGAD: FCFD or EICROC (strip) AC-LGAD: EICROC (pixel)	bTOF 128 ch/ASIC, 64 ASIC/RDO eTOF 1024 pixel/ASIC, 24-48 ASIC/RDO (41 ave)
PID-Cherenkov: dRICH pfRICH DIRC	317,952 69,632 69,632	1242 17 24	1240 24 11	13.5 12.5 6	30 1 1	SiPM / ALCOR HRPPD / EICROC (pixel) MCP-PMT (or HRPPD)	Worse case after radiation. Includes 30% timing window. Requires further data volume reduction software trigger