AC-LGAD Workfest Summary

Alex Jentsch (BNL)

On behalf of AC-LGAD workfest conveners

ePIC Collaboration Meeting

Argonne National Laboratory

January 9th-13th, 2024

Overview and Goals

- **Jan. 9th:**
  - Requirement and Design
  - AC-LGAD sensor
  - Frontend ASIC
  - Readout electronics
- **Jan. 10th:**
  - Detector Module
  - Mechanical structure and cooling
- **Jan. 10th & 11th:**
  - EICROC0 Demonstration (several sessions) organized by Alessandro Tricoli (Alessandro.Tricoli@cern.ch) & PrithwishTribedy (ptribedy@bnl.gov)

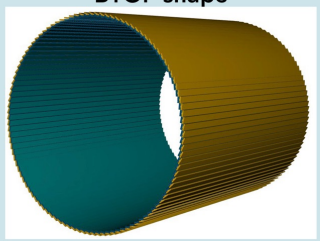
It's impossible to summarize the full scope of the important discussions which took place during the parallel session – please review the talks for more details on progress.

AC-LGAD applications (present)

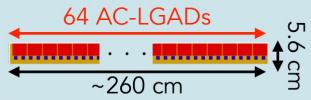
Slide from Satoshi Yano

- BTOF is composed of 144 modules to make a cylindric
- 64 AC-LGAD strip sensors are attached to one module
  - ASIC place is under discussion (depending on the ASIC pixel geometry)
- Radius is 60 - 63 cm from the beam pipe covering -1.42<η<1.77
- Total material budget in acceptance is ~0.01 X/X_0

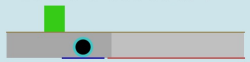
BTOF shape



Module top view

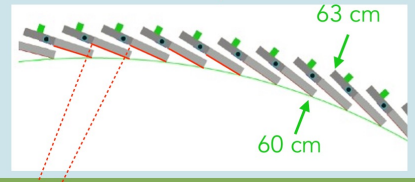


Module cross section

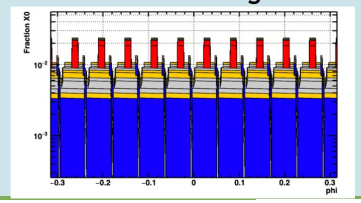


Cylindrical structure by modules

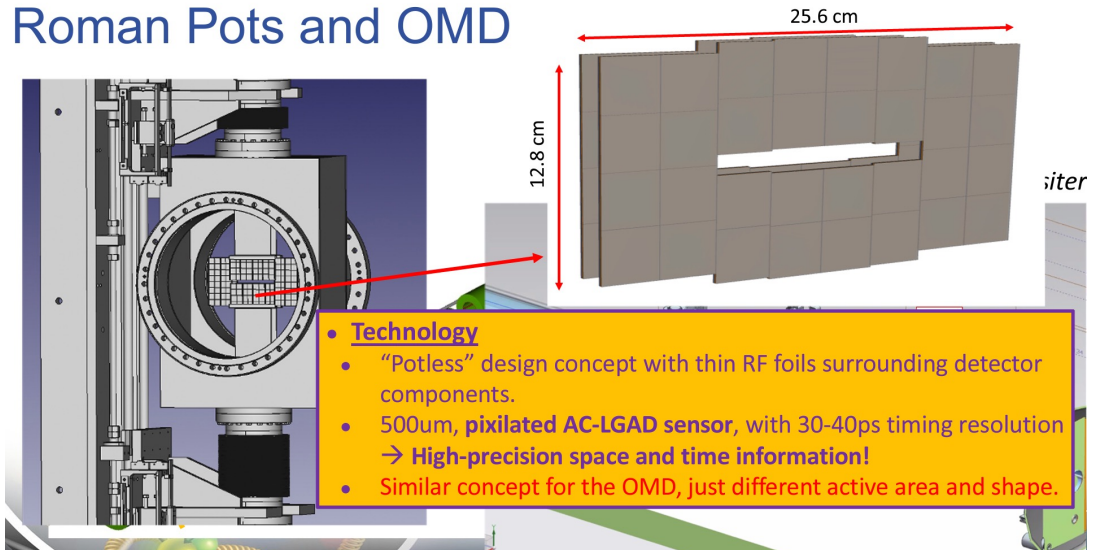
3 mm overlap in ϕ



Material budget



Roman Pots and OMD

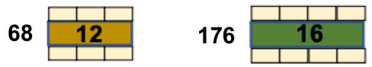


- **Technology**
  - "Potless" design concept with thin RF foils surrounding detector components.
  - 500um, **pixilated AC-LGAD sensor**, with 30-40ps timing resolution → **High-precision space and time information!**
  - Similar concept for the OMD, just different active area and shape.

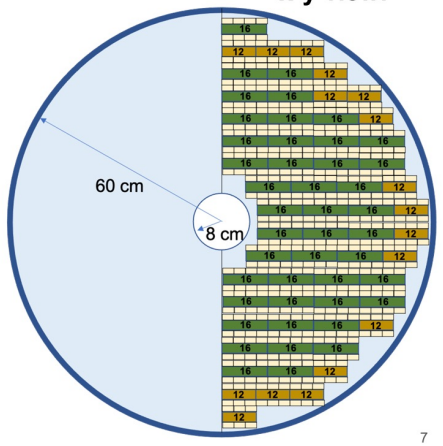
FTOF detector layout (v1)

FTOF disk will consist of two "DEE"s, made of carbon fibers and cooling pipes.

Each DEE is tiled by modules and SHs on both faces to maximize the coverage



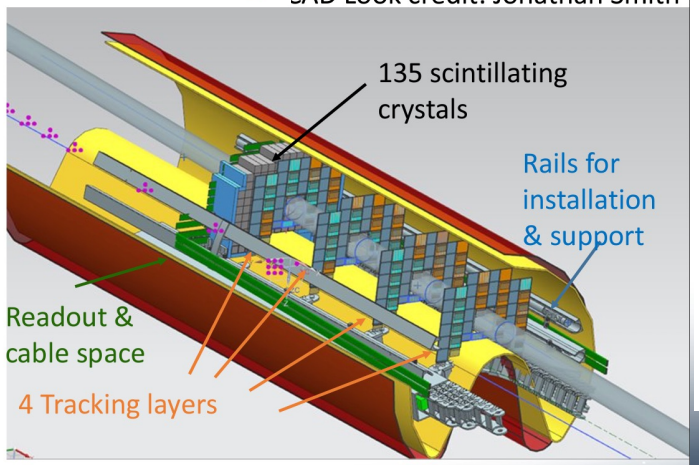
x-y view:



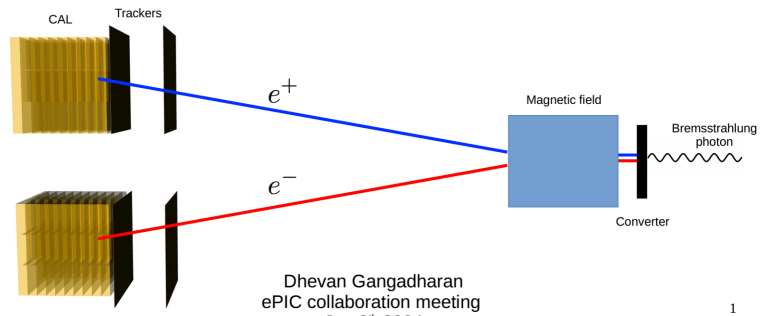
Slide from Wei Li

B0 Tracking

CAD Look credit: Jonathan Smith



AC-LGAD Trackers for the Luminosity Pair Spectrometer



Dhevan Gangadharan
ePIC collaboration meeting
Jan 9th 2024

AC-LGADs

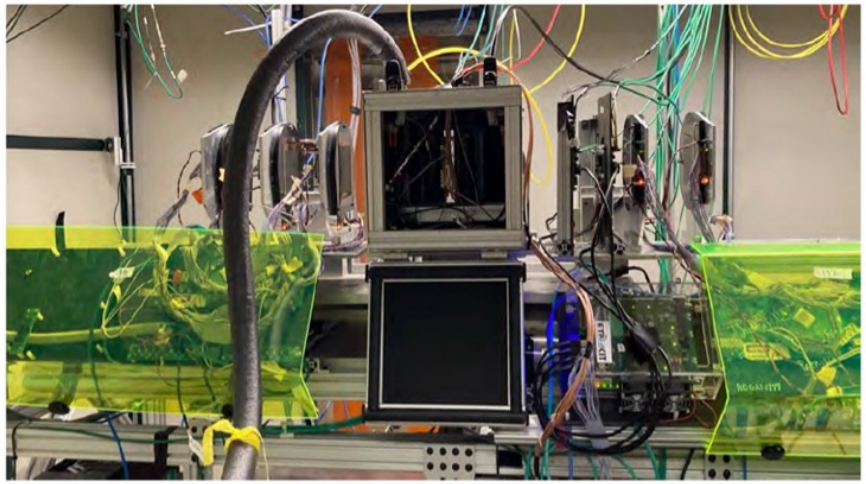
AC-LGAD Sensor

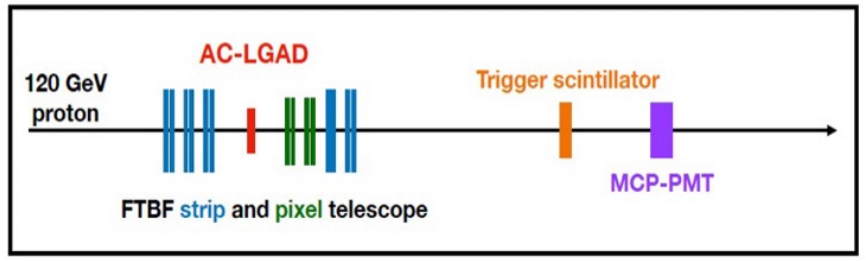
Slide from Zhenyu Ye

- Sensors with different configurations produced by BNL-IO and HPK, and tested with 120GeV protons
- Prototype strip sensors with ~35 ps time resolution and <15 um spatial resolution (more in the next talk).
- Prototype pixel sensors with ~20 ps time resolution and ~20* um spatial resolution.

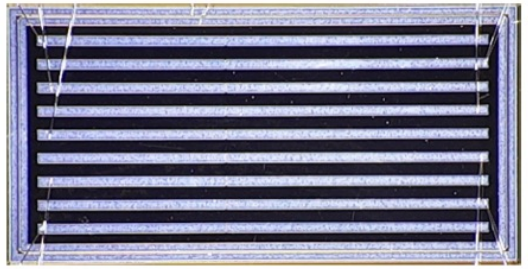
* ~50 um under metal electrodes. To be improved

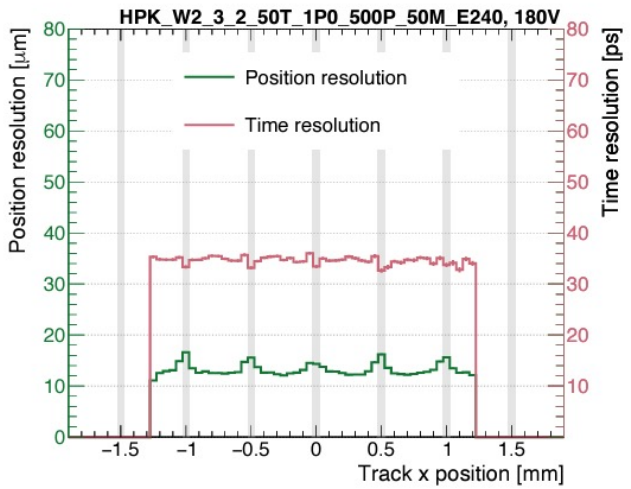
Fermilab Test Beam Setup



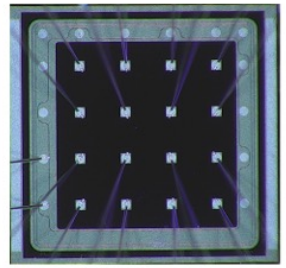


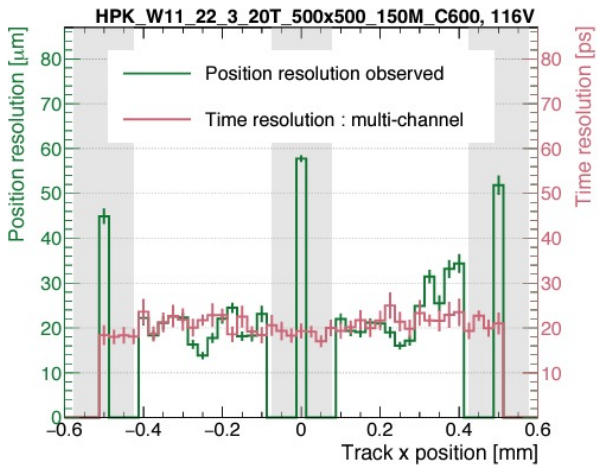
HPK Strip Sensor (4.5x10 mm²)





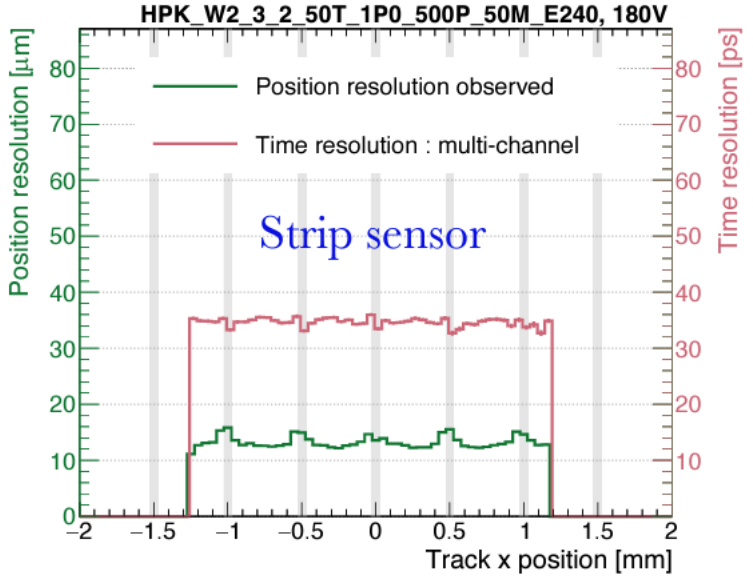
HPK Pixel Sensor (2x2 mm²)

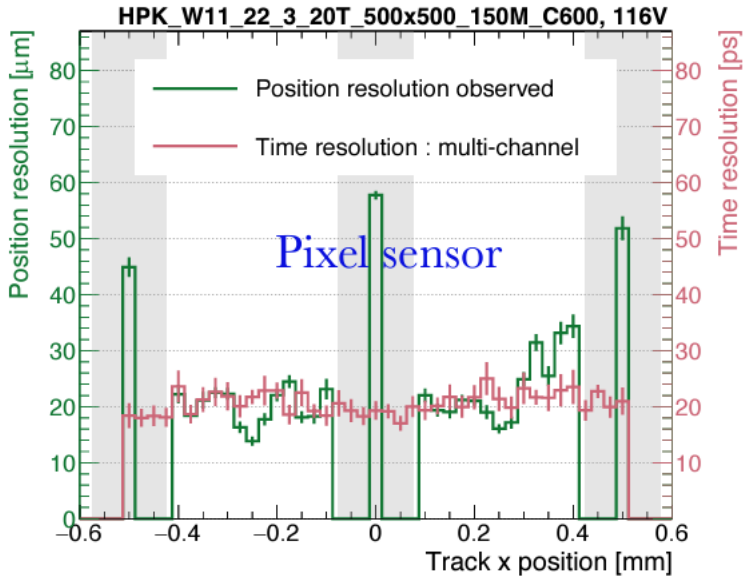




AC-LGAD production and testing

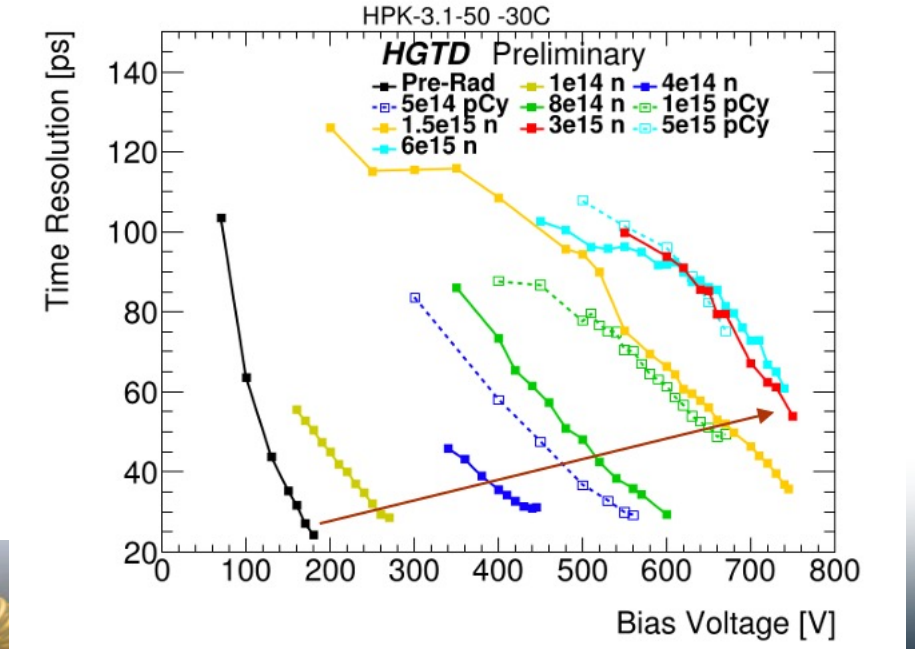
- **Beam and irradiation tests of *sensor* presented:**
  - Lab test talk shown by Jennifer Ott (Santa Cruz)
  - Beam test talk shown by Shirsendu Nanda (UIC) [plots shown to the right]
  - Irradiation experience with DC-LGADs and plans for testing with AC-LGADs talk shown by Simone Mazza (Santa Cruz) [plot below]
- Sensor production at BNL presented in talk by Gabriele Giacomini (BNL).
  - New sensor productions at HBK/FBK/BNL are planned.





Plot shows time resolution as a function of bias voltage for various levels of irradiation.

***Note: the fluences shown here are ~ 3 orders of magnitude higher than what is expected at ePIC.



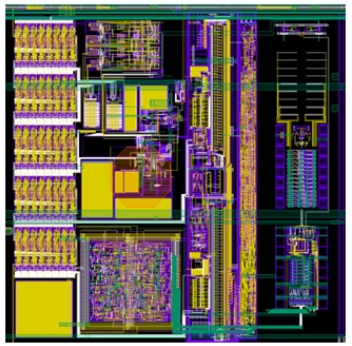
Readout for AC-LGADs

Frontend Readout ASIC

Slide from Zhenyu Ye

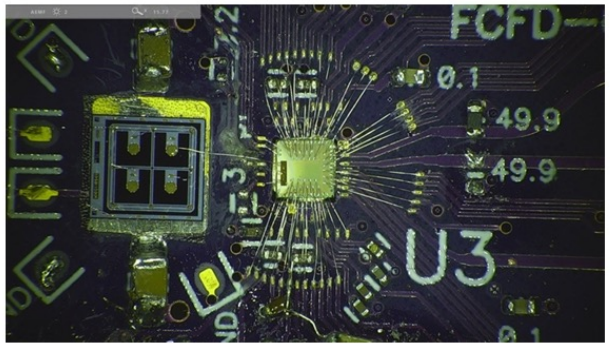
- **R&D Goals**
  - 15-20 ps jitter with minimal (1-2 mW/ch) power consumption, match AC LGAD sensors for ePIC.
- **Plan**
  - Utilize the design and experience in ASICs for fast-timing detectors from ATLAS and CMS, and investigate common ASIC design and development for TOF and FF.

Pixilated AC-LGAD (RP, B0, Forward TOF, Lumi pair spec)



EICROC by Omega/IJCLab/Irfu/AGH

- Preamp, discri. taken from ATLAS ALTIROC
- I2C slow control taken from CMS HGCROC
- TOA TDC adapted by IRFU Saclay
- ADC adapted to 8bits by AGH Krakow
- Digital readout: FIFO depth8 (200 ns)



FCFD by Fermilab (more in the next talk)

- Adapt the Constant Fraction Discriminator (CFD) principle in a pixel paired with a TDC, one time measurement gives the final answer.
- Charge injection consistent with simulations: ~30 ps at 5 fC, and <10 ps at 30 fC
- Tested with laser, beta source and beam

Strip AC-LGAD (Barrel TOF)

Discussions with experts during meeting suggested that modified HGCROC could be an option for AC-LGAD strips (see Christophe's talk).

See talk by Christophe de la Taille (Omega): https://indico.bnl.gov/event/20473/contributions/85274/attachments/51864/88689/CdLT_EICROC_9jan24.pdf

See talk by Artur Apresyan (Fermilab): https://indico.bnl.gov/event/20473/contributions/85276/attachments/51862/88685/FCFD-ePIC.pdf

Top-level goals of the various R&D efforts

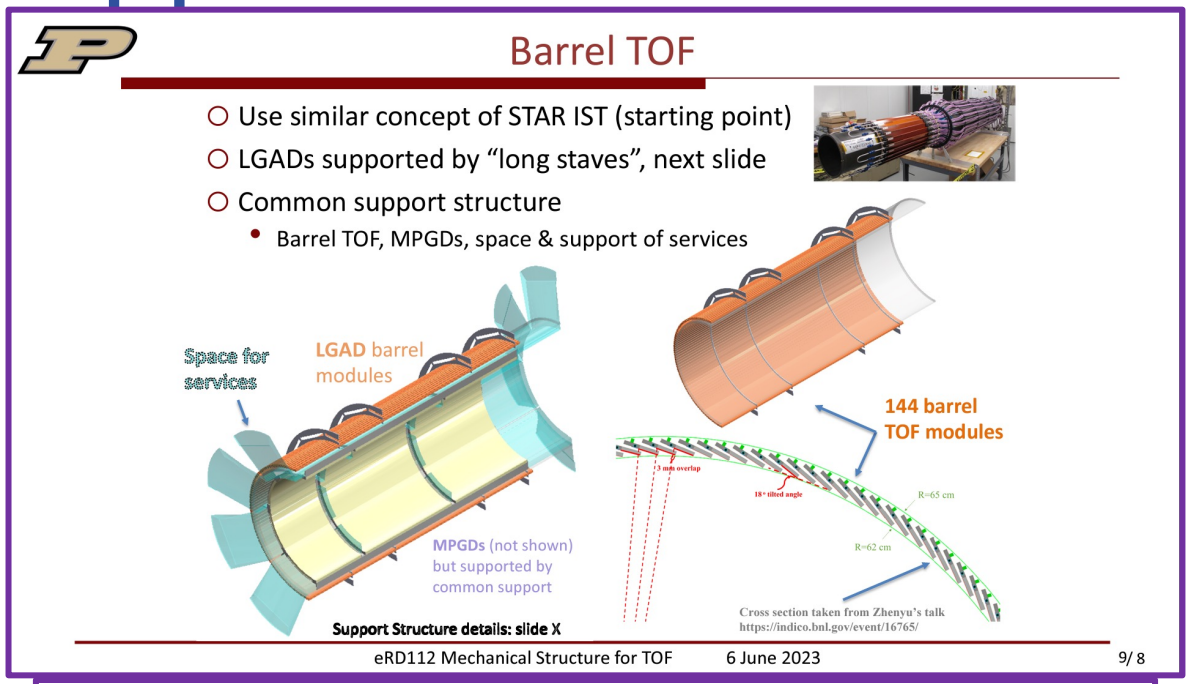
- Refinement of sensor to maximize spatial resolution via charge/signal sharing.
  - ~ x7 improvement in resolution from standard (pixel pitch)/Sqrt(12), but areas for improvement exist.
- Timing requirements.
  - Sensor alone meets requirement → noise, ASICs, etc. can all contribute to worsening the performance – work to be done to mitigate effects, more testing of full packages (e.g. sensor + ASIC + boards) needed.
- Power consumption.
  - ASIC design aiming for ~ 1mW/channel power. Non-trivial, but current progress is promising.
- Engineering design for support systems for the detector packages.
  - Bump-bonding of sensor/ASIC packages (Mathieu Benoit talk)
  - Cooling (liquid for TOF; under-discussion for B0/Lumi; conductive cooling for RP/OMD)

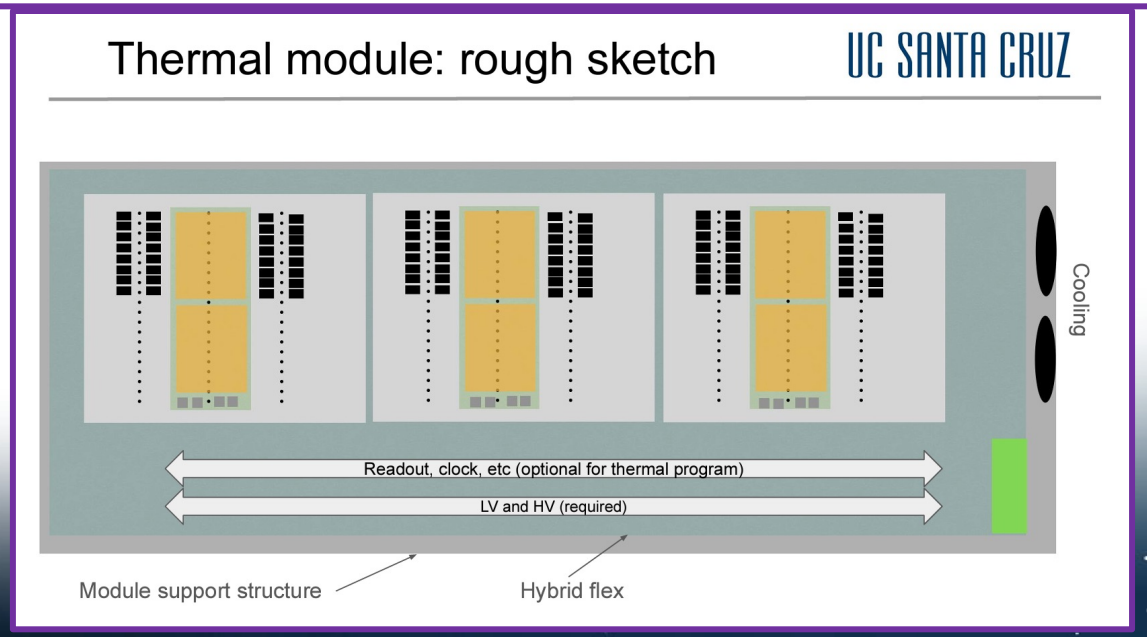
Preliminary plan for test beam in June at DESY (details to be worked out).

Progress on engineering/support

- Mathieu Benoit (ORNL) and Matthew Gignac (Santa Cruz) presented plans on the module assembly for FTOF and BTOF, respectively.
  - Plan on BTOF module prototyping will soon be presented as a PED request to the project (a similar plan for FTOF will follow) [plot on bottom right].
- R&D for CF module structures for BTOF staves well underway – see talk by Shushrut and Andy (Purdue).
- Thermal simulation work underway (e.g. Ansys) – see talk by Yu-Tang and Yi (NCKU).
- Progress on global mechanical support for TOF systems – see talk by Andy from Purdue [plot on top right].

FEA studies are being done together with studies of material budget to balance cost and required specs for physics.

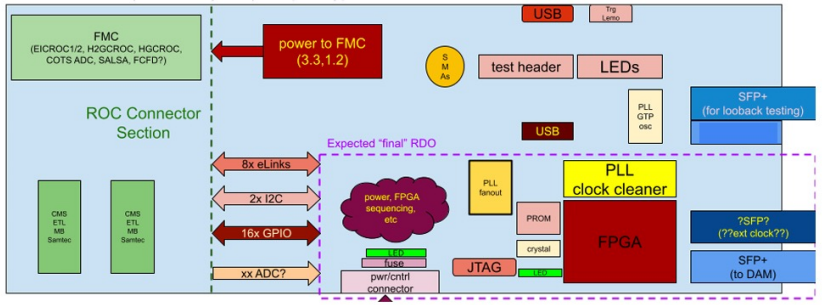




Progress on electronics

- Plan for frontend electronics for TOF – see talk by Tonko (BNL).
- Low-mass Kapton PCB talk by Oskar (ORNL)
- Service hybrids talk by Wei Li (Rice) [plot on right].
- Details on needs for common electronics presented in talk by Zhangbu Xu (BNL).

Readout board prototype v0 design



FPGA section:
- Xilinx Artix Ultrascale+ family
- PROM for remote reconfiguration
- PLL for clock jitter cleaner

- essentially serves functionalities of lpGBT+SCA/MUX64

Optical fiber - SFP+ modules
- 1 for data/timing, 10Gbs
- 1 transceiver for direct clock timing-only, 100MHz
- 1 for various loopback tests (NOT on the final RB)

ROC connector:
- Connection to EICROC FMC test board
- Connection to CMS ETROC2 module board

First very preliminary PCB schematic done! Lots of details to be worked out next. 6

Service hybrid to replace commercial XILINX board currently used for testing.

Experience with DC-LGADs in LHC experiments

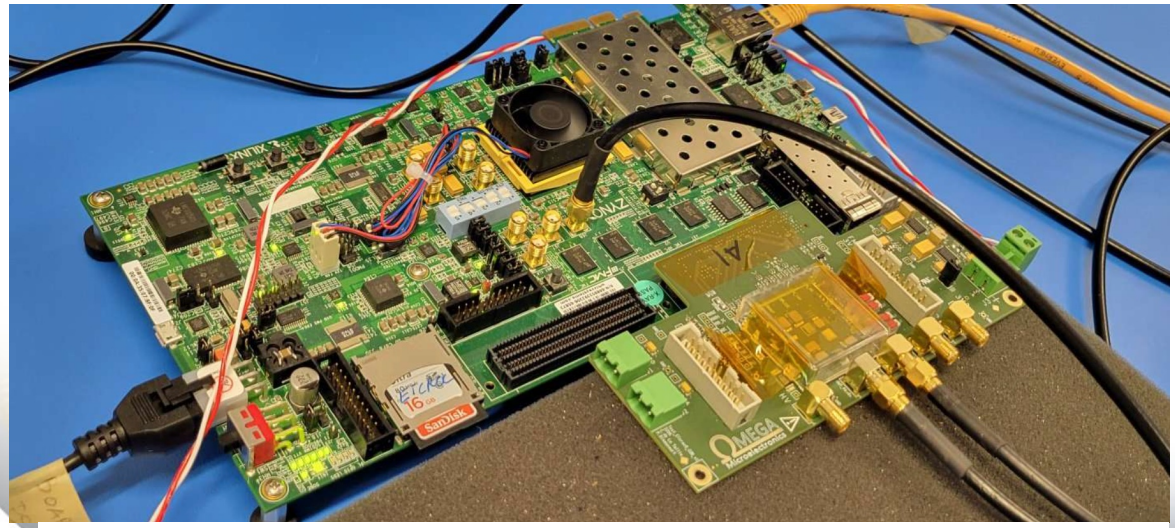
- Development of LGAD ETL system for CMS presented in talk by Chris Madrid (Fermilab).
- Experience with ETROC for CMS ETL presented in talk by Ted Liu (Fermilab).

➢ Helpful to see progression of design for both sensor and ASIC for this subsystem in CMS – helps us to identify potential trouble spots in testing, fabrication, and construction of full detector and learn from the wealth of experience.

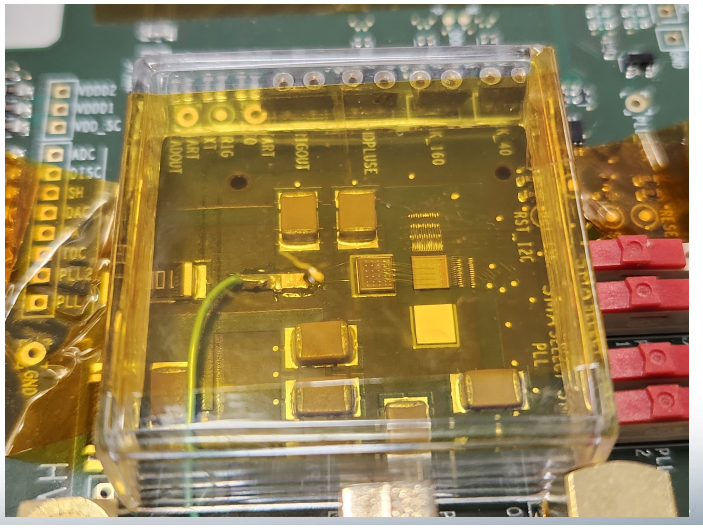
  - Discussions will continue as AC-LGAD systems evolve.

Some real “work” taking place this week

- AC-LGAD folks took advantage of being in-person to try and work on testing.
  - Extra-special thanks to Manoj Jadhav, Whitney Armstrong, et al. for helping us with lab space, power supplies, scope, etc.
- Friends from IJCLAB, OMEGA, BNL, Japan, et al. met together to try and short-circuit remote testing to ensure testing apparatus can provide reproducible results.
  - Goal is to work together on EICROC0 + AC-LGAD setup to inform refinements and improvements for the next version & discuss future plans (e.g. test beams).

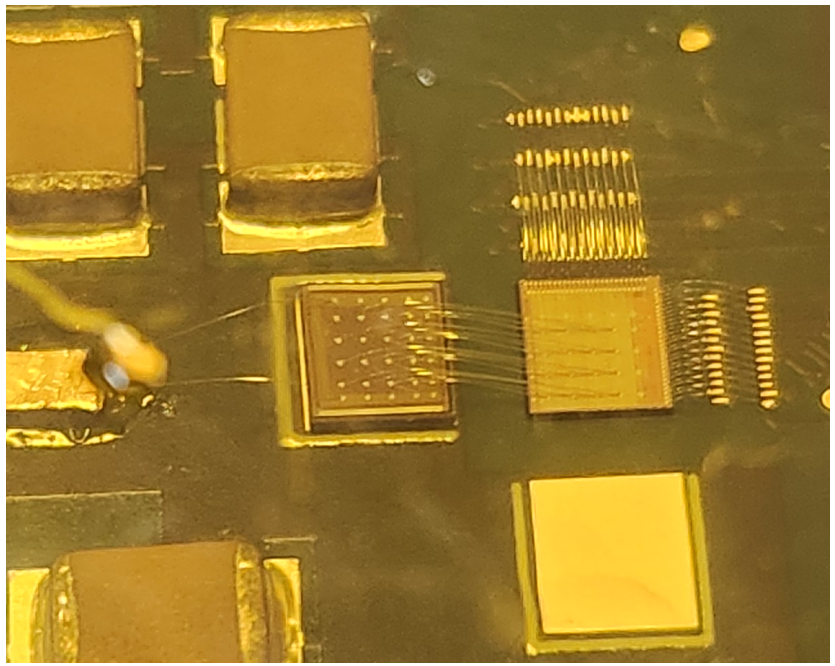


Test board produced by OMEGA (smaller board) connected to XILINX for DAQ (larger board).

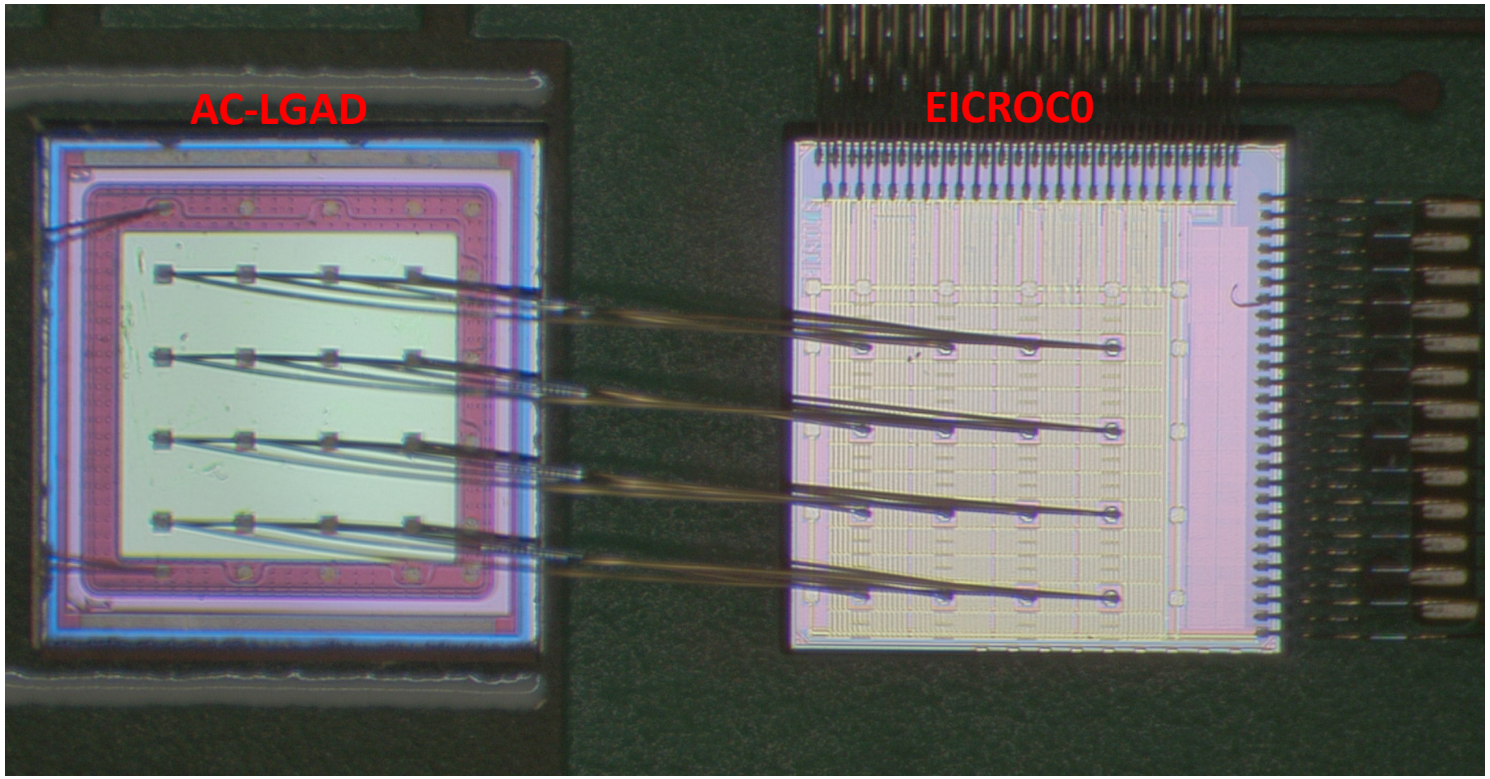


BNL-produced AC-LGAD sensor wire-bonded to EICROC0 (OMEGA/ICJLab).

Some real “work” taking place this week



- AC-LGAD sensor (BNL) wire-bonded to EICROC0 (OMEGA/ICJLab) for testing on custom test board produced by OMEGA.



BNL AC-LGAD:

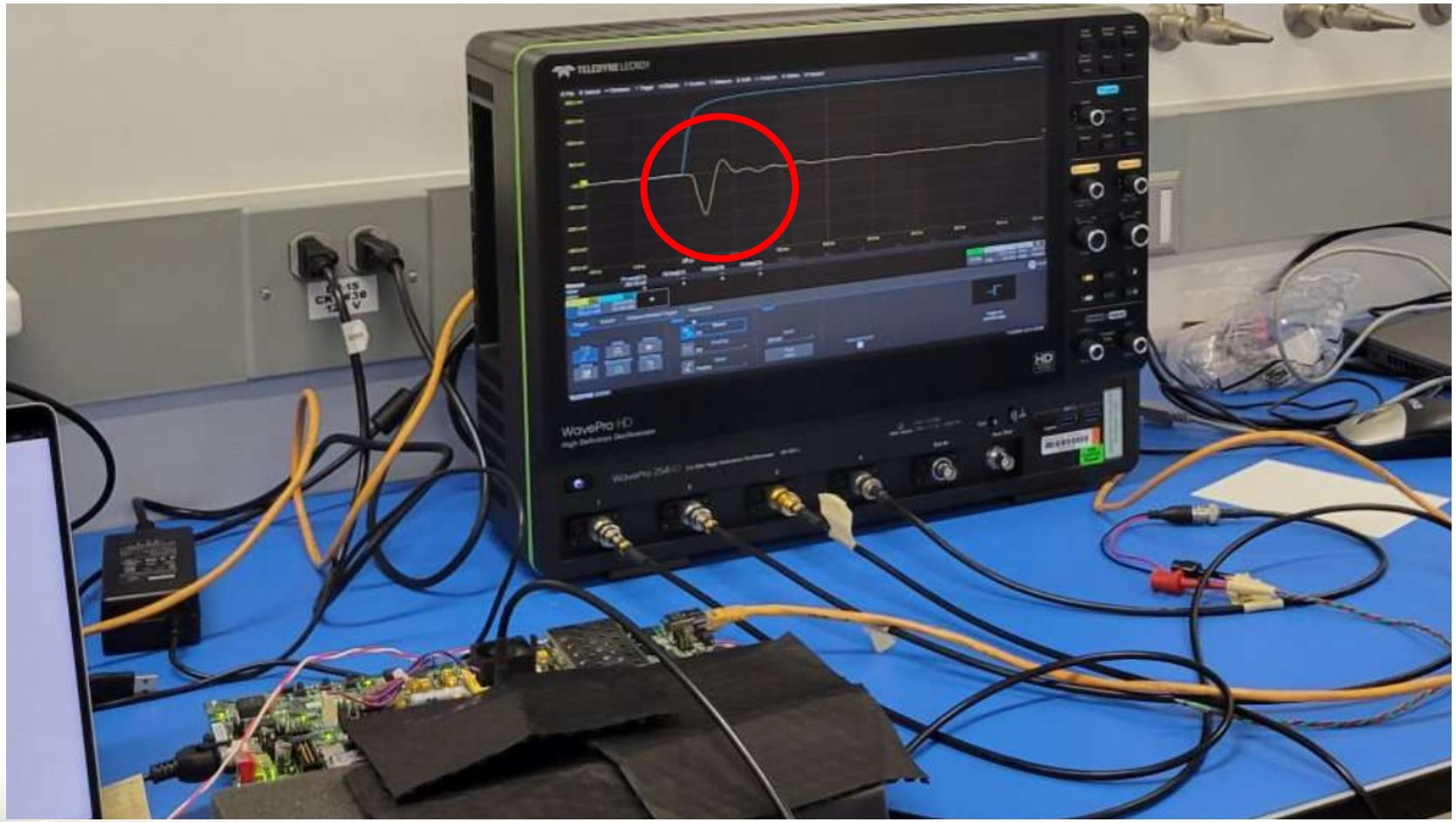
- 500x500 um^2 pixel pitch
- 100x100 um^2 metal electrode
- 30um active thickness

- Setup is presently wire-bonded for initial tests, bump bonding to follow very soon – both at BNL.
- Two other similar boards with EICROC0 were produced and sent to IJCLab and Hiroshima U. for testing.

Some real “work” taking place this week

- Full test setup with borrowed LV/HV power supplies, scope, and some cables. (thank you ANL lab friends for your immense help and patience).
- The test bench enabled in-person troubleshooting (which is ongoing today as well ☺).

Some real “work” taking place this week



- Actual analog signal from beta source on AC-LGAD, read through the EICROC0 + test-board and XILINX.

Work allowing for nice demos

- See how happy everyone is? It must be the clean room PPE.

Some key takeaways

- Being in-person for troubleshooting readout has been crucial → it saves on time immensely.
  - We are working on a follow-up meeting as we move toward the new ASIC versions.
- Test-beam and irradiation test planning very much underway.
  - Preparation of test-setup (e.g. bonding sensor + ASIC, final characterization of ASIC, etc.)
  - Understanding of setup at testbeam location (availability of support/alignment systems, reference telescopes, beams + energies, etc.)
- There is lots to learn from our friends who have experience with the DC-LGADs in present experiments.
- Progress made recently on engineering design → more work to be done to optimize balance between specs, complexity, robustness, and cost on the way to the TDR.
- Workfest format was beneficial for this group, and we thank all who participated in the meeting!