ePIC Collaboration Meeting - Jan 2024 (ANL)

### AstroPix v3

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### **AstroPix Developments**

<code>AstroPix v1</code> - 0.45 cm  $\times$  0.45 cm chip

- $18 \times 18$  pixel matrix, 175 µm pitch
- Tested for analog output





**AstroPix v2** - 1  $\times$  1 cm2 chip (MPW)

- $35 \times 35$  pixel matrix, 250 µm pitch
- Row/Column hit identification
- Analog + digital output





# **AstroPix v3 Specifications**

#### AstroPix v3

- $2 \times 2$  cm<sup>2</sup> full-size chip with  $35 \times 35$  pixel matrix
- 300 µm pixel size, 500 µm pixel pitch
- Increased spacing between the outer pixel nwell and the chip edge
- Timestamp clock 2.5MHz, ToT clock 200 MHz
- 10-byte data frame per hit
- Chip-generated injection signal
- The first 3 columns are implemented with PMOS amplifier



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# AstroPix v3 Measurements

#### Full-size chip (ongoing testing)

- Sensor characterization
  - IV/CV measurements
  - TCT measurements
- Test bench validation and optimazation
- FTBF testbeam performance studies
- Active and passive irradiation ~10<sup>15</sup> n<sub>equivalent</sub>/cm<sup>2</sup>
- Quad-chip readout (under testing) for NASA's hosted payload mission (A-Step) (Taylor's talk)
- Integration with Pb/SciFi (Henry's talk)

#### IV measurements for different versions



#### APXV3 W02S09 at 2-20kHz and W08S12 at 2-10kHz CV



### **AstroPix v3 Results**

#### **Test Bench Measurements**

- Injection voltage scan shows that the analog and digital ToT agree well
- The energy resolution of 5.6% is measured using an injected pulse
- Noise scan shows <1% of noisy pixels</li>
  resolves issue with noisy pixels observed with v2
- Noisy pixels can be masked by disabling the comparator





# **AstroPix v3 Results**

#### Source Scan Measurements

Ba133, 30min, ~8 nCi

Ba13

32

30

28

26

24

22

20

18

16

14

12

10

0 2

- Am241, 10min, ~106 nCi
- 200 mV threshold, delta(TS)<=1
- First 3 cols (PMOS) disabled
- Ba133, 5min, ~8 nCi, enabling PMOS amplifier col

10<sup>2</sup>

10<sup>1</sup> 101

- higher hit rate in PMOS cols

14 16 18 20 22 24 26 28 30 32 34

6 8 10 12 14 16 18 20 22 24 26 28 30 32 34



Ba133 - 93.6% of hits paired

8 10 12 14 16 18 20 22 24 26 28 30 32 3

0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34



4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34



#### Mean ToT distribution

### AstroPix v3 TestBeam



Participants: Jihee Kim, Maria Zurek, Manoj Jadhav, Jessica Metcalfe

# AstroPix v3 TestBeam Results

### 120 GeV Proton Low intensity beam

- 120 GeV Proton
  - 5000 protons/spill
  - 4.7 mm  $\times$  4.8 mm beam spot
- Data acquisition
  - Total 8 hours
  - 300 mV threshold
  - HV bias voltage 150 V
- Total 37,472 raw events
  - 96.67 % of events were decodable
  - 44,742 pixels\* were fired
  - Among 91.1 % of active pixels, 91.02 % of pixels were fired
- Uniform pixel response for Minimum Ionizing Particle

\*Matching hits with exact time timestamp + ToT matching



### **Software and Firmware Development**

SW led by N. Striebig (KIT) and A. Steinhebel (GSFC), FW led by R. Leys and N. Striebig (KIT)

- FW-driven SPI readout to reduce deadtime
  - The self-trigger readout when there is data in buffers without SW check
  - Sensor data frame detection, IDLE discard, Tagging/reframing, routing to single Readout Buffer
- FW Scale-ability
  - Read through the daisy chain in FW rather than SW
  - Up to 20 daisy-chained SPI inputs have their own interfaces, which feed into the global buffer
- SW speedup to match FW
  - Reduce the chance of incomplete data return
  - Speed-up in analysis scripts, esp. when probing every pixel individually

#### Slide from Amanda's Talk in TIC

### **Next Steps**

- Energy calibration of AstroPix v3
- Optimize configuration settings
- Depletion depth measurements are ongoing
  - TCT data collected by Amanda with the help of UCSC colleagues
- Irradiated AstroPix v3 with different 400 MeV Proton dose
  - Data analysis and sensor characterization of irradiated samples
- AstroPix v3 quad-chip development
  - Carrier board if designed by Taylor (check his talk this afternoon)
  - We have assembled the first few boards
  - They are under testing
- Module-like board design with 8 single chips is undergoing



AstroPix v3 quad-chip carrier board

- Demonstrate required services
- Daisy chaining

### Thank you

### AstroPix

#### HV-CMOS Monolithic Active Pixel Sensor (MAPS):

- Combination of silicon pixel and front-end ASIC
- On-pixel charge amplification and digitization
- The technology uses more typical CMOS wafer processing for cost-effective mass production
- Fabrication on a single wafer enables a shorter design cycle
- No need to bump-bond to each pixel improves yield

#### AstroPix (based on ATLASPix3 arXiv:2109.13409)

- 180 nm HV-CMOS MAPS sensor designed at KIT (also designed ATLASPix, MuPix, etc.)
- Developed for AMEGO-X GSFC/NASA mission (Upgrade to the Fermi's LAT)

AstroPix





### **AstroPix v3 Iradiation**

- IV and CV measurements performed for the v2/v3 chips before irradiations
  - Same measurements will be repeated post irradiation
- 9 v2 & 6 v3 chips irradiated for Passive Irradiation (Al-foil dosimetry)
- Active Irradiation for Latch-up (and SEE) is planned week of 26th May

#### V2 Irradiation

Nb of samples	Doses (400 MeV protons)
3	4.50E+13
3	1.08E+15
2	1.01E+16
1	5.02E+16

#### V3 Irradiation (low and high ResChips)

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Nb of samples	Doses (400 MeV protons)							
2	4.50E+13							
1	5.04E+15							







AstroPix

# **AstroPix Readout**

- 10 bytes of data per hit header (chipID, payload), row/column, timestamp, ToT
- SPI I/O daisy chained chip-to-chip signal transfer
  - signals are digitized and routed out to the neighboring lex bus tape chip using 5 SPI lines via wire bond **Digital periphery**
- Power/Logic I/O distribution on the module (through a bus tape)
  - 4 power lines (LV, HV), ~20 Logic I/O (SPI, clk, timestamp, interrupt, digital Injection, etc.)
  - HV, VDDA/VDDD(1.8V), VSSA(1.2V), Vminuspix(0.7V) §
  - power distribution can be controlled using voltage regulators
  - mostly part of the end of the stave services
- Data will be received by FPGA at the end of the stave
  - FPGA aggregates data before sending off-detector
- Low heat load at chip, only cooling of end of the stave card
- The operational temperature for AstroPix is at room temperature and considered to be operated at 22 °C AstroPix





# **AstroPix Assembly**

#### AstroPix v5 (Production version)

- Full size chip  $2 \times 2$  cm<sup>2</sup>, pixel pitch 500  $\mu$ m,
- $35 \times 35$  pixel matrix  $\rightarrow 1225$  hit buffers
- Fix any bug from v4



\*The designs presented on these slides are not final but for illustration only

### **Module Strategy**

- QC testing with wafer probing + Module and stave level QC testing and tuning
- "Baseline" model of Modules on Stave
  - Module 8 single chips
  - Stave 13 Modules 104 chips
  - 12 or 14 Staves per AstroPix layer per Calorimeter Sector
  - Total 249600 chips
- All staves are identical and get combined in a separate production step
- Data is transmitted to the end of the Stave card using flex base tape
- Institutions ANL, GSFC/NASA, KIT, UCSC, Korea, Oklahoma State

# **AstroPix Timeline and Production**

### v3 full size chip (ongoing testing)

- Test bench characterization (ongoing)
- Testbeam performance studies
- Active and passive irradiation ~10<sup>15</sup> n<sub>equivalent</sub>/cm<sup>2</sup>
- Quad-chip readout (ready to test) for NASA's hosted payload mission (A-Step) - January 2025
- Integration with Pb/SciFi FY2024 (Henry's talk)

### v4 new features for better performance (MWP)

- **Final design version**, smaller chip (1cm × 1cm)
- Fabricated wafers delivered last week
- Chip carrier board design for bench test is ready for the PCB fabrication

### v5 full size final chip

- Fix any bugs from v4
- v5 chips available November 2024

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v3 Depletion Test																									
v3 multi-layer testing (A-STEP)																									
Integrate v3 w/ proto Segment																									
AstroPix v4 MPW design + fab																									ĺ
AstroPix v4 carrier board																									
AstroPix v4 testing																									
v4 Depletion Test																									
Standard test procedure dev.																									ĺ
AstroPix v5 testing carrier board																									
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GSFC/NASA ComPair-2 AstroPix timeline

### **BIC@ePIC** Timeline

- Prototype R&D (v3) Ongoing till Nov 24
- Pre-Production (v5) chips starts Nov 2024 (More info in Maria's talk)

### Production

• Fabrication by TSI - with a large production order, AMS is a backup