AstroPix v4 Design and first tests

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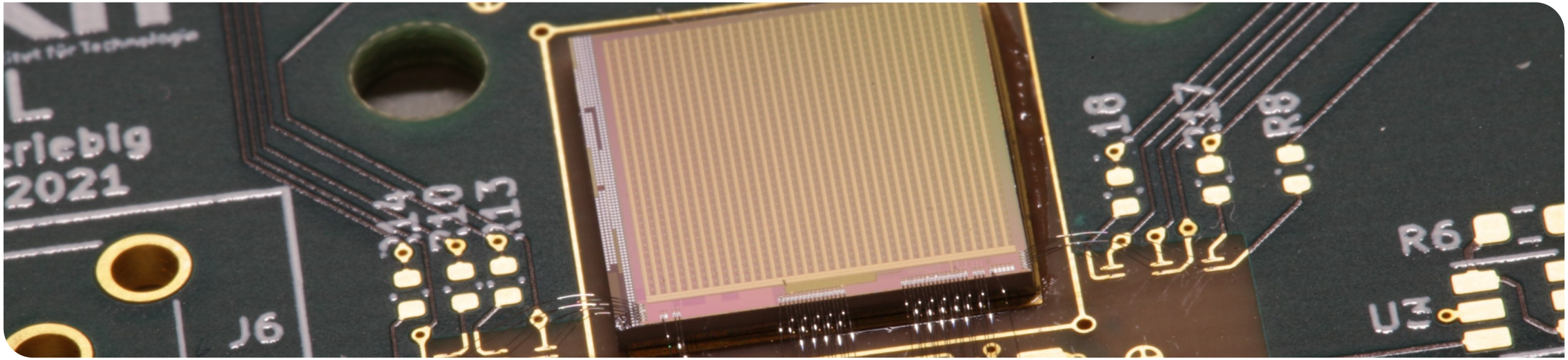


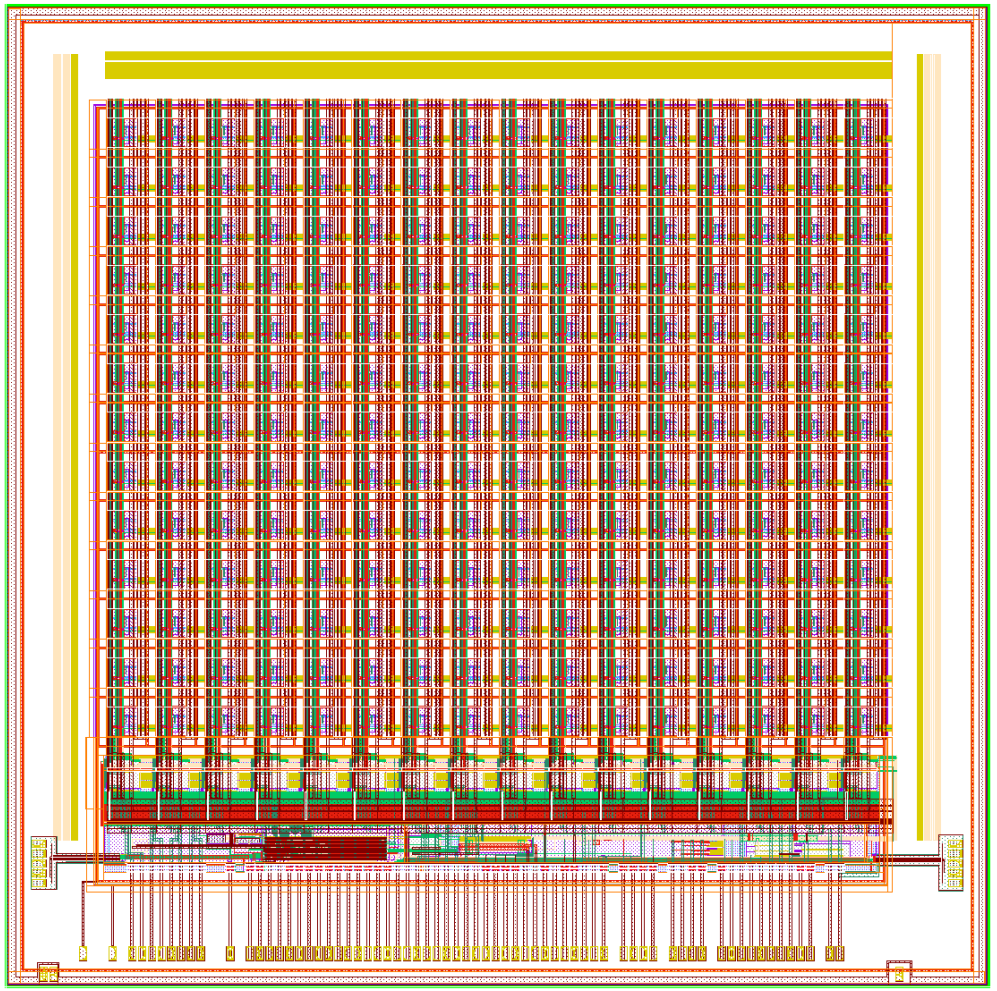
Content

- AstroPix4 design
- First functionality tests
- Summary and Outlook

Specifications for TSI May 2023 run

- Size: 1 cm x 1 cm
- Matrix: 16 x 13 pixels
- Pixel size: 300 um x 300 um
- Pixel pitch: 500 um
- Interfaces: QSPI Daisychain, SR
- Integrated voltage DACs
- Integrated injection switch
- Integrated temperature sensors

- **Improvements over v3:**
  - TuneDACs
  - Hitbuffers + FlashTDC measurement
  - Reduced pixel capacitance
    274 fF vs 391 fF @100um depletion

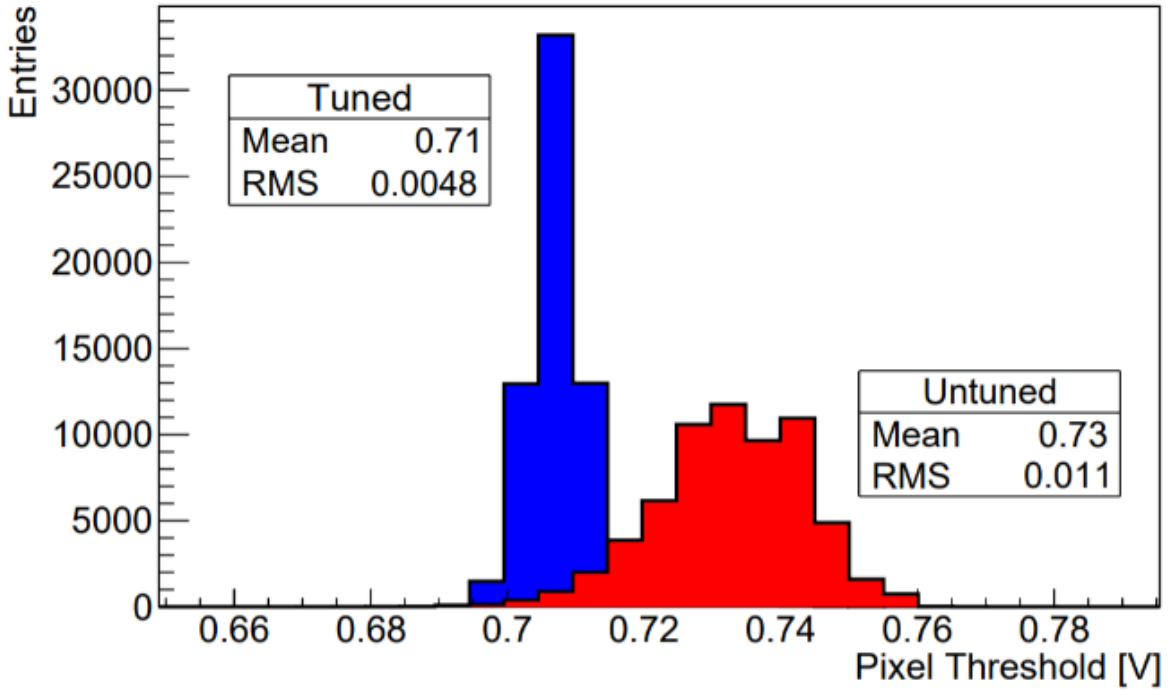


AstroPix4 I/O

- Clocks: 2.5 MHz timestamp clock (used as refclk for PLL)
- Digital Interfaces:
  - QSPI max. 5 MB/s: Configuration, Readout
  - Shiftregister Interface: Configuration fallback
- Interrupt, Hold
- Analog output: monitor amplifier output in Row0
- Hitbus: monitor comparator outputs
- Cal: Injection pulse
- Power:
  - Analog 1.8 V + 1.2V
  - Digital 1.8 V
  - Vminuspix 0 – 0.9 V
  - HV

TuneDACs

- 3 SRAM cells per pixel to control current DAC
- Number of bits can be increased if needed
- Placed in periphery
  - would add capacitance if placed in pixel
- Used to tune comparator branch currents to compensate threshold dispersion

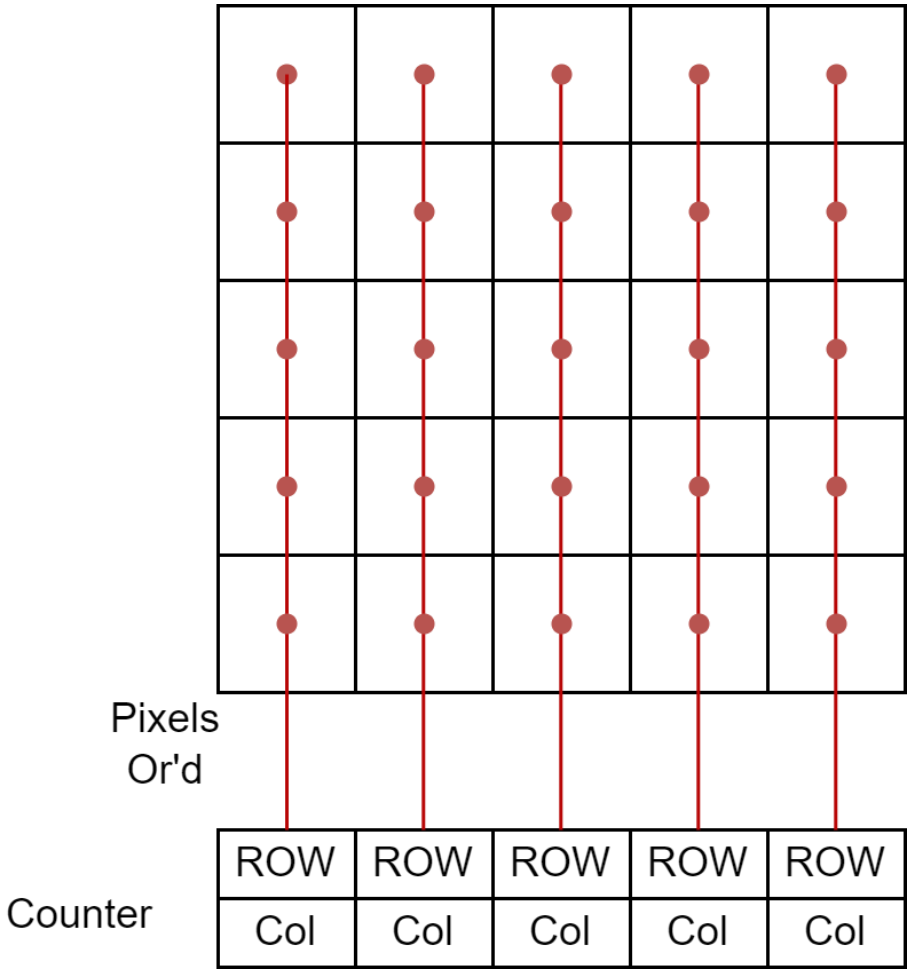


(b) The threshold dispersion before (red) and after (blue) tuning for the full MuPix10 matrix with an equivalent signal of 3000 e^-.

Source: https://arxiv.org/pdf/2012.05868.pdf

Astropix v1 - v3: Or'd Rows and Columns

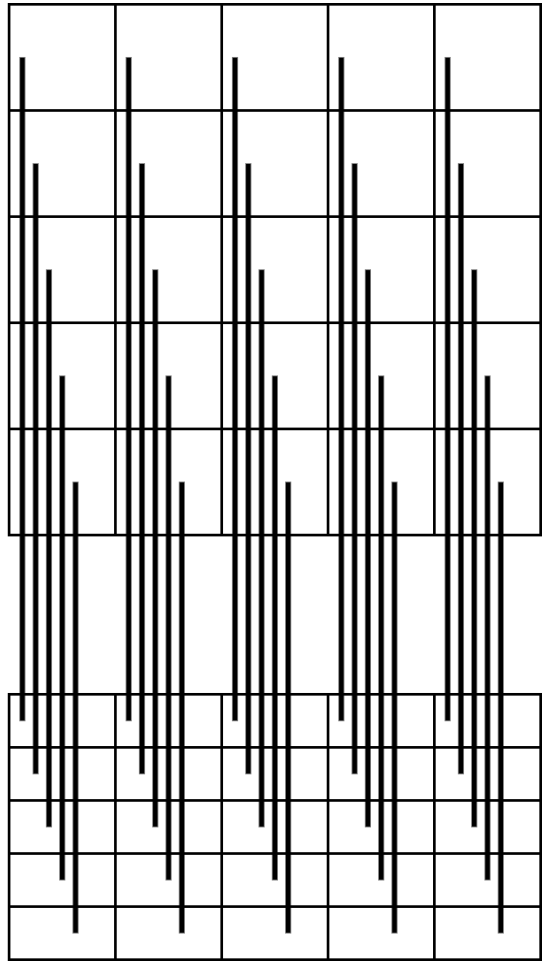
- Or'd Rows and Columns
- Advantages:
  - Low number of channels
- Disadvantages:
  - Identification problems with multiple hits in Row/Col
  - High bus capacitance → limits time resolution



Astropix v4: Individual Hitbuffers

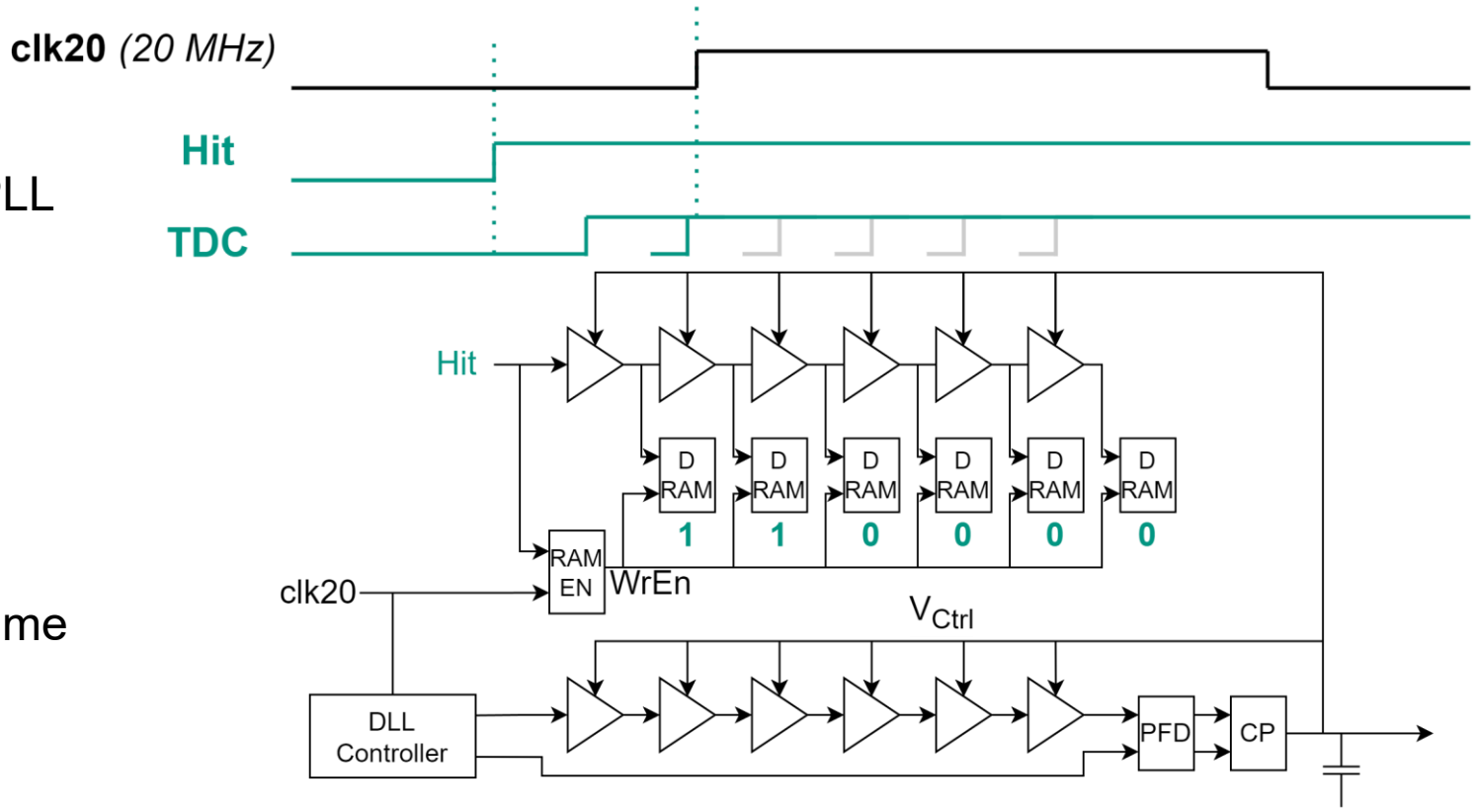
- Hits from every pixel are saved individually
- 16 x 13 pixel matrix -> 208 hitbuffers
- Similar to ATLASpix design

- Advantages:
  - No identification problems with multiple hits in Row/Col
  - Lower occupancy
- Disadvantages:
  - Occupies larger chip area



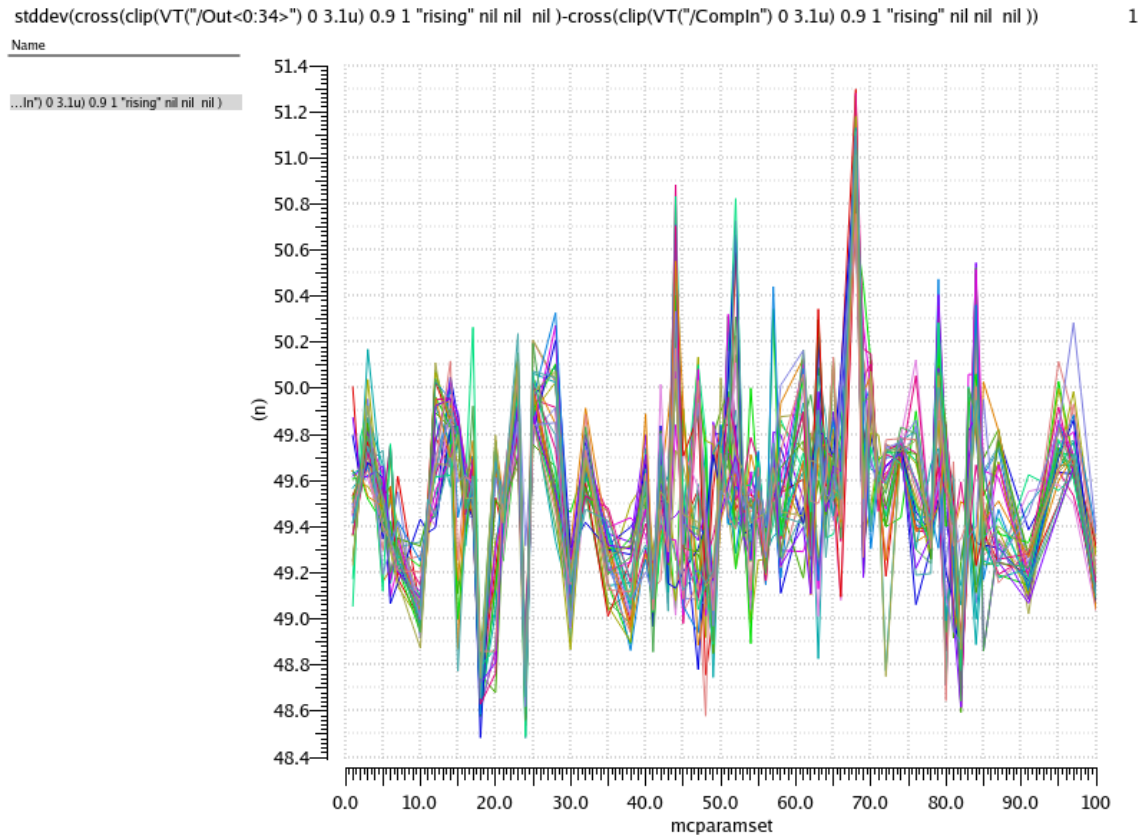
AstroPix Hitbuffer

- Coarse 20 MHz timestamp saved on leading and trailing edge of a hit
- 20 MHz clock generated by internal PLL
- Each Hitbuffer contains priority logic, DRAM and TDC
- Global DLL stabilized Flash TDC measures time from hit edge to next rising clock edge
- Resolution ~3ns
- No static power, will idle most of the time average power dominated by leakage <100 nW



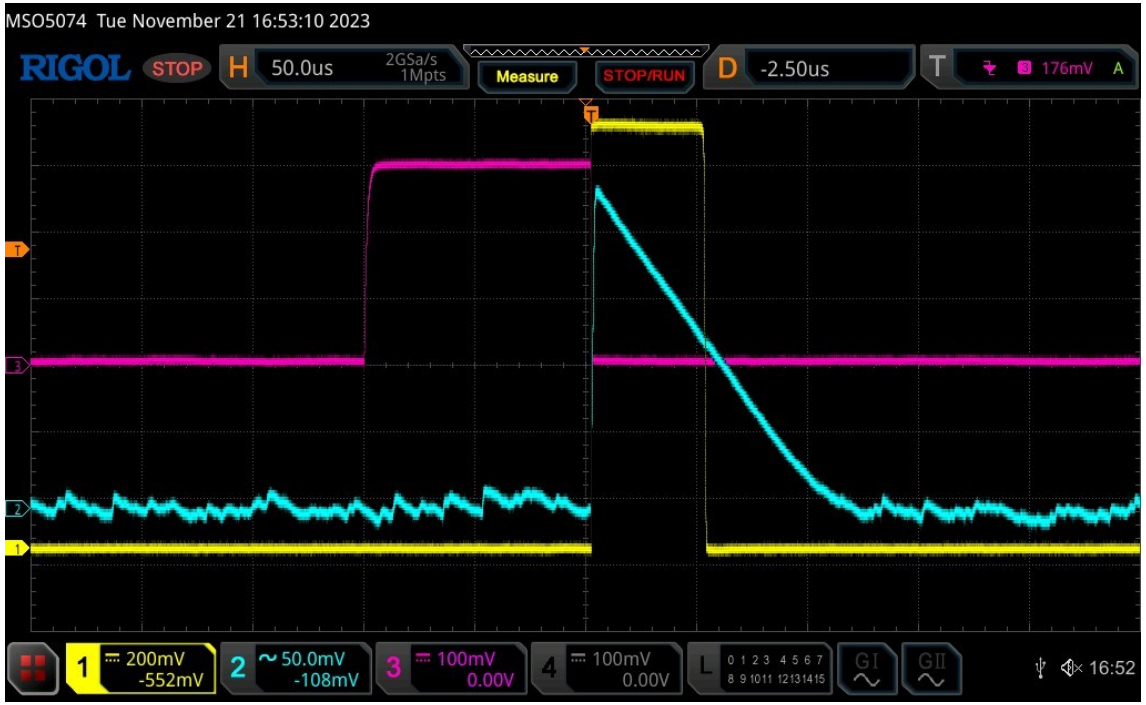
AstroPix Hitbuffer TDC

- TDC delay elements are stabilized by global DLL (1 per chip)
- Without calibration:
  - Mismatch: +/- 0.5 LSB
  - Temperature variation (10 to 50 °C): < 0.17 LSB
- Could be improved with automatic calibration
  - After each measurement, automatic measurement of a fixed time period, i.e. 1 clock cycle



First Functional tests

- Analog
  - Signal shape looks good
  - Less baseline noise
  - Hitbus works
- Breakdown (Okmetic 370 Ohm-cm)
  - -380V
- Digital with internal PLL
  - Injection 4 pixels enabled
  - Hits can be properly decoded
  - TS1 and TS2 timestamps (20 MHz rising/falling edge) look good
  - TDC currently not working
- Digital Power
  - 4x decrease to ~3mW
    - 0.65 mW leakage
    - 0.38 mW LVDS receiver
    - ~2 mW digital logic

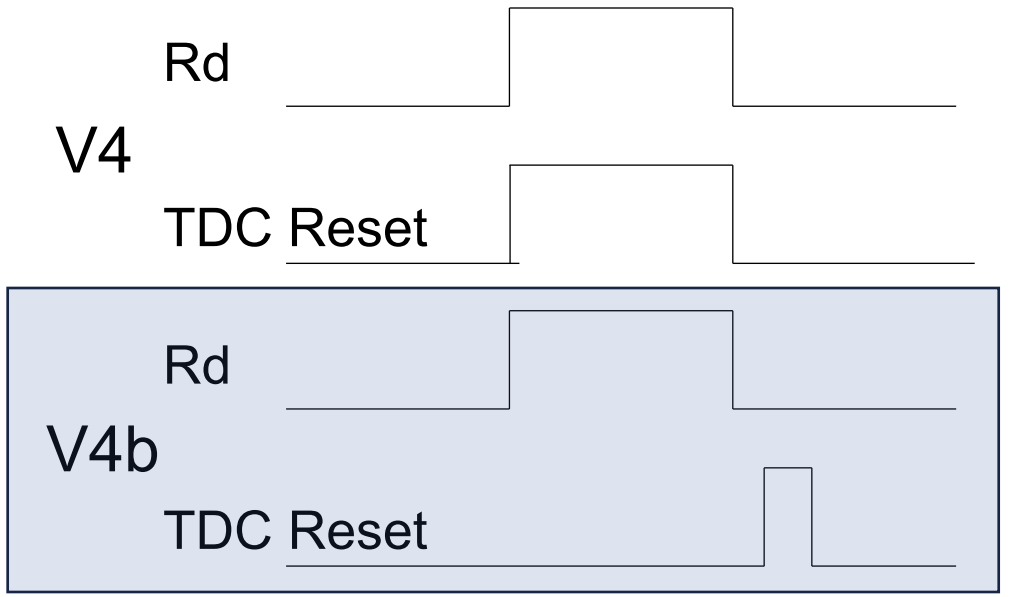


	id	payload	row	col	ts1	tsfine1	ts2	tsfine2	tsneg1	tsneg2	tstdc1	tstdc2	ts_dec1	ts_dec2
0	0	7	3	6	14538	5	14445	5	0	0	0	0	97177	97718
1	0	7	0	0	14539	4	14395	2	1	1	0	0	97175	97939
2	0	7	11	6	14539	4	14398	1	1	1	0	0	97175	97953
3	0	7	0	6	14539	4	14399	4	1	1	0	0	97175	97960

$$P_{VDD} = 1.8\,\mathrm{V} \cdot 1.65\,\mathrm{mA} = 2.97\,\mathrm{mW}\ (\mathrm{V3{:}}\ 12\,\mathrm{mW})$$

DLL and TDC

- DLL
  - DLL seems to work
    - Sometimes gets stuck after configuration -> 4mA current draw on VDD
    - This is expected, after reseting locks again
  - Not a DLL problem -> Timing problem in TDC control
  - TDC control logic restarts to early
    - Basically resets at the same time as bits are read out
  - TDC bits therefore always 0
  - Will be fixed in V5



AstroPix QSPI

- AstroPix2 digital: 2x5 Byte
  - Each per Col/Row
    - 8b Header
    - 8b col/row
    - 8b TS
    - 16b ToT

- AstroPix4: 1x8 Bytes
  - 8b Header (5 bit ChipID, 3 bit Payload)
  - 6b Row
  - 6b Col
  - 2x 18b TS
  - 2x 4b TDC

Commands

bits

7	6	5	4	3	2	1	0
Command			Chip Address				

BIT	FIELD	DESCRIPTION
[4:0]	Address	Requires 20 single addresses - 0x00 - 0x14 : Single addresses - 0x15 - 0x1F : Reserved - 0x1D: Invalid - 0x1E: Broadcast
[7:5]	Command	8 Commands: - 0x01 - NOCMD / IDLE - 0x02 - Routing: dispatch addresses - 0x03 - Shift Register Config

Readout

- Wait for interrupt signal low
- Toggle SPI clk to read out

AstroPix4 Summary

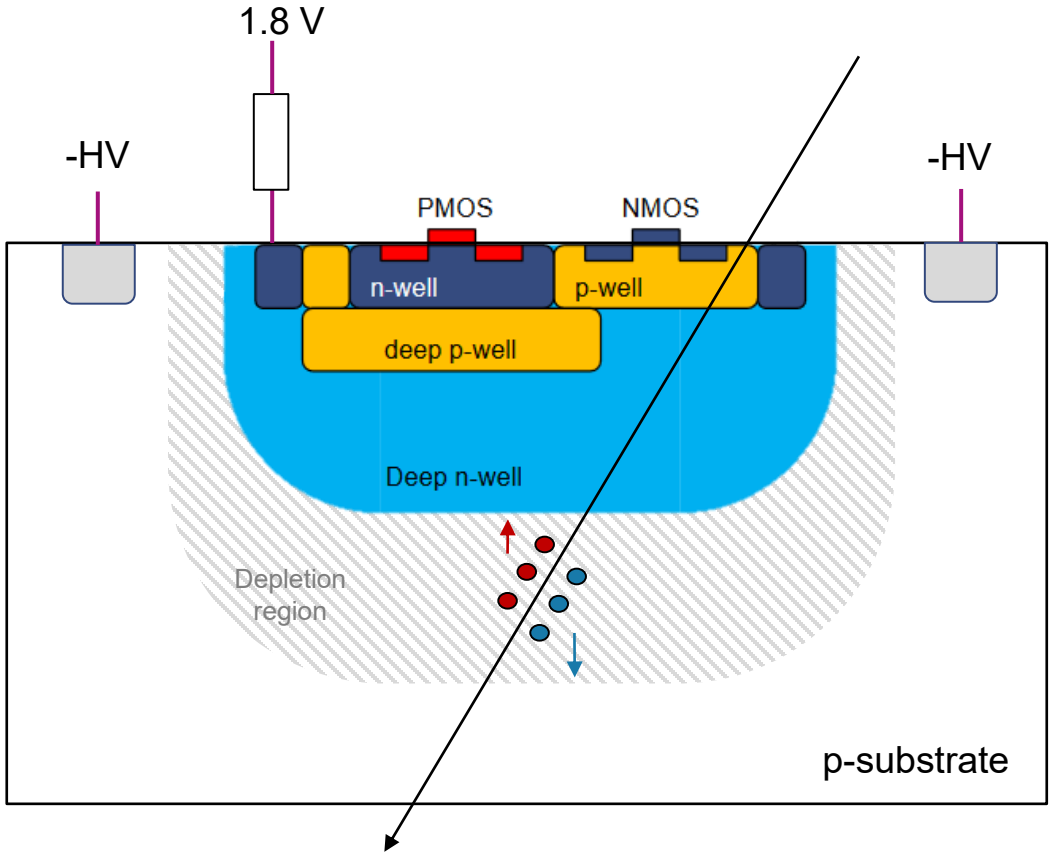
- AstroPix4 received in September 2023, first test in Nov 2023
- Reduced digital power
- Per pixel readout works
- TDC problem identified and understood
- Breakdown voltage promising

- Outlook on further measurements
  - Breakdown voltage measurements with HiRes wafers
  - Time resolution measurements
  - TuneDAC characterization

Backup

Introduction – HV-CMOS

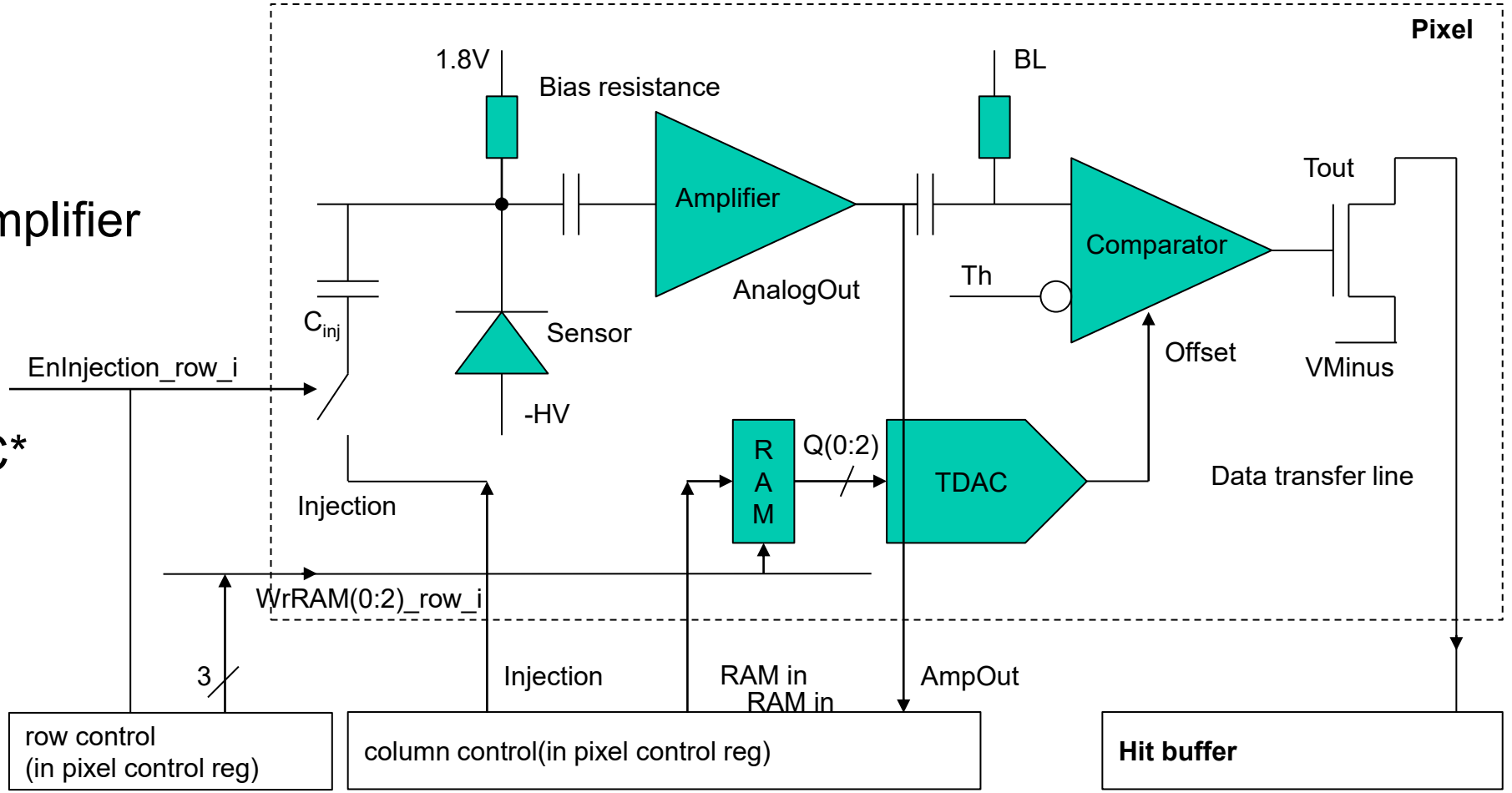
- Charged particles or photons generate electron-hole pairs in depletion region of the sensing diode formed by deep n-well and p-substrate
- Separated by strong electric field
- Electrons drift to charge-collecting deep n-well
- Deep n-well contains shallow wells for electronics
- **High-Voltage CMOS Active Pixel Sensor (HVMAPS)**



AstroPix4: Analogue Part

Pixel contains:

- Sensor diode
- Charge Sensitive Amplifier (CSA)
- Comparator
- Threshold tune DAC*
- RAM for tune bits*



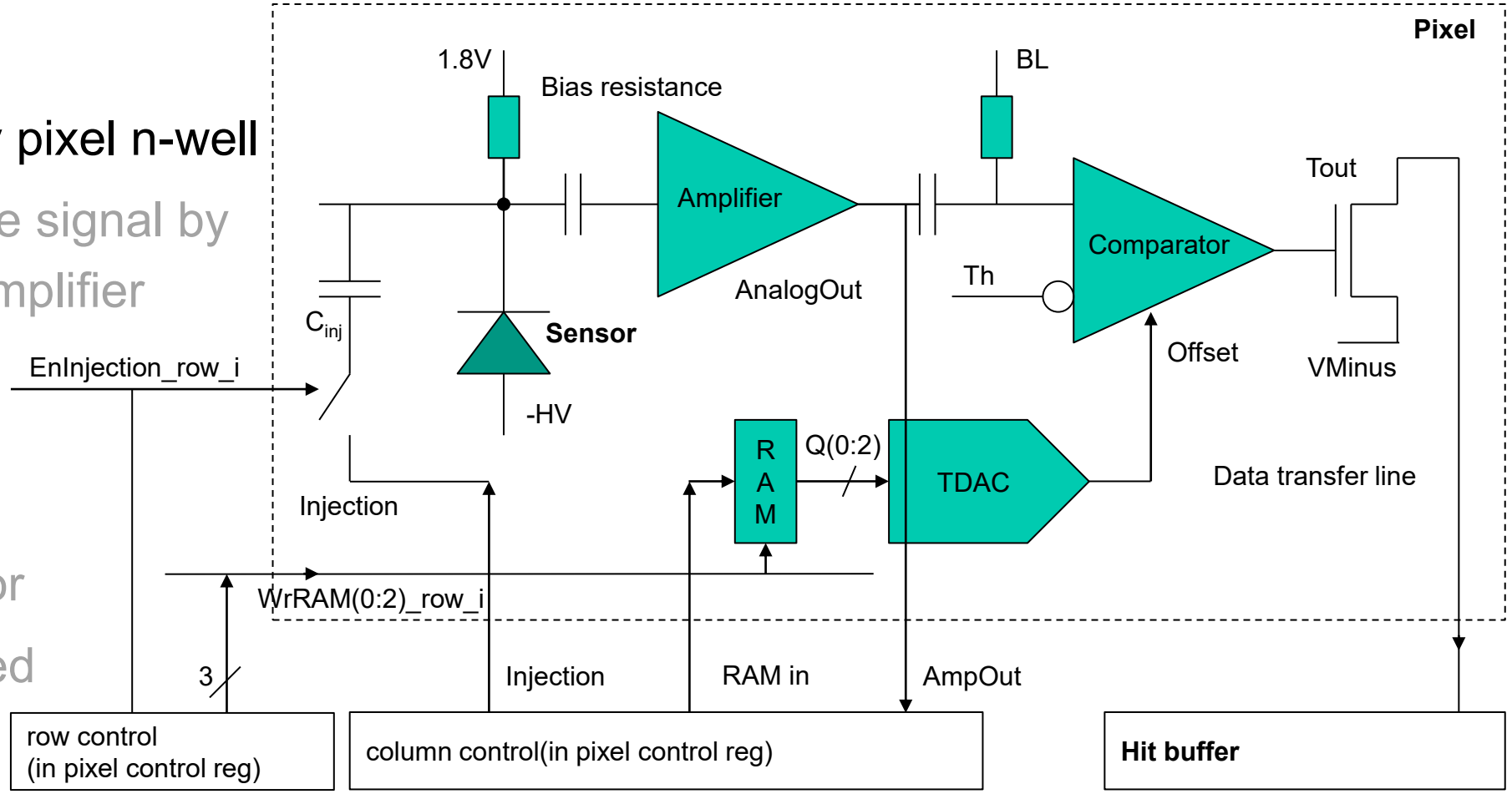
*placed in the periphery

Source: Ivan Perić

AstroPix4 : Analogue Part

Working principle:

1. Charge collected by pixel n-well
2. Converted to voltage signal by Charge Sensitive Amplifier
3. Analog voltage pulse shaped and converted to digital signal by comparator
4. Hit information stored in hit buffer



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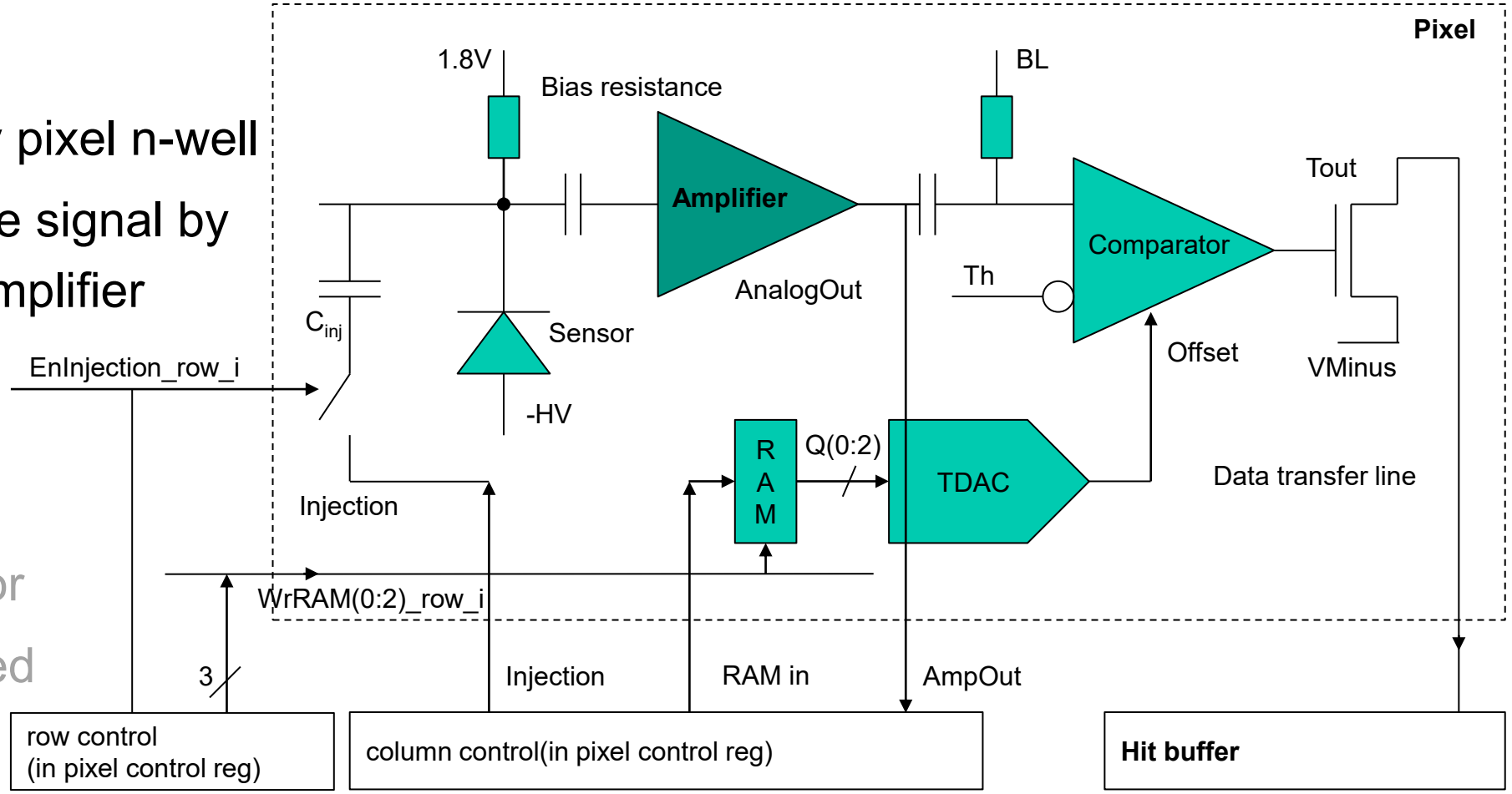

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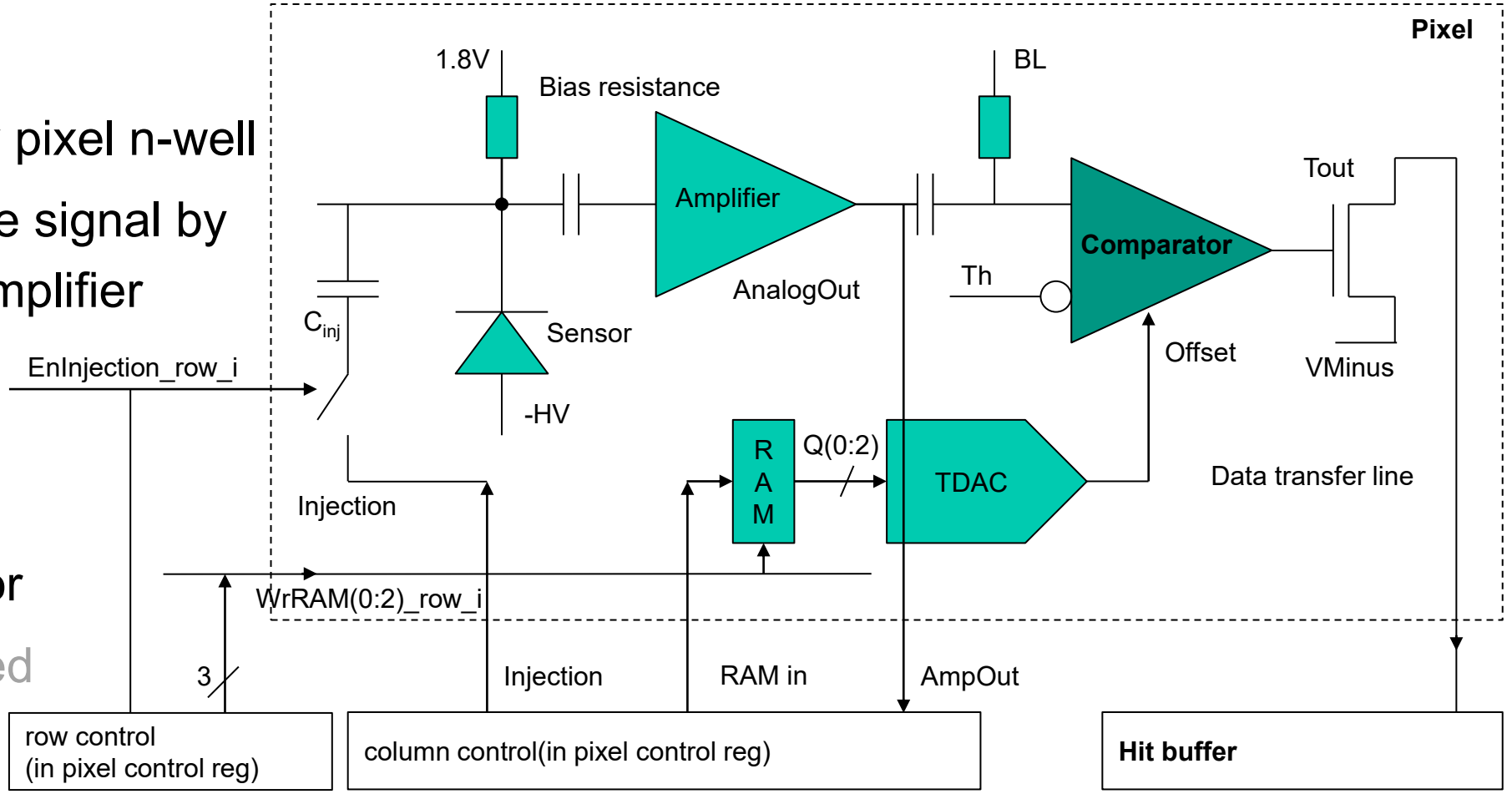

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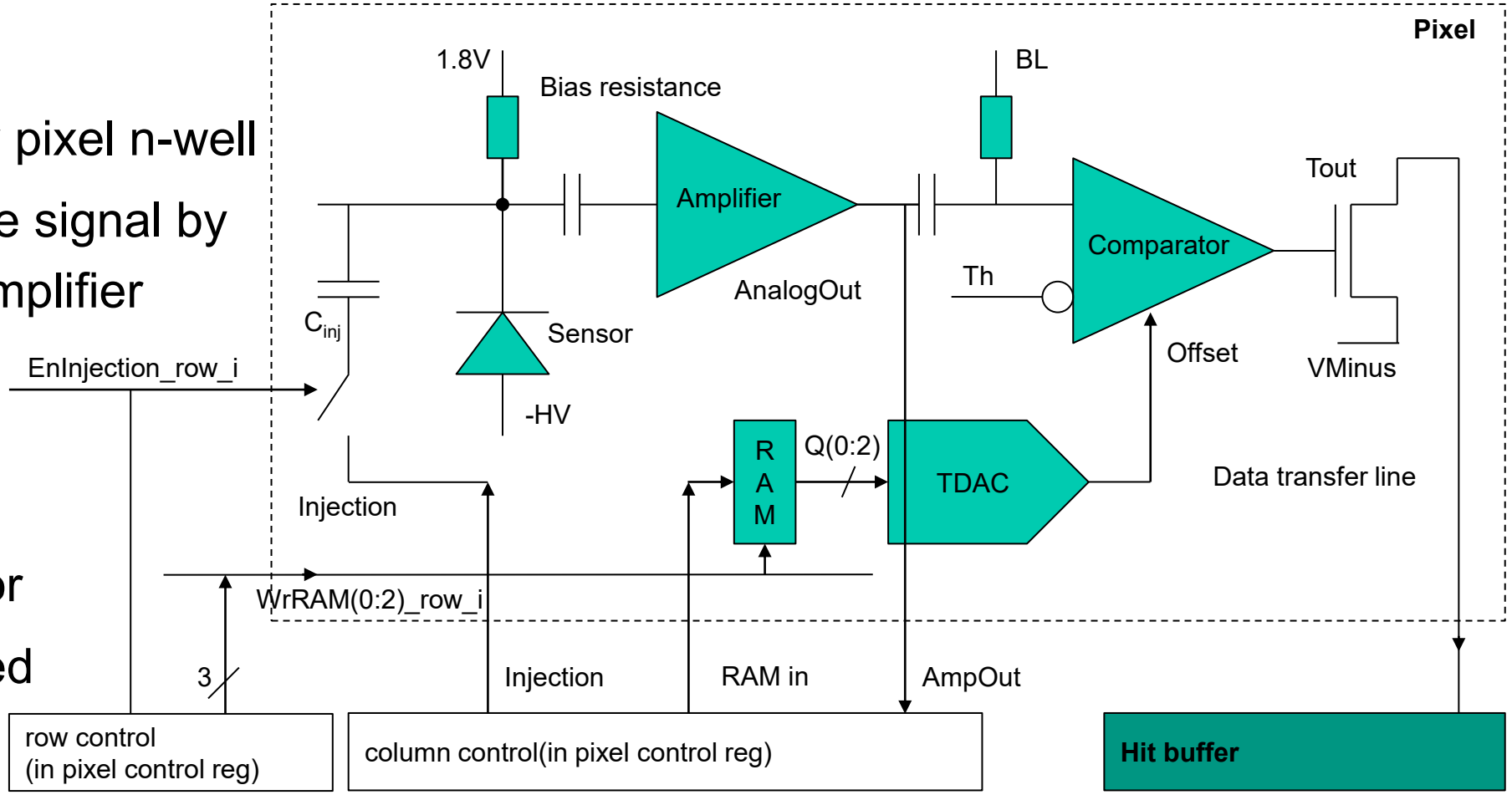

Source: Ivan Perić

Readout logic

- Controlled by state-machine (FSM)
- Working principle:
  - Priority Logic: Data from highest active Hitbuffers in every column are loaded into EoCs
  - FSM goes trough all loaded columns and writes the data into async FIFO
  - If FIFO is not empty, interrupt goes low
  - DAQ toggles the SPI clock, which initiates FIFO readout via QSPI Interface
  - From the outside perspective i.e. the DAQ, no difference to older AstroPix version, same protocol just different payload size