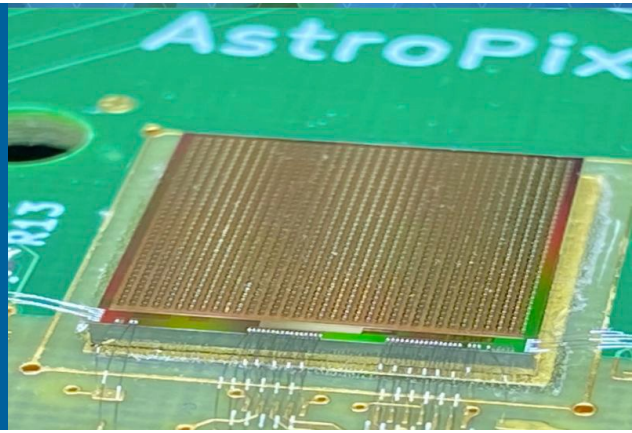
ASTROPIX: DESIGN DISCUSSIONS



JESSICA METCALFE

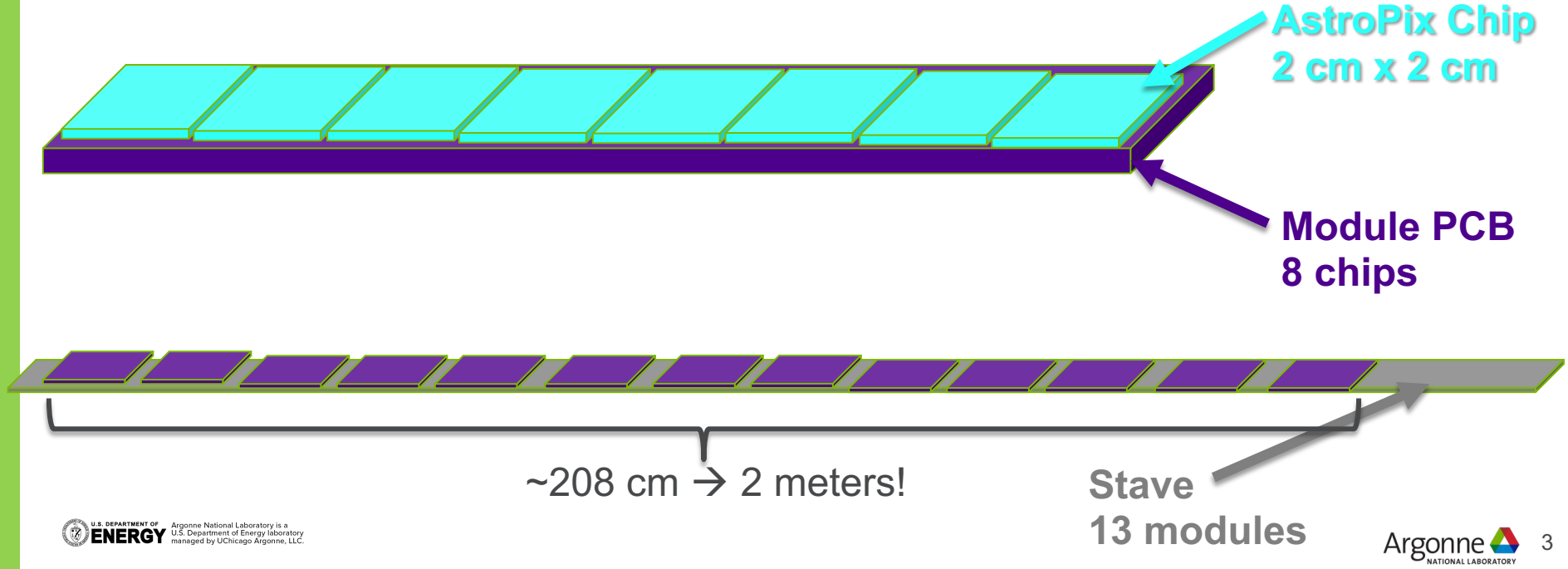
January 10, 2024
EIC Users Collaboration Meeting

OVERVIEW

- A few points have come up where a solution **might** be best found by modifying the AstroPix chip design
- We would like to introduce those topics today have some preliminary discussion
- If needed, we may ask people to do some small homework that may enable us to take a decision
- Tomorrow we have another session to go over the homeworks and have the remaining discussion
- Also, if there are any other open points or concerns, this is a good time to bring it up
- We hope that by the end of the workshop we can say what, if any, design changes we want to implement in AstroPix
    - Or at least identify what work needs to be done to take a decision

DATA TRANSMISSION

Q: Do we need differential receiving/transmission drivers for a chip that is 2 meters away from the FPGA readout board? i.e. how far can we currently reliably transmit the data/command signals? Can we bypass a bad or noisy chip in a module?



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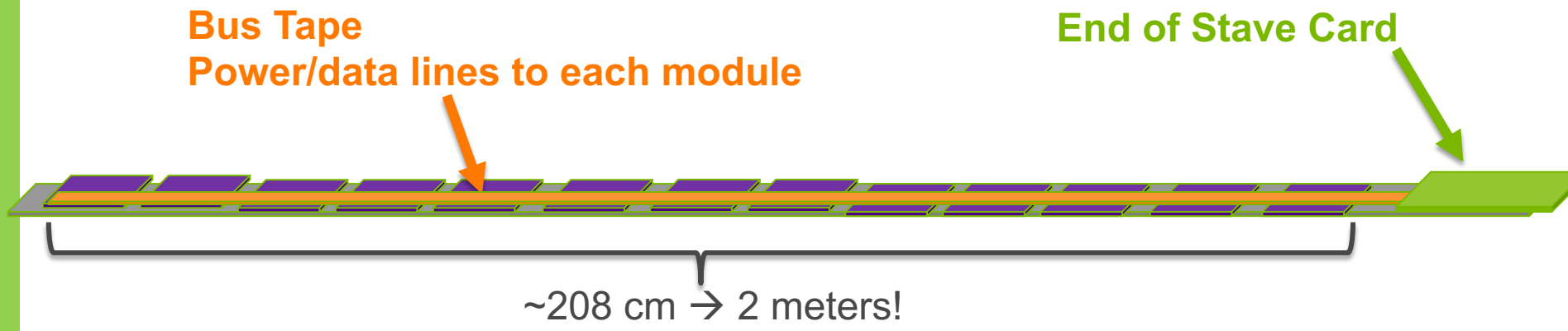
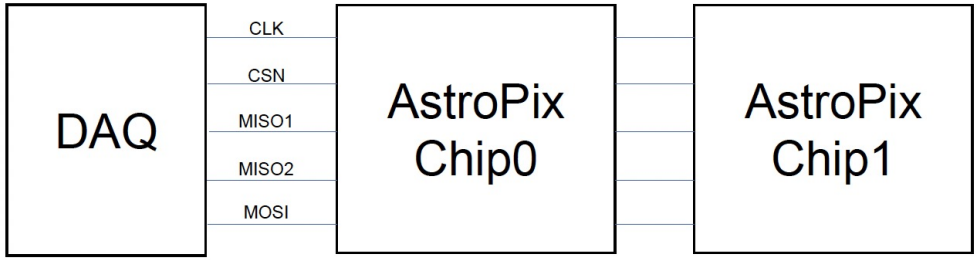


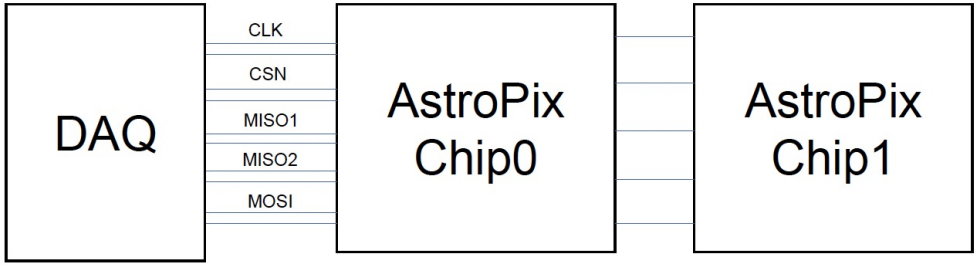
SPI Data Transmission

- **Current/V4 Implementation**
  - Completely single-ended communication
  - **Protocol**
    - 1 Byte Header (5 bit ID, 3 bit payload length)
    - 7 Byte Data
- **Plans for V5**
  - Differential LVDS-compatible signals to DAQ
  - Differential drivers/receivers only enabled in first chip in each row to reduce static power
  - Short chip-to-chip connections still single ended
  - **Good compromise between signal integrity and power consumption**
  - **Protocol**
    - **2 Byte Header** (min. 7 bit ID)
    - 7 Byte Data

V4



V5



SPI Chain Reliability

- High probability
  - Noisy pixels
    - Pixels can be enabled/disabled individually
    - Does not disturb readout chain

- Low probability
  - Failure in the digital logic especially in the SPI interface
    - Could potentially disturb the entire chain or a part of it
    - During Operation: Bypass switches for SPI lines possible, but should not be controlled via SPI -> Second Control connection to the chip needed -> Use existing Shift Register Interface?
    - After Manufacturing: Wafer level testing -> Implement scan chain?

INPUT POWER REGULATION

Q: How stable do each of the power inputs need to be on the chip? Do we need power regulation? What is does the solution look like to have power regulation on the chip? What does the solution look like to have power regulation on the module PCB or bus tape?

Power

- Especially analog circuits connected to VDDA and VSSA are susceptible to noise
- Usually DC-DC step-down converters are used together with low noise linear regulators

- On-chip regulator
  - Advantages
    - Simpler module design

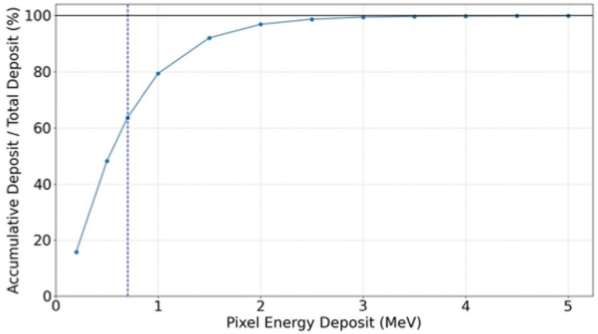
- Off-chip regulator
  - Advantages
    - No additional chip design complexity
    - One regulator can supply several chips
    - Higher efficiency due to lower dropout voltage of commercial off-the-shelf LDOs

DYNAMIC RANGE (SPECIFIC TO EIC)

Q: How difficult/risky is it to modify the dynamic energy range to be more specific to the EIC physics performance?

Facts:

- AstroPix specifications for 20 keV – 700 keV
- above 700 keV the signal amplitude saturates making an energy measurement from that pixel difficult
- Still get the yes/no hit info and the ~max amplitude indicates that the energy is ‘greater than or equal to’ instead of ‘equal to’



Accumulative energy deposit to the total energy deposit for 2 GeV electrons.

- About 63% of the energy deposit was made through hits with deposit < 700 keV
- hits with deposit < 3 MeV contribute to 99% of the total energy deposit

Q: What is the impact on physics performance?

Dynamic Range

- Amplifier is optimized for high dynamic range required by AMEGO-X 20 - 700 keV (EIC ~3 MeV)
- Closed loop gain V ~ Q/C
  - High gain seen by small signals
    - Small feedback capacitance ~500aF
  - Low gain seen by large signals
    - 10 fF VNCAP
    - Configbit to disable low gain mode by disconnecting the capacitor through a switch
- **If needed an additional capacitor and switch could be added for EIC**
    - Low risk, circuits already tested in AstroPix2-4
- **Can we even absorb 3 MeV with 500um depletion?**

SUMMARY

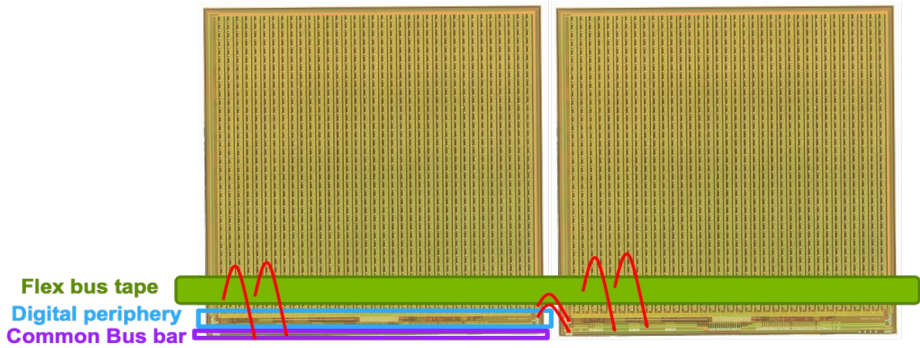
- Conclusions?
- Homework items to discuss tomorrow?

BACKUP

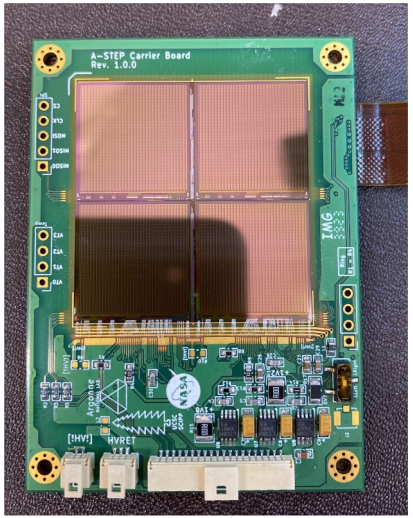
ASTROPIX: NEXT STEPS

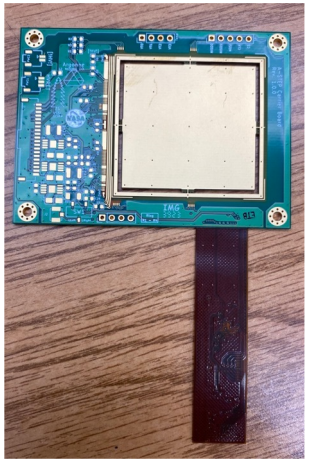
Several Features to Validate Performance:

- Daisy chain readout
  - Multi-chip module read-out board
  - Check for data loss/max occupancy
- Sensor efficiency between pixels, depth
  - Preparing for edge-TCT measurements
  - Charge collection efficiency
- Flex bus tape design
- DAQ development
- Update previous results with v4
  - Test Beam
  - Irradiation: SEU, LET, Total Dose



- Command/Power is distributed through a bus tape
- Wire bonded from bust tape
- Signals are digitized and routed out to the neighbor chip via wire bonds



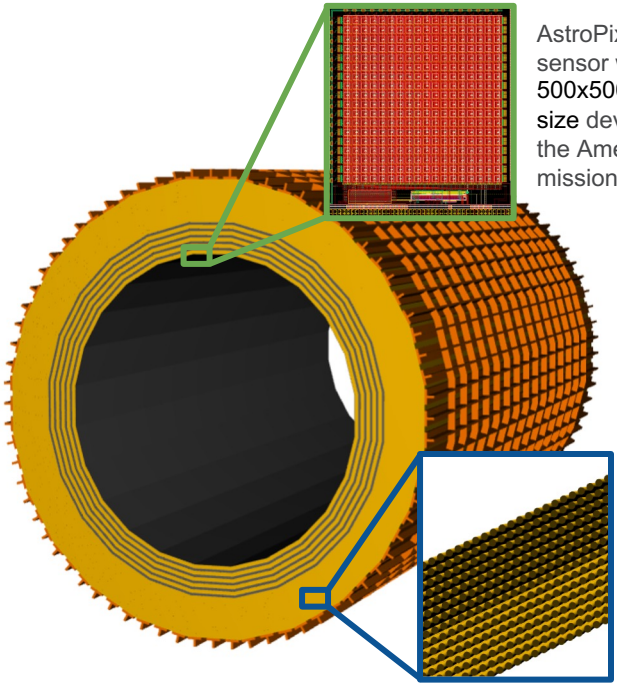


BIC

Addressing the unique challenges for the barrel region in ePIC

Hybrid concept: 6(4 now) layers of Astropix interleaved with the first 5 Pb/ScFi layers, followed by a large volume with the rest of the Pb/ScFi layers

- ✓ Deep calorimeter (21 X_0) but still very compact at ~ 40 cm
- ✓ Excellent energy resolution (5.2% /$\sqrt{E}$ ⊕ 1.0%)
- ✓ Unrivaled low-energy electron-pion separation by combining the energy measurement with shower imaging
- ✓ Unrivaled position resolution due to the silicon layers
- ✓ Deep enough to serve as inner HCal
- ✓ Very good low-energy performance
- ✓ Wealth of information enables new measurements, ideally suited for particle-flow
- ✓ Makes the tracking MPGD layer behind the DIRC unnecessary



AstroPix: silicon sensor with 500x500μm^2 pixel size developed for the Amego-X NASA mission

ScFi Layers with two-sided SiPM readout

Thank You

USA

- Argonne National Laboratory
- NASA Goddard Space Flight Center
- Oklahome State University
- University of Connecticut
- University of California Santa Cruz

Canada

- University of Manitoba
- University of Regina
- Mount Allison University
- NSERC
- Canada Fund for Innovation

Korea

- Kyungpook National University
- Yonsei University
- University of Seoul
- Pusan National University
- Korea University
- Sungkyunkwan University
- Hanyang University
- Gangneung-Wonju National University

Germany

- Karlsruhe Institute of Technology
- University of Giessen

ePIC BIC Detector Subsystem Collaboration

AstroPix Collaboration:

- Hiroshima University
- Nagoya University

AstroPix Developments

AstroPix v1 - January 2021

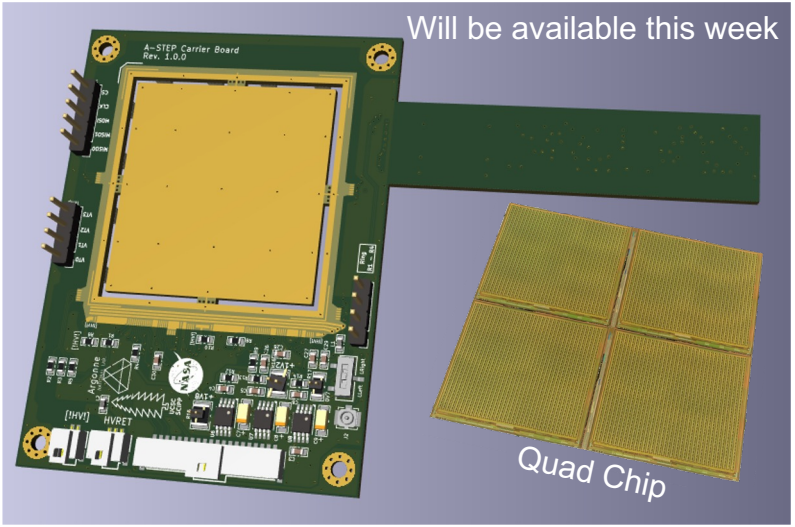
- 0.45 × 0.45 cm^2 chip, 175 µm pixel pitch
- 18 × 18 pixel matrix
- Power dissipation ~14.7 mW/cm^2

AstroPix v2 - December 2021

- 1 × 1 cm^2 chip with 250 µm pixel pitch
- 35 × 35 pixel matrix
- Hit identification with Row/Column readout
- Power dissipation ~3.4 mW/cm^2

AstroPix v3 - February 2023

- 2 × 2 cm^2 chip with 500 µm pixel pitch
- Power dissipation <1 mW/cm^2 (targeted)
- Timestamp clock 2.5MHz, ToT 200 MHz
- 10 byte data frame per hit



AstroPix v3 Quad-chip Carrier Board

AstroPix v4/v5

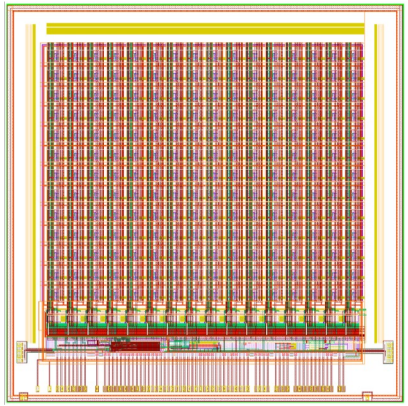
AstroPix v4 : Final design version will small size

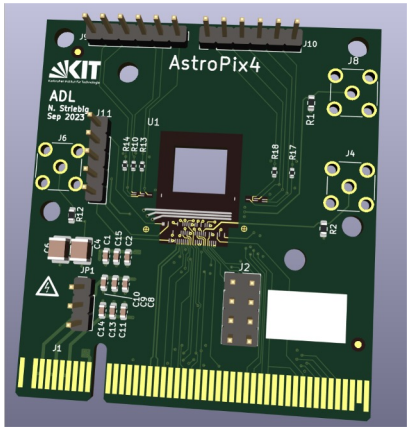
- Chip size 1 × 1 cm^2; Thickness 700 μm, V_{BD} ~ 400V
- Pixel pitch 500 μm with pixel size 300 μm, 16 × 16 pixel matrix
- Individual pixel readout with individual hit buffer
  - No identification issue due to ghost hits
- 3 Timestamps - 2.5MHz (TS), 20 MHz (Fine TS), and 16 bit Flash TDC
  - Fast ToT and Timestamp with 3.125 ns time resolution
- TuneDACs - Pixel-by-pixel threshold tuning and pixel masking
- Daisy Chain readout - pass hits to next chip through QSPI
- Self-triggered (reads out active hits)

AstroPix v5 : Full size final design

- No planned design changes
- Fix any bug from v4
- Full size chip - 2 × 2 cm^2, pixel pitch 500 μm,
- 35 × 35 pixel matrix → 1225 hit buffers

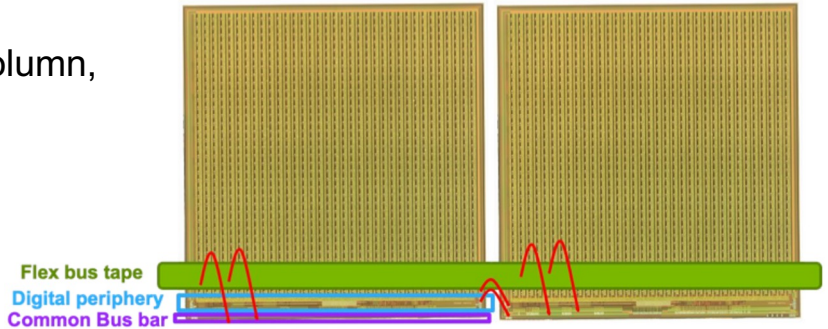
AstroPix v4

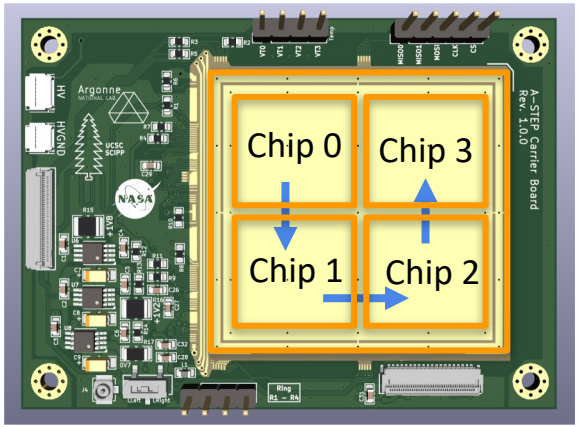




AstroPix Readout

- 8 bytes data per hit - header (chipID, payload), row/column, timestamp, ToT
- SPI I/O daisy chained - chip-to-chip signal transfer
  - signals are digitized & routed out to the neighboring chip using 5 SPI lines via wire bond
- Power/Logic I/O distribution on the module (through a bus tape)
  - 4 power lines (LV, HV), ~20 Logic I/O (SPI, clk, timestamp, interrupt, digital Injection, etc.)
  - HV, VDDA/VDDD(1.8V), VSSA(1.2V), Vminuspix(0.7V)
  - power distribution can be controlled using voltage regulators
  - mostly part of end of the stave services
- Data will be received by FPGA at the end of stave
  - FPGA aggregates data before sending off-detector
- Low heat load at chip, only cooling of end of the stave card
- Operational temperature for AstroPix is at room temperature and considered to be operated at 22 ℃





AstroPix v3 quad-chip carrier board
- Demonstrate required services
- Daisy chaining

AstroPix at ePIC

Low Rates

- The expected hit rate for **all imaging layers together** is well below < 3 × 10^7 Hz
- This translates to a maximum hit rate per tracker stave (1 x 104 chips) < 36 kHz

Zero-suppression below threshold 20 keV (4 × noise floor) well suited for EIC electromagnetic showers

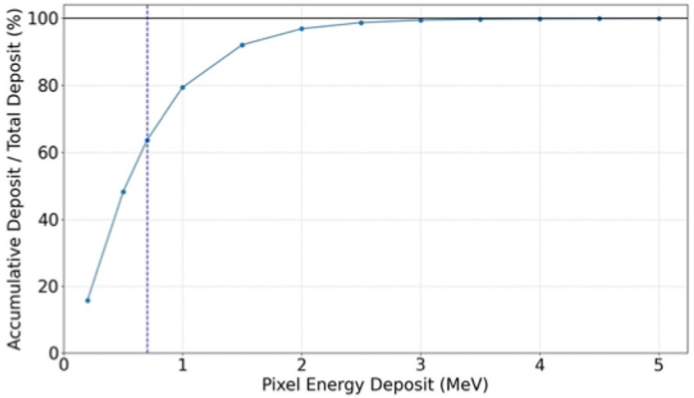
Timing requirement: 3.125 ns (v4/v5) - **driven by 10 ns bunch crossing**

Low Ionization radiation dose and neutron flux

- The maximum **ionizing radiation dose < 1 kRad/year** for the barrel region
- Max neutron flux - order of **10^9 $n_{equivalent}/cm^2$ per year**

Dynamic range (see plot for 2 GeV e^-)

~ 3 MeV



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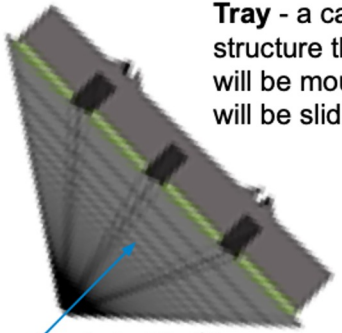
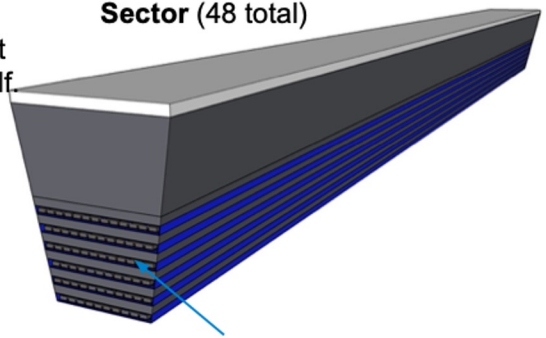
AstroPix Assembly



Tray - a carbon fiber structure the staves will be mounted on. It will be slid into a shelf.

AstroPix **Stave**
Consists of 1 x 108 chips with the support structure, “turbofanned”
AstroPix **Module**
Subset of chips

Sector (48 total)



Shelf - a carbon fiber structure that is glued to the Pb/ScFi layers, that we will slide trays with AstroPix staves on.

*The designs presented on these slides are not final but for illustration only

Module Strategy

- QC testing with wafer probing + Module and stave level QC testing and tuning
- “Baseline” model of Modules on Stave
  - Module - 8 single chips
  - Stave - 13 Modules - 104 chips
  - 12 or 14 Staves per AstroPix layer per Calorimeter Sector
  - Total 249600 chips
- All staves are identical and gets combined in a separate production step
- Data transmitted to end of the Stave card using flex base tape
- Institutions - ANL, GSFC/NASA, KIT ,UCSC, Korea, Oklahoma State