AstroPix Questions EIC Workshop

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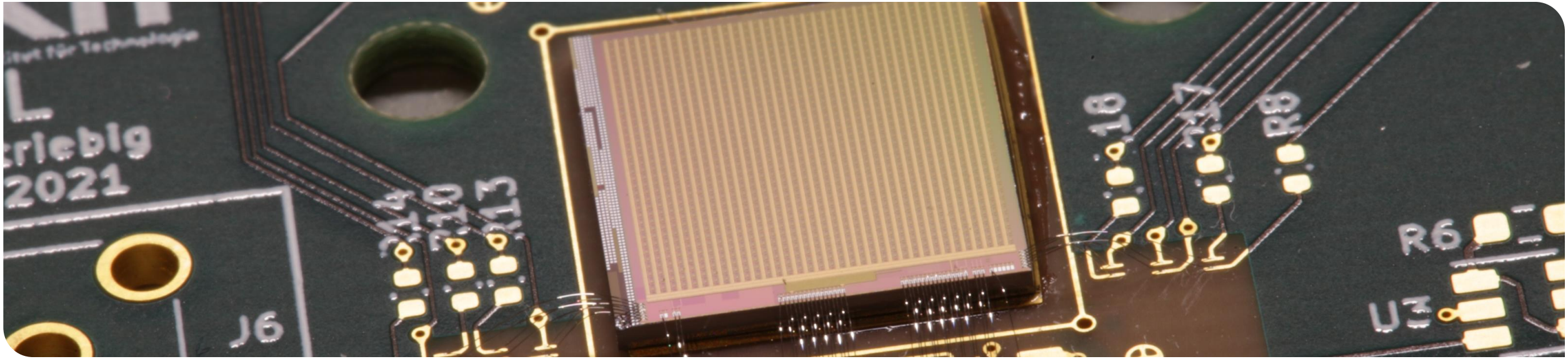
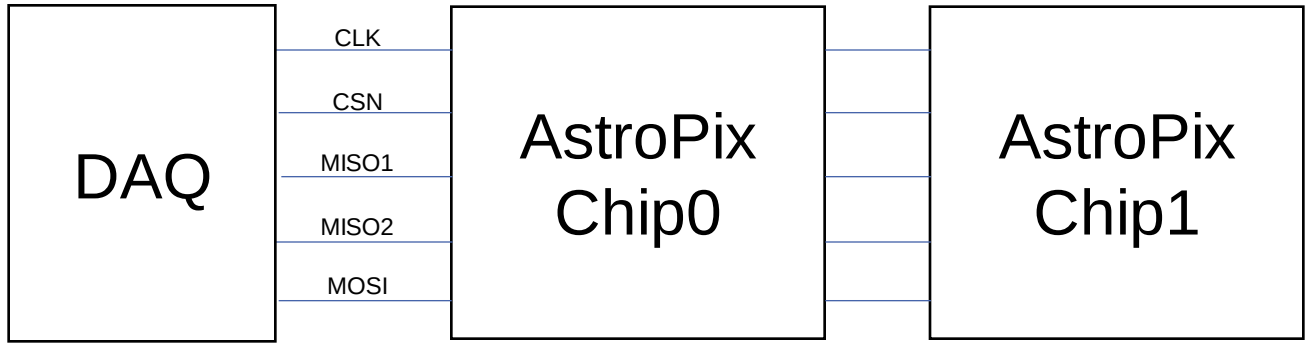


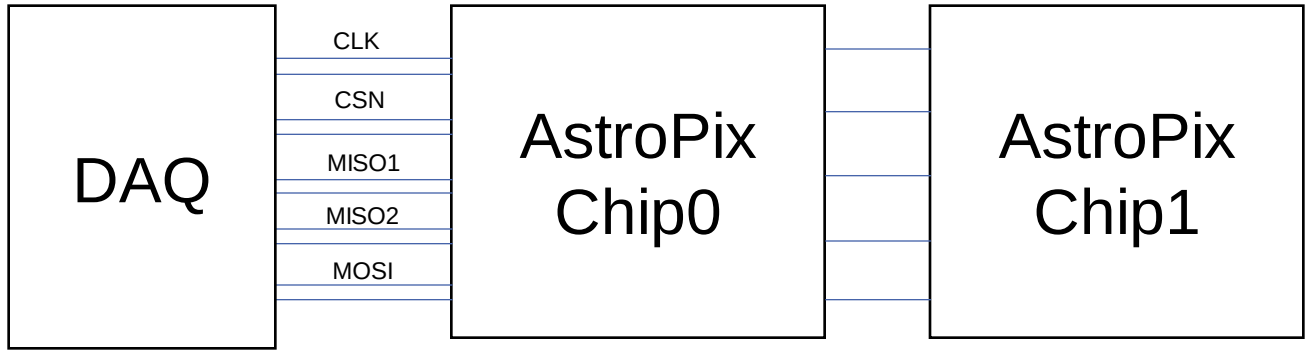
SPI Data Transmission

- **Current/V4 Implementation**
  - Completely single-ended communication
  - **Protocol**
    - 1 Byte Header (5 bit ID, 3 bit payload length)
    - 7 Byte Data
- **Plans for V5**
  - Differential LVDS-compatible signals to DAQ
  - Differential drivers/receivers only enabled in first chip in each row to reduce static power
  - Short chip-to-chip connections still single ended
  - **Good compromise between signal integrity and power consumption**
  - **Protocol**
    - 2 Byte Header (min. 7 bit ID)
    - 7 Byte Data

V4



V5



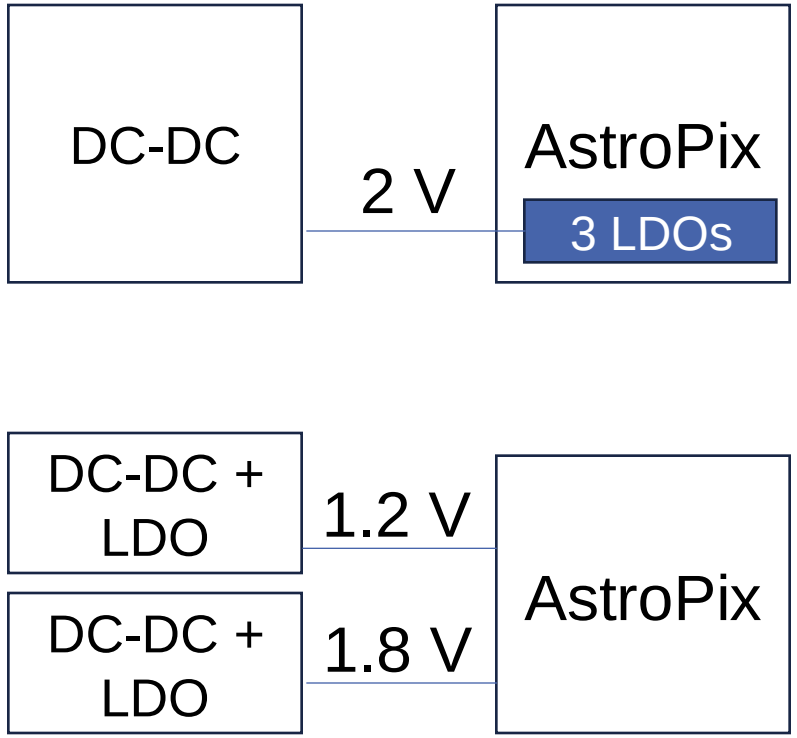
SPI Chain Reliability

- High probability
  - Noisy pixels
    - Pixels can be enabled/disabled individually
    - Does not disturb readout chain

- Low probability
  - Failure in the digital logic especially in the SPI interface
    - Could potentially disturb the entire chain or a part of it
    - Bypass switches for SPI lines possible, but should not be controlled via SPI -> Second Control connection to the chip needed -> Shift Register Interface?
    - After Manufacturing: Wafer level testing -> Implement scan chain?

Power

- Especially analog circuits connected to VDDA and VSSA are susceptible to noise
- Usually DC-DC step-down converters are used together with low noise linear regulators
- Voltages needed by the chip:
  - VDDA = 1.8 V
  - VSSA = 1.2 V
  - VDDD = 1.8 V
  - Vminuxpix = 0-1V
- On-chip regulator
  - Advantages
    - Simpler module design
- Off-chip regulator
  - Advantages
    - No additional chip design complexity
    - One regulator can supply several chips
    - Higher efficiency due to lower dropout voltage of commercial off-the-shelf LDOs



Integrated Voltage Regulator

- Could be based on MuPix/ATLASpix design
- Single 2 – 2.2V input from DC-DC on module to generate voltages internally
  - VDDA,VSSA = 1.8 V
  - VDDD = 1.8 V
  - Vminuxpix = 0-1V
- Option to use internal regulators or external supplies
- More design time needed
- Not guaranteed to work better than external solution

Power supply specifications

- Higher voltages than nominal are generally no problem as long as they don‘t exceed 1.95V
- Digital VDDD should work down to 1.62 V
- Lower VDDA and VSSA can have impact on performance
  - Reduced VDDA decreases amplifier output swing -> lower dynamic range
  - Characterisation with respect to different operating temperatures needed
- For impact of ripple and noise, characterisation is needed
  - As reference our lab supplies from Toellner (8733) are specified to 50 uV ripple

Dynamic Range

- Amplifier is optimized for high dynamic range required by AMEGO-X 20 - 700 keV
- Closed loop gain V ~ Q/C
  - High gain seen by small signals
    - Small feedback capacitance ~500aF
  - Low gain seen by signals
    - 10 fF VNCAP
    - Configbit to disable low gain mode by disconnecting the capacitor through a switch
- **If needed an additional capacitor and switch could be added for EIC**
    - Low risk, circuits already tested in AstroPix2-4
- **Can we even absorb 3 MeV with a 500um depletion?**