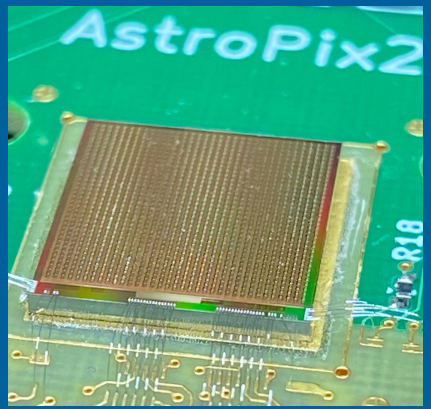
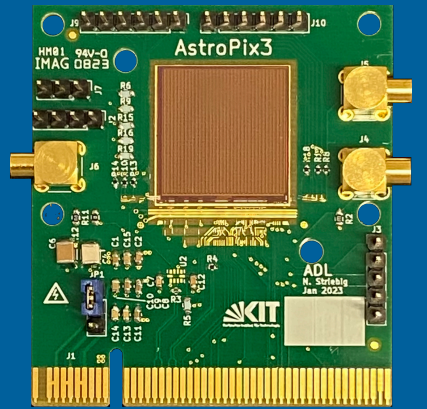
ePIC Collaboration Meeting - Jan 2024 (ANL)

Module Block Diagram



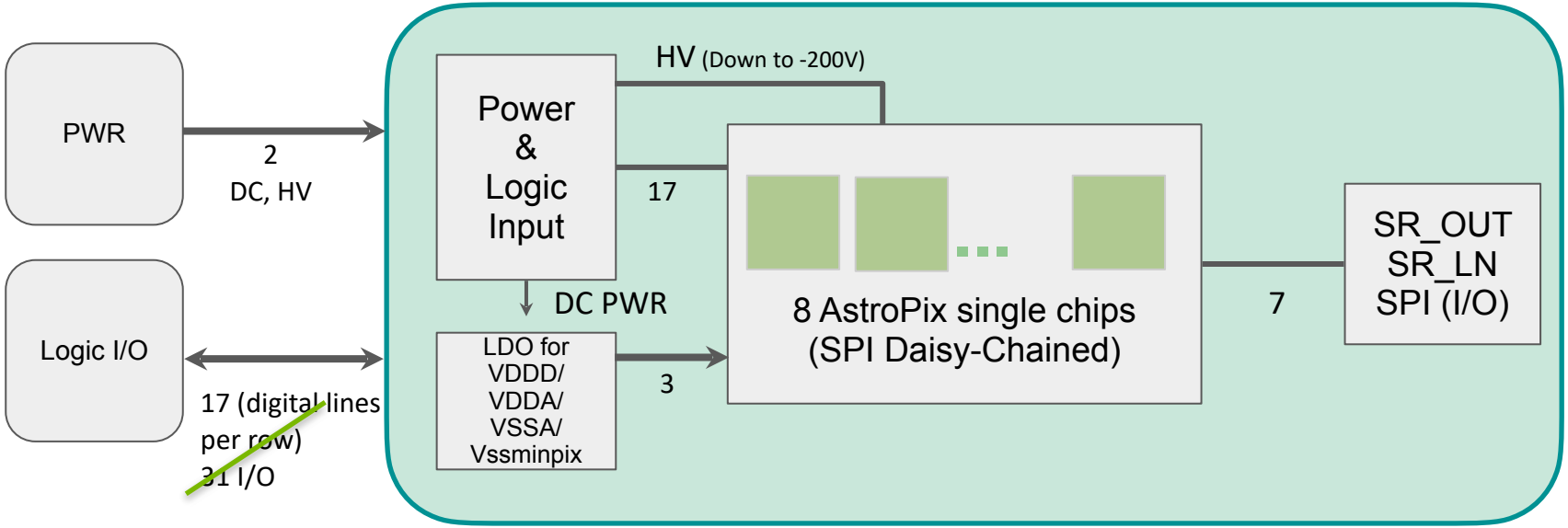


Manoj Jadhav
Argonne National Laboratory

Jan 10, 2024

Block Diagram

1. 8 chips are all daisy chained via SPI
2. WB connections through flex bus tape



- DC power -> VDDA/VDDD (1.8V), VSSA (1.2V), Vssminpix (0.7V), HV -> Do we want seprate out digital and analog?
- LDOs for DC power -> On module pcb or flex bus tape?
- SR_OUT, SR_LN, SPI_XXX -> 5 SPI lines, ~~Interrupt, 200 MHz Time-over-Threshold (ToT) clock~~
- ~~Each AstroPix quad-chip carrier board connector has a total of 17 digital lines which result in 31 I/Os at the FPGA after considering shared interface lines.~~

We don't need any digital I/O for the actual project -> only 5 SPI lines (interrupt is optional), 200 MHz is on chip in V4 (differential)

Block Diagram

- DC power -> VDDA/VDDD (1.8V), VSSA (1.2V), Vssminpix (0.7V), HV -> Do we want seprate out digital and analog?
- LDOs for DC power -> On module pcb or flex bus tape?
- SR_OUT, SR_LN, SPI_XXX -> 5 SPI lines, ~~Interrupt, 200 MHz Time-over Threshold (ToT) clock~~
- ~~Each AstroPix quad-chip carrier board connector has a total of 17 digital lines which result in 31 I/Os at the FPGA after considering shared interface lines.~~

We don't need any digital I/O for the actual project -> only 5 SPI lines (interrupt is optional), 200 MHz is on chip in V4 (differential)

Where power is coming from -> project provides power (The main power supplies in the experiment are in racks on a platform (South) and are about 20 m away. These are floating, low noise supplies, ground referenced at the detector.) These supplies have sense inputs that are wired all the way to the point of use and so compensates automatically for cable losses.

The potentials at the point of use are thus what you set/need.

Space on end-of-stave card -> we don't know

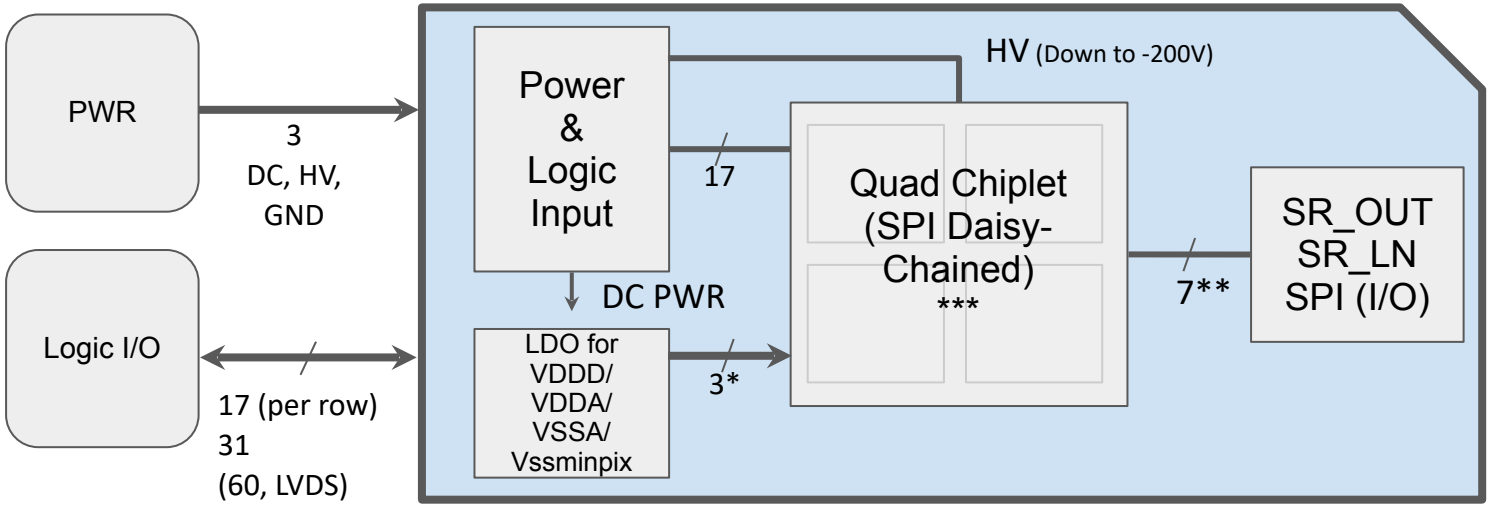
13-14 cm z-direction

Magnetic field -> 2T max

DC-to-DC converter

Thank you

Block Diagram



*VDDA/VDDD (1.8V)/VSSA (1.2V)/Vssminpix (0.7V)
** SR_OUT, SR_LN, SPI_XXX

1. Assumed 4 chips are all daisy chained via SPI
2. Upper 2 chip WB connections through flex bus tape

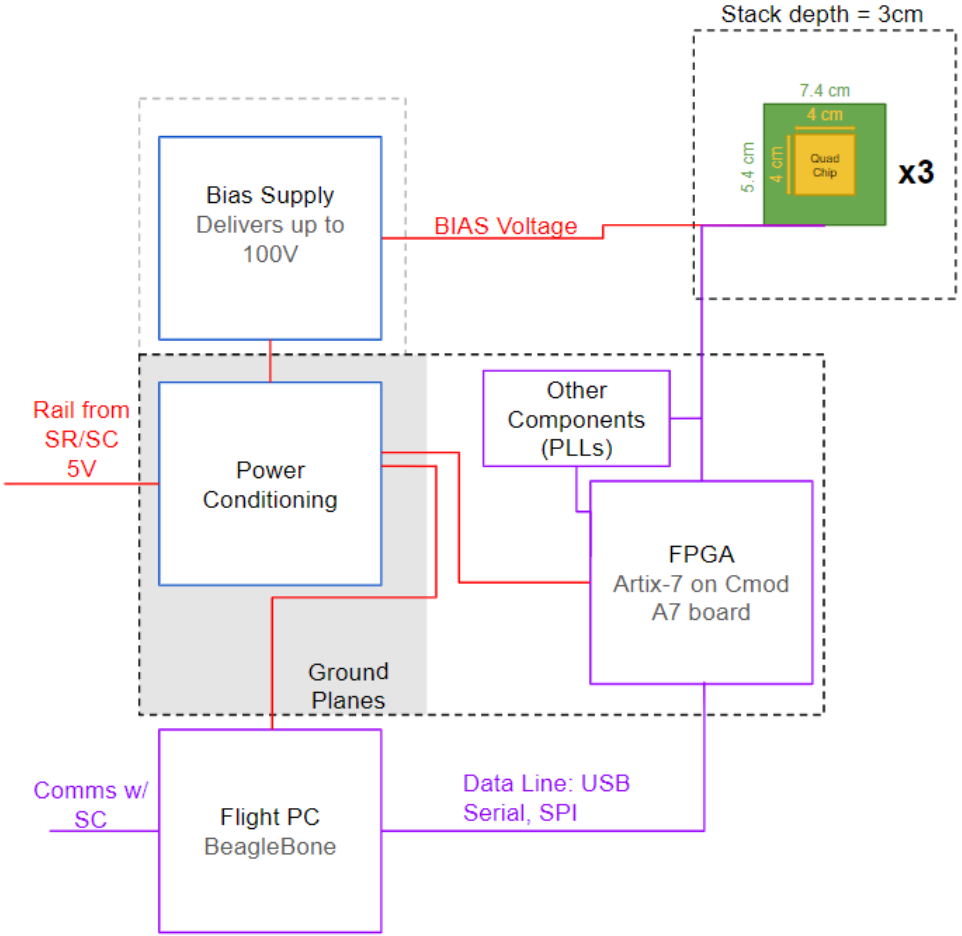
Block Diagram A-Step

Require trade studies for:

- FPGA
- Bias supply
- Power rail requirement
- Stack height
- Quality of power supplied by SR/SC (jitter, etc)
- Thermal requirements

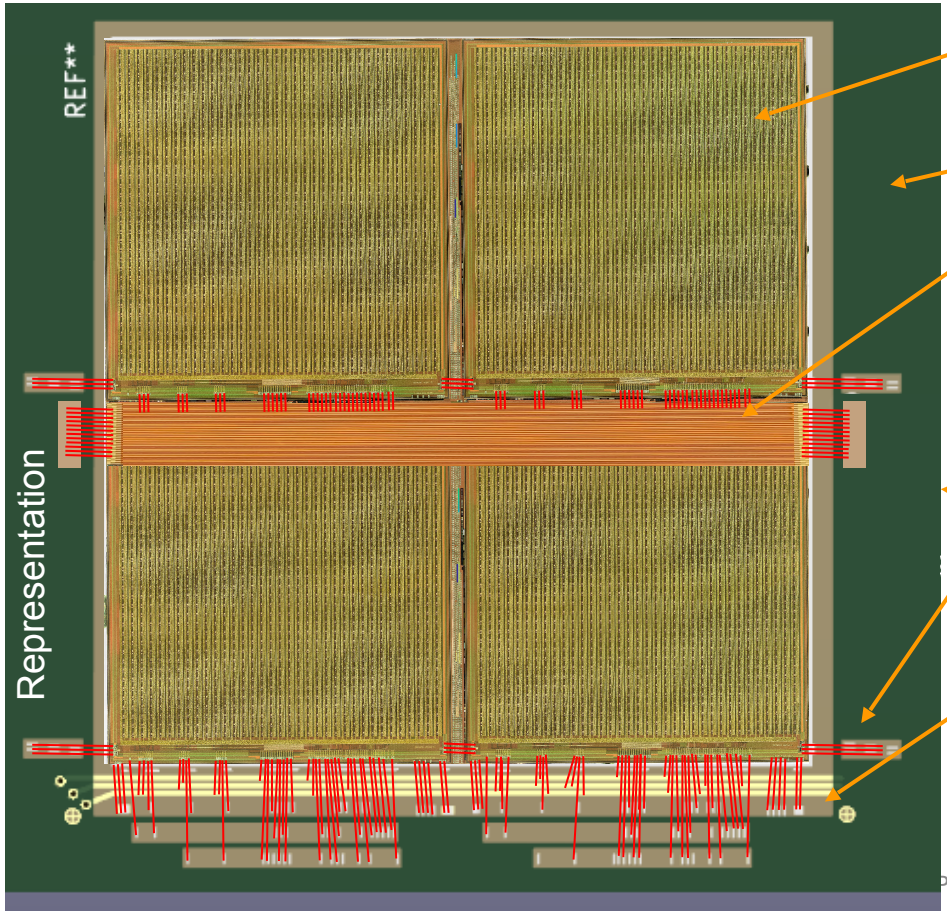
Development still in progress:

- Chip carrier boards (functionality and form factor)
- PLL integration
- Flight PC / SC communication



Quad-Chip Carrier Board

The Quad Chip
(mounting representation)



AstroPix V3
quad-chip

Chip Carrier PCB

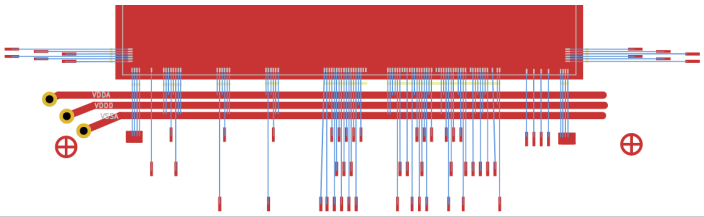
Flex bus tape glued on the top of quad chip (allows wire-bond connection to top row chip pads)

Glue Recommendations:
SE4445-CV or
ARALDITE 2011

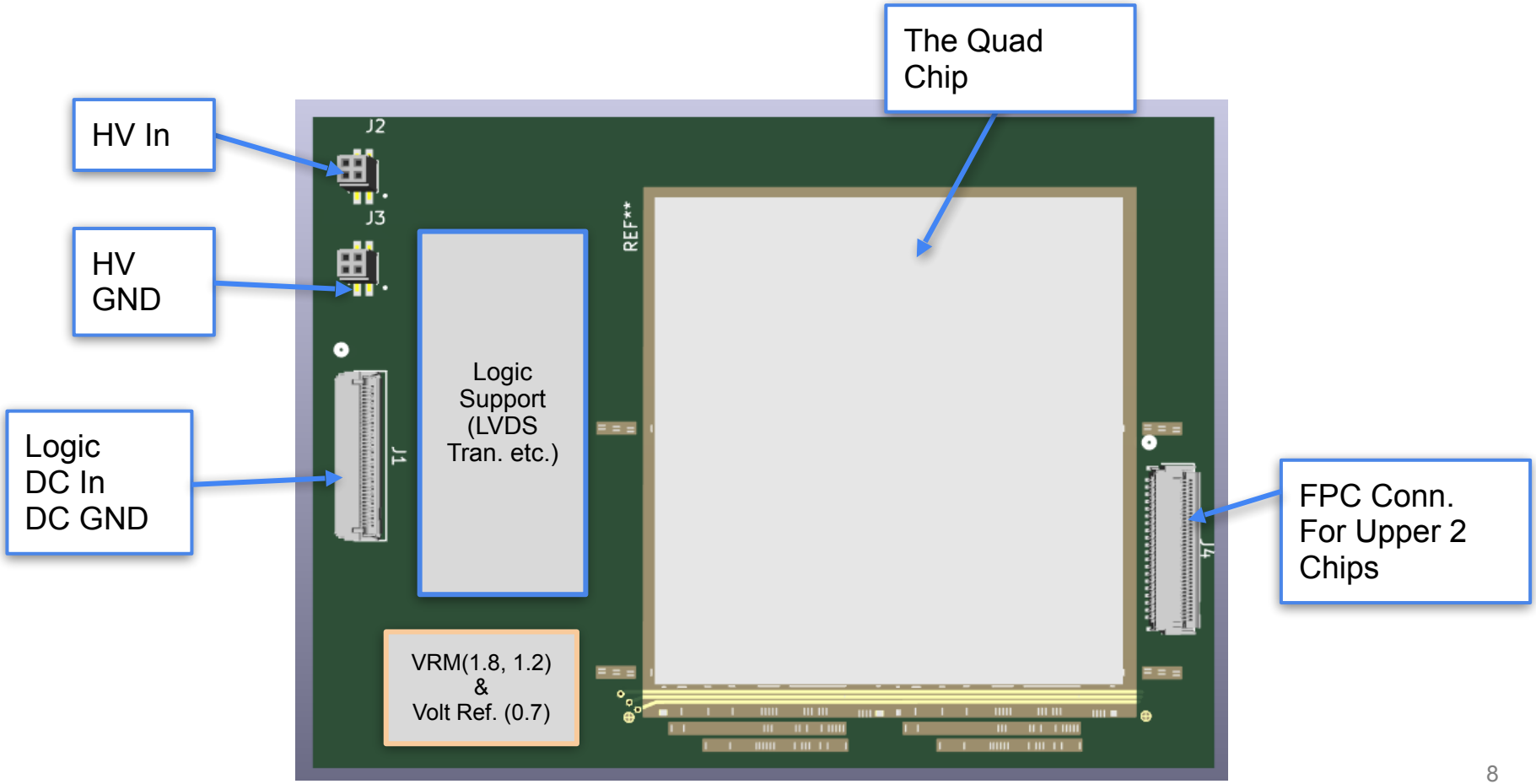
Daisy-chained SPI bus

Wire-bond pads

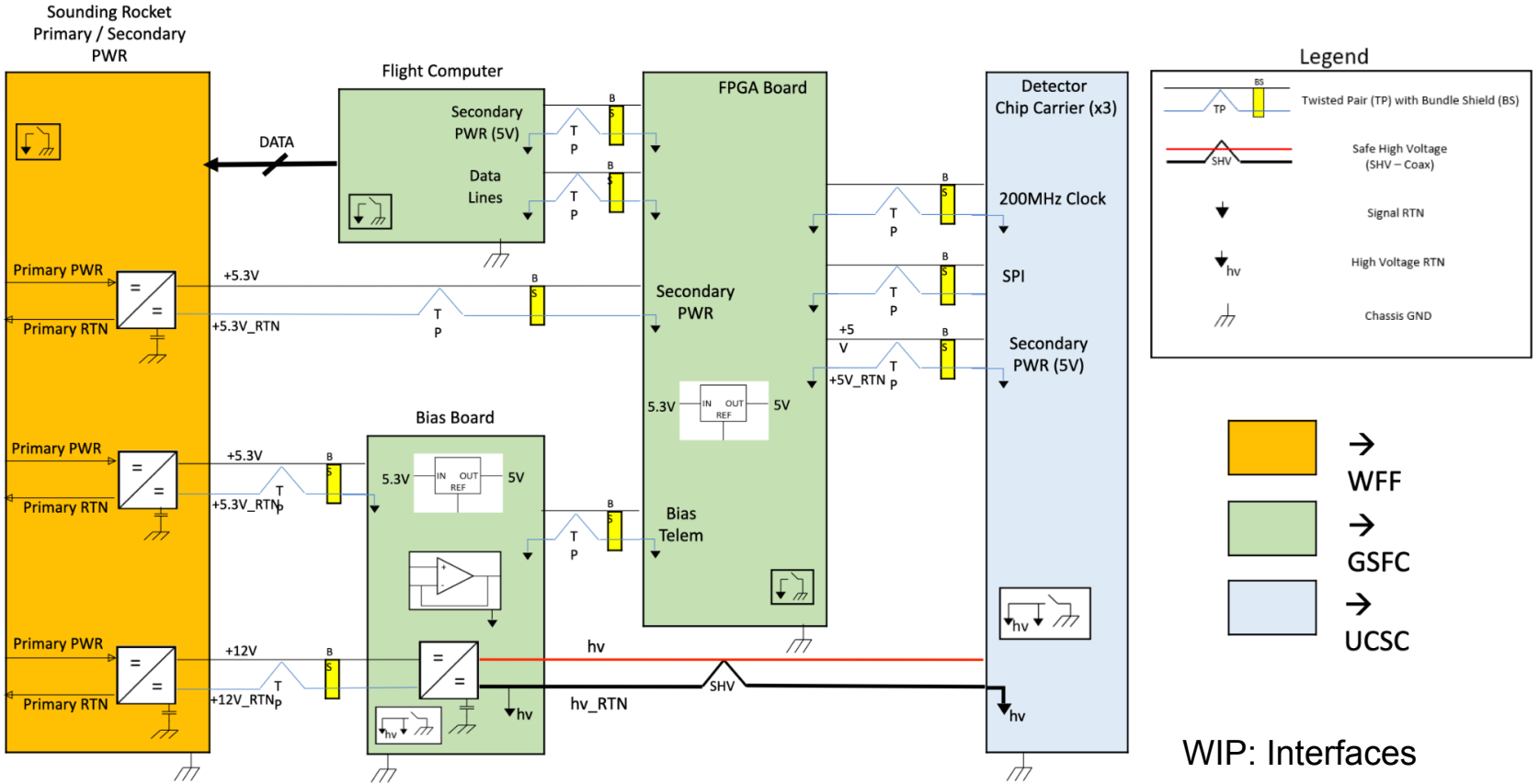
Wire-bond plan for V3 single chip



Quad-Chip Carrier Board

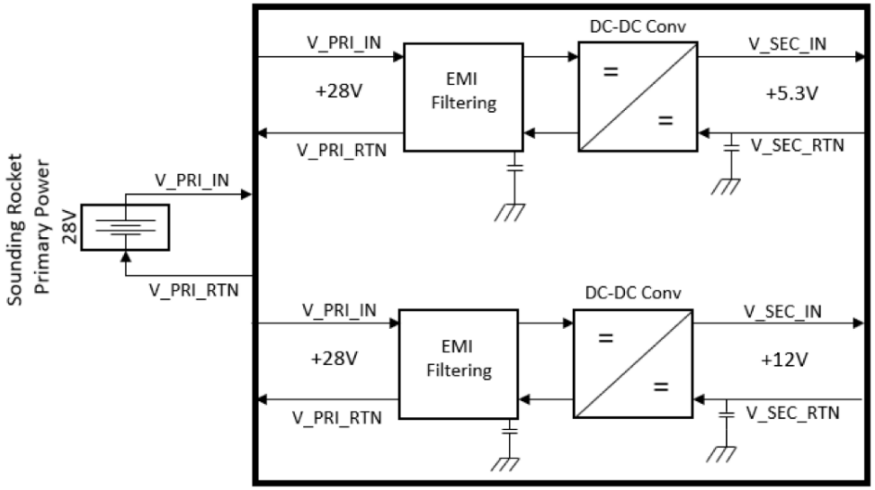


Grounding Configuration for Power Board

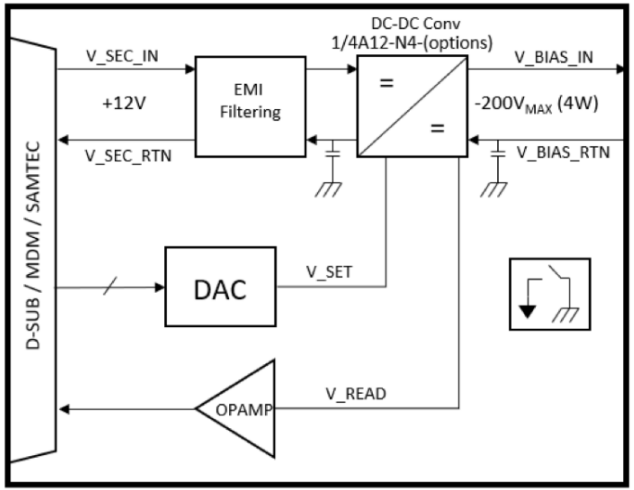


Power Boards

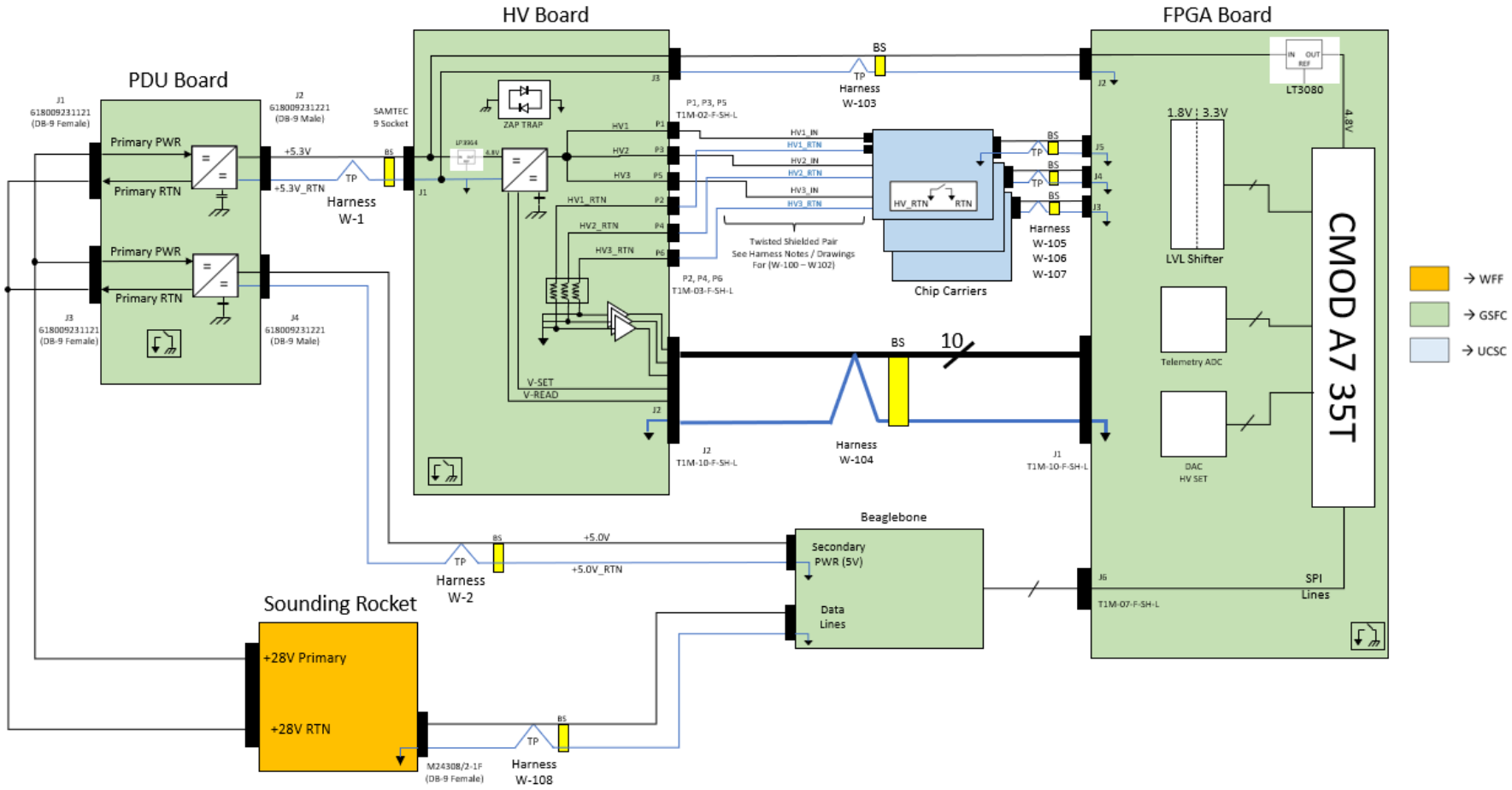
- Primary Power (28V) provided by sounding rocket.
  - Will provide +5.3V and +12V for the instrument



- Detector Bias Board
  - Bias needs: -150V to -175V
    - Max current draw is 3mA, 525mW per detector



Power Boards


HV Board
FPGA Board
PDU Board
Primary PWR
Primary RTN
Primary PWR
Primary RTN
+5.3V
+5.3V_RTN
Harness
W-1
SAMTEC
9 Socket
ZAP TRAP
HV1
HV2
HV3
HV1_RTN
HV2_RTN
HV3_RTN
V-SET
V-READ
BS
TP
Harness
W-103
HV1_IN
HV1_RTN
HV2_IN
HV2_RTN
HV3_IN
HV3_RTN
Twisted Shielded Pair
See Harness Notes / Drawings
For (W-100 – W102)
HV_RTN
RTN
Chip Carriers
Harness
W-105
W-106
W-107
LT3080
1.8V ; 3.3V
LVL Shifter
Telemetry ADC
DAC
HV SET
CMOD A7 35T
10
Harness
W-104
Beaglebone
Secondary
PWR (5V)
Data
Lines
+5.0V
+5.0V_RTN
Harness
W-2
SPI
Lines
Sounding Rocket
+28V Primary
+28V RTN
Harness
W-108
→ WFF
→ GSFC
→ UCSC