Argonne NATIONAL LABORATORY

ASTROPIX TRACKER PRODUCTION MODEL

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U.S. DEPARTMENT OF ENERGY
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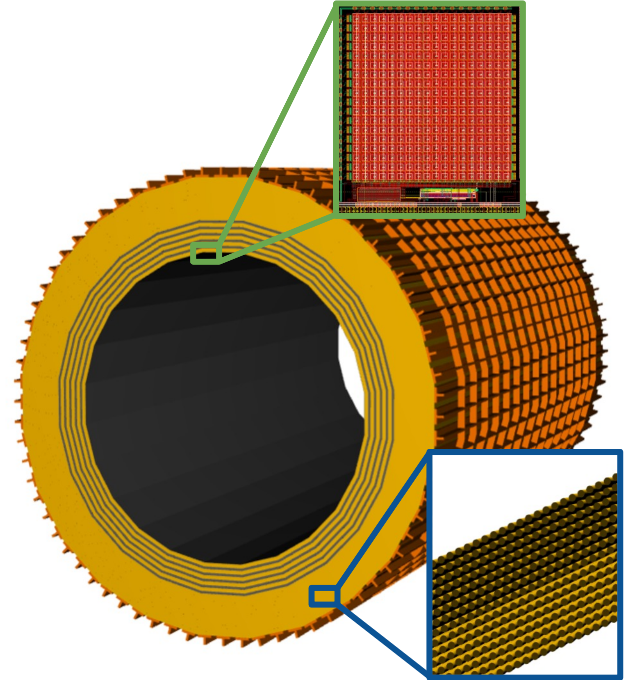
EIC Users Collaboration Meeting

ASTROPIX TRACKER PRODUCTION

BIC Tracker

- ~100 m^2 of silicon
- ~5,000 wafers
- ~250,000 chips
- Optimize the design & building procedures for industrial scale production
    - 1 module flavor x31,200
    - 1 stave flavor x2,400



ASTROPIX CHIPS

~5,000 wafers
~250,000 chips

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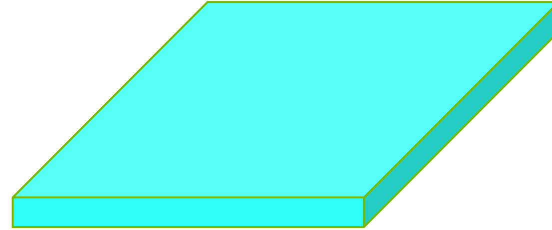
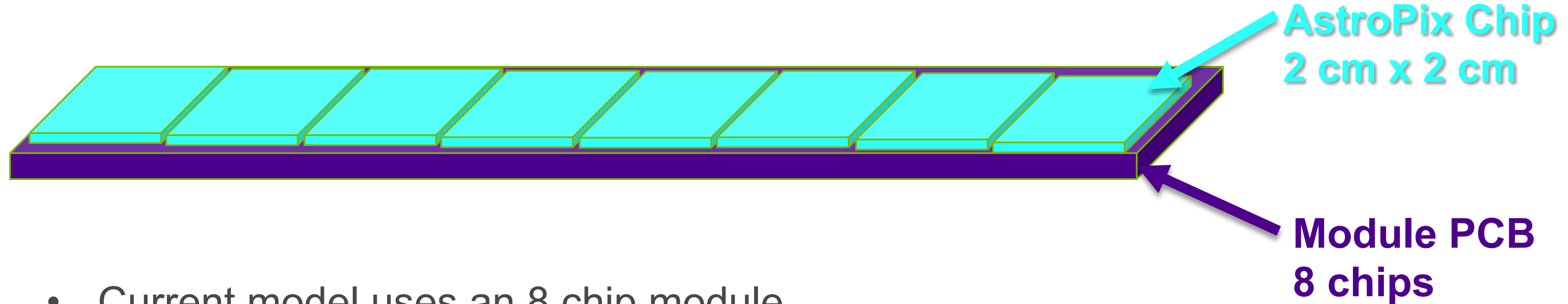


- Probe wafers using a fully automated machine
  - Load a cartridge of 10 wafers, let the machine do the work
  - Identify failing chips (digital/analog) and failing bumps
- Wafers are diced

ASTROPIX MODULE

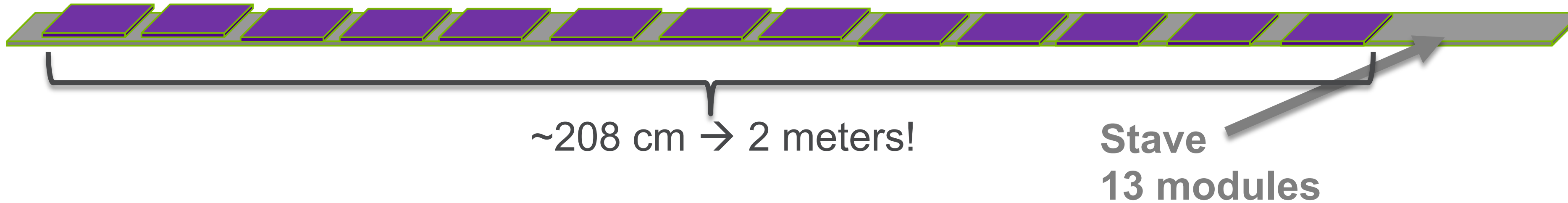
Build ~31,200



- Current model uses an 8 chip module
- Mounted on a rigid pcb for easy handling
  - For space and cooling reasons, the pcb may need to go on top of the chips…
- Chips are mounted using an automatic pick-and-place machine
- Chips are wire bonded to the pcb
- Chips undergo mechanical and electrical QC to verify they work

ASTROPIX STAVE(STEP 1)

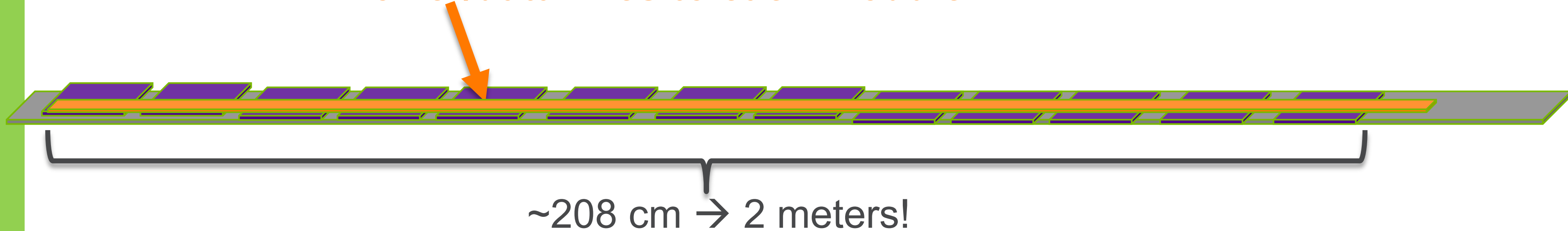
Build ~2,400



- Current model has 13 modules on a stave
  - This will be frozen ASAP
- Plan to use Aluminum staves
- Nice to have some easy screw mounting to the staves
  - Or could use tooling similar to SLAC for ATLAS Pixels
  - Or could be automated with pick-and-place machine
- Metrology QC is done at this stage

ASTROPIX STAVE+BUS TAPE (STEP 2)

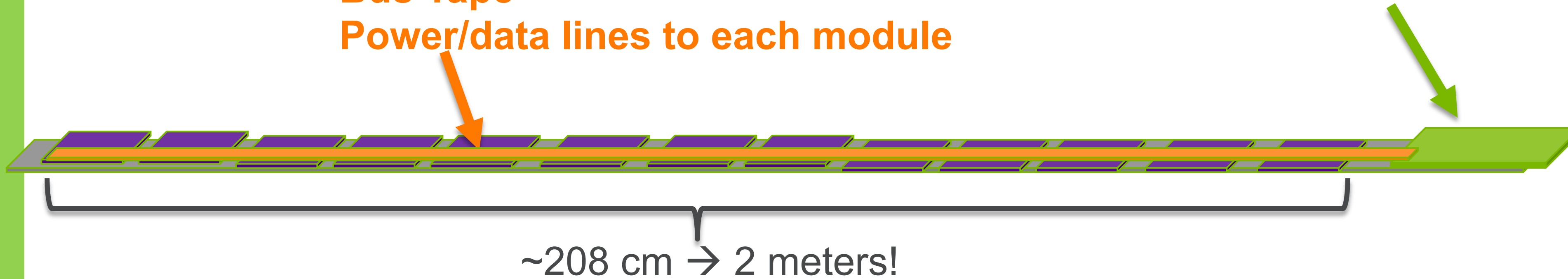
Build ~2,400



- Connect the modules to the bust tape
- Bus tape will provide power, command, data, and any types of monitoring lines
- Easiest to have a connector(s) on each module that connects to the bus tape
  - Also used for module testing

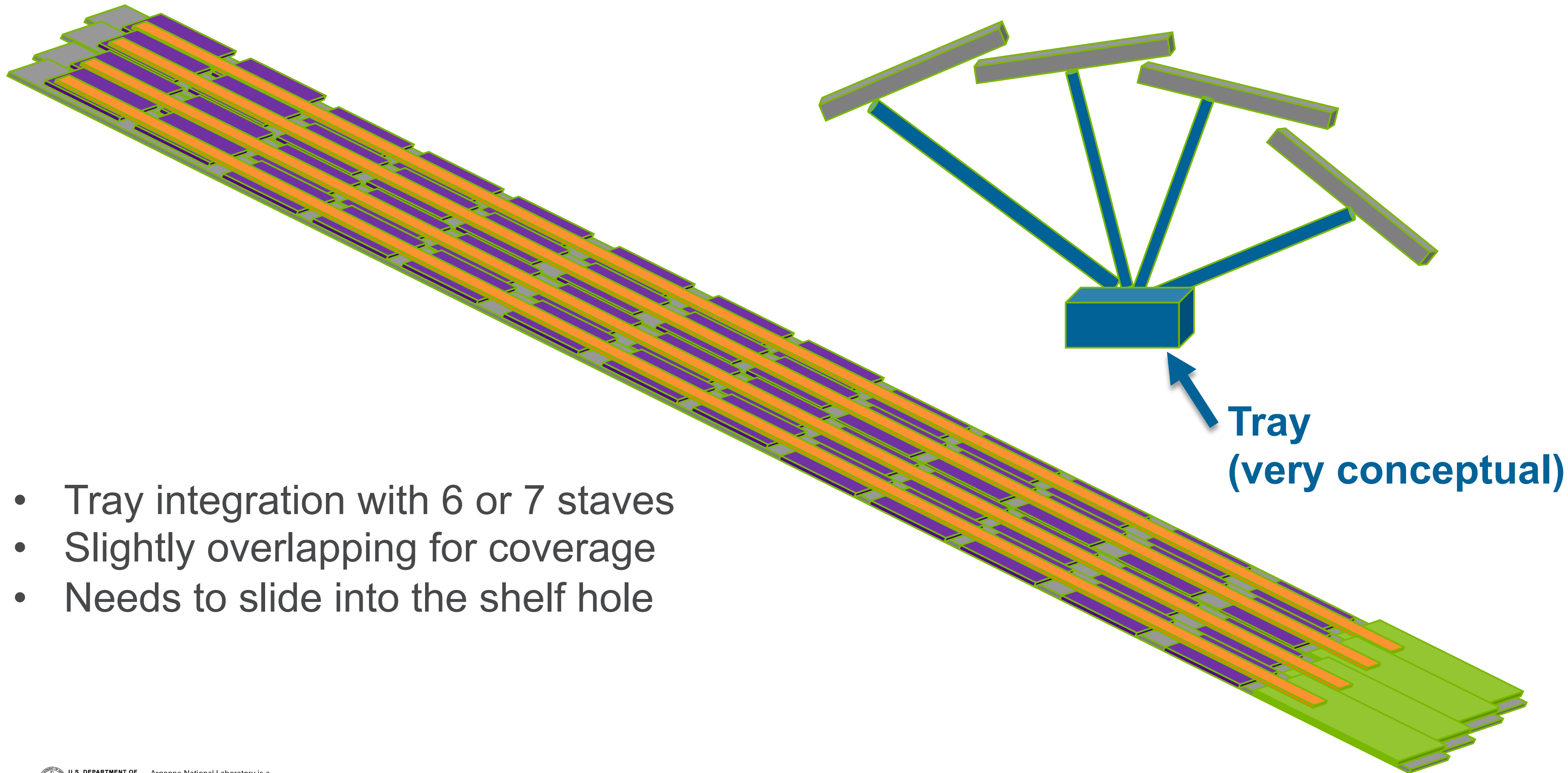
ASTROPIX STAVE+BUS TAPE+EOS (STEP 3)

Build ~2,400



- Stave will be connected to the end-of-stave card via the bus tape
- End-of-stave card will interface to the ePIC DAQ
- This end-of-stave card is used for QC testing the stave
  - It could be the final EOS or one associated with a test stand
- Assume that the modules are relatively easy to rework on a stave, then the majority of detailed electrical tests will happen at this stage

ASTROPIX TRAYS



- Tray integration with 6 or 7 staves
- Slightly overlapping for coverage
- Needs to slide into the shelf hole

ASTROPIX TRACKER PRODUCTION

	# On-Detector	Yield	Total to Build	Total Good After Yield	Hours/ piece	Total Hours*
wafers			4838			
chips	249,600	89%	290,304	261,274	0.05	14,515
modules	31,200	98%	32,659	32,006	0.21	6,858
staves	2,400	99%	2,462	2,437	0.63	1551
trays	384	99%	390	386	2.5	975
Module PCB	31,200	95%	34,378	32,659	0.025	860
Bus tape	2,400	90%	2,736	2,462	0.025	68
EOS cards	2,400?	90%	433	390		

*Total hours don’t reflect parallelization or people hours
All yields and times are a first assumption and will change

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BACKUP

Thank You

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University of California Santa Cruz

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University of Manitoba

University of Regina

Mount Allison University

NSERC

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Kyungpook National University

Yonsei University

University of Seoul

Pusan National University

Korea University

Sungkyunkwan University

Hanyang University

Gangneung-Wonju National University

Germany

Karlsruhe Institute of Technology

University of Giessen

ePIC BIC Detector Subsystem Collaboration

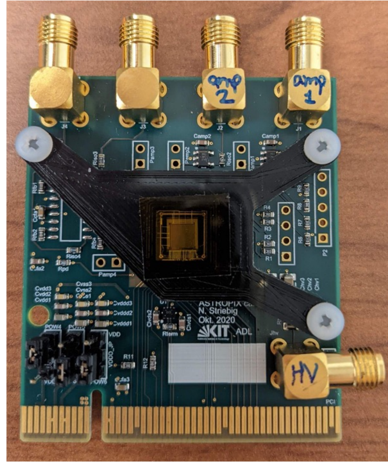
AstroPix Collaboration:

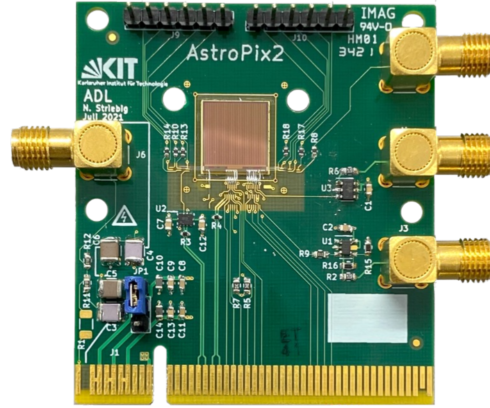
Hiroshima University

Nagoya University

ASTROPIX DEVELOPMENT

ATLASPix	AstroPix_v1	AstroPix_v2	AstroPix_v3



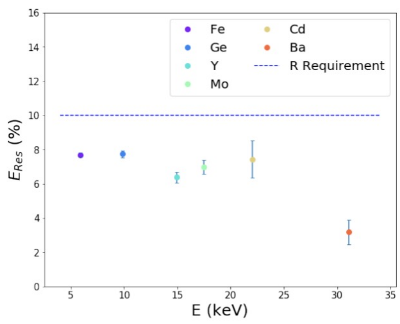


ATLASPix	AstroPix_v1	AstroPix_v2	AstroPix_v3
100 µm thick wafer	----------------720 µm thick wafer----------------		
40 x 130 µm^2 pitch	175 x 175 µm^2 pitch	250 x 250 µm^2 pitch	500 x 500 µm^2 pitch
0.3 x 1.6 cm^2 chip	0.5 x 0.5 cm^2 chip	1 x 1 cm^2 chip	2 x 2 cm^2 chip
150 mW/cm^2	14.7 mW/cm^2	3.4 mW/cm^2	1.06 mW/cm^2

(Power numbers represent amplifier+comparator only, not full digital power. Full v3 power draw = 4.12 mW/cm^2)

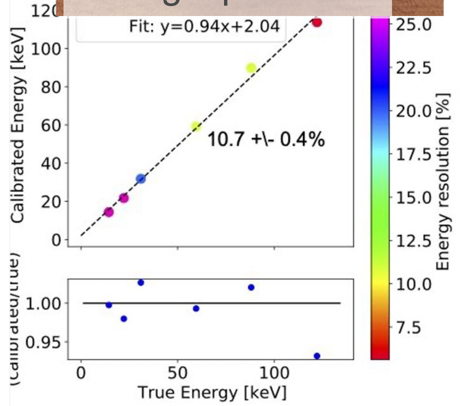
ASTROPIX DEVELOPMENT

ATLASPix



I. Brewer *et al*, 2021

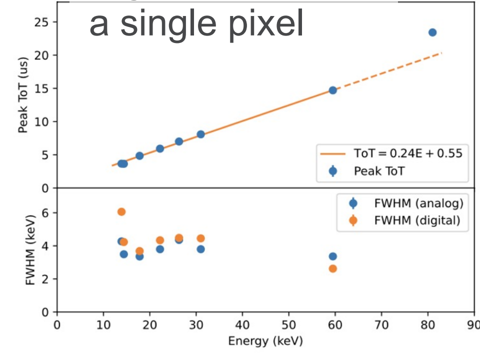
AstroPix_v1



A. Steinhebel *et al*, 2022

AstroPix_v2

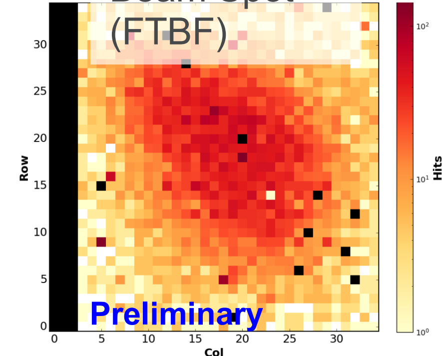
Digital data from
a single pixel



Y. Suda *et al*, 2023

AstroPix_v3

Beam Spot
(FTBF)



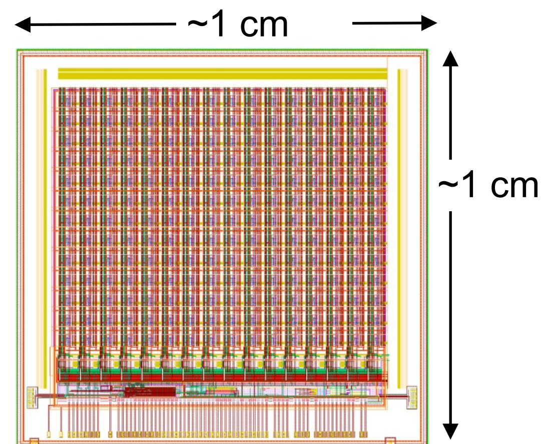
ASTROPIX: V4

AstroPix Features (v4):

- Potentially the final design in small size 1 cm x 1 cm
- 500 um pixel pitch
- Wafers recently delivered by foundry
- Previous versions needed to meet certain ’flyable’ specifications like low power
- Implement more features for better performance

Features:

- Time stamp w/ 3.125 ns time resolution
- Row & Column from individual pixel hitbuffer
- Increase Time-Over-Threshold (ToT) bits
- Improve Threshold tuning (5-bit)
- Mask noisy pixels
- Pass hits to next chip (daisy chain)
- Self-triggered (only read out active hits)

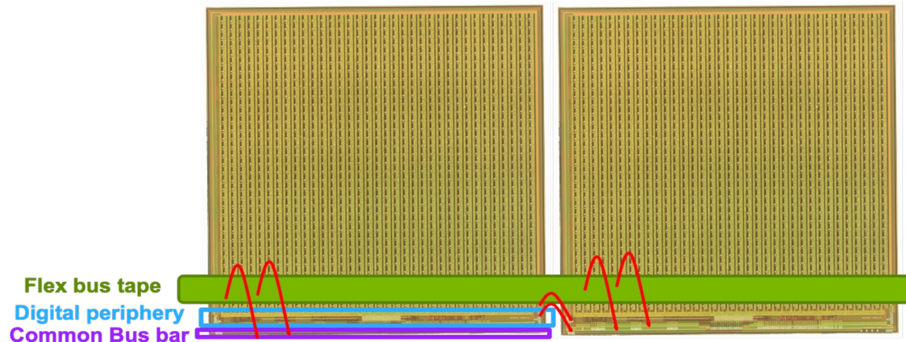


N. Striebig *et al*, in prep

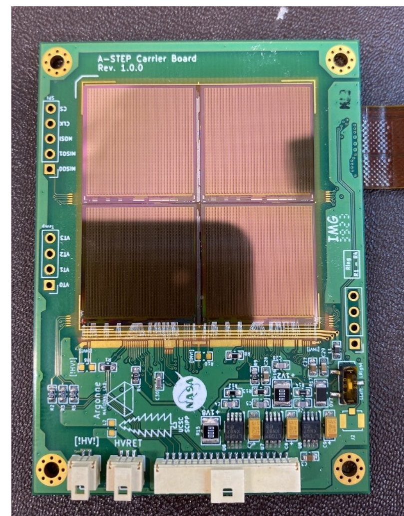
ASTROPIX: NEXT STEPS

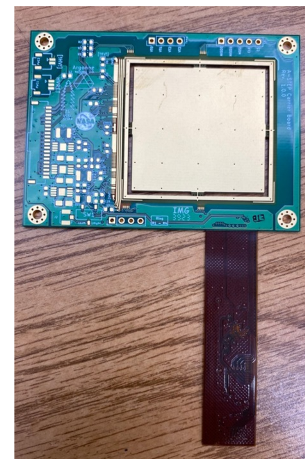
Several Features to Validate Performance:

- Daisy chain readout
  - Multi-chip module read-out board
  - Check for data loss/max occupancy
- Sensor efficiency between pixels, depth
  - Preparing for edge-TCT measurements
  - Charge collection efficiency
- Flex bus tape design
- DAQ development
- Update previous results with v4
  - Test Beam
  - Irradiation: SEU, LET, Total Dose



- Command/Power is distributed through a bus tape
- Wire bonded from bust tape
- Signals are digitized and routed out to the neighbor chip via wire bonds





BIC

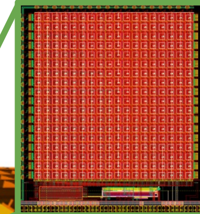
Addressing the unique challenges for the barrel region in ePIC

Hybrid concept: 6(4 now) layers of Astropix interleaved with the first 5 Pb/ScFi layers, followed by a large v... Pb/ScFi layers

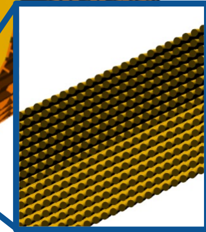
- ✓ Deep calorimeter (21...
- ✓ Excellent energy reso...
- ✓ Unrivaled low-energy... the energy measuren...
- ✓ Unrivaled position res...
- ✓ Deep enough to serv...
- ✓ Very good low-energy...
- ✓ Wealth of information... suited for particle-flow
- ✓ Makes the tracking MPGD layer behind the DIRC unnecessary

BIC Tracker

- ~100 m^2 of silicon
- ~5,000 wafers
- ~250,000 chips
- Optimize the design & building procedures for industrial scale production
  - 1 module flavor x31,200
  - 1 stave flavor x2,400



AstroPix: silicon sensor with 500x500μm^2 pixel size developed for the Amego-X NASA mission



ScFi Layers with two-sided SiPM readout

SENSORS: MONOLITHIC HVCMOS
(MONOLITHICS ACTIVE PIXEL SENSOR (M

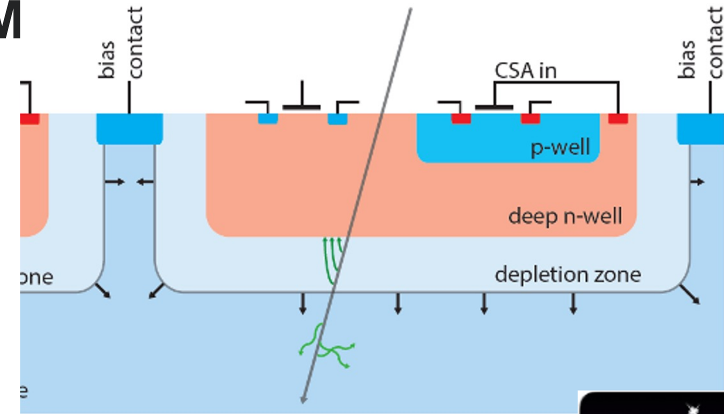
Monolithic: combines a traditional silicon pixel sensor wafer and the Front-End ASIC in a single wafer

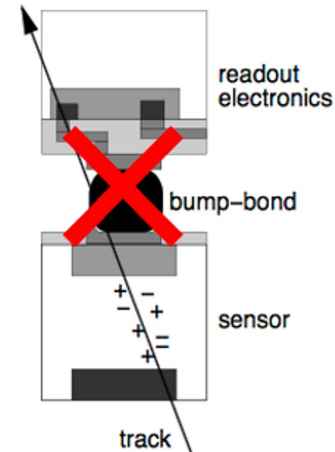
- Each pixel has it's own amplifier in a deep n-well
- High-resistivity substrates enable sensor depletion for collection via drift rather than diffusion
- Technology uses more typical CMOS wafer processing for cost effective production
- Single wafer enables shorter design cycle

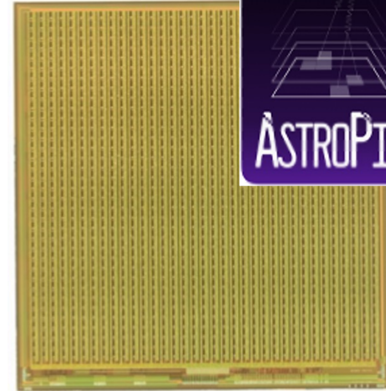
History: HVCMOS developed by Ivan Peric at Karlsruhe Institute of Technology (KIT). He has designed MuPix, ATLASPix, AstroPix, etc.

AstroPix: initially for space-based applications

- Upgrade to the next generation Fermi Telescope—AMEGO-X







ASTROPIX TIMELINE & PRODUCTION

AstroPix versions

- v1 early prototype
- v2 current test bench & test beam studies
  - extensive test bench characterization
  - higher noise due to larger pixel size
  - LET radiation testing
  - first test beam run a few weeks ago
- v3 full size chip
  - minor fixes from v2
  - OR'd rows & columns
  - just received
- v4 new features for better performance (MPW)
  - 'final version', but smaller chip (1 cm x 1 cm)
  - plan to submit in May 2023
  - better noise/threshold performance
  - per pixel hitbuffer
- v5 full size chip
  - fix any bugs from v4
  - Final production version
  - chips available November 2024

Design Validation

- test bench characterization complete
- LET irradiations done
- test beam measurements on-going
- multi-chip DAQ development
- daisy chain readout validation
- compare-1 NASA balloon test Fall 2023
  - DSSD's
- A-STEP sounding rocket January 2025
- ComPair-2 balloon launch 2026

Multi-layer calorimeter prototype (ANL)

- full scale prototype to be built and tested w/ v3
- DAQ development joint with NASA

Production

- fabrication by TSI
  - AMS is a backup, but need a large order

ASTROPIX DEVELOPMENT SCHEDULE

Not shown:
Early CD4 (Oct 2032)
CD4 (Oct 2034)

We are here

	FY19		FY20				FY21				FY22				FY23				FY24				FY25				FY26				FY27				FY28				FY29		
	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3

- AstroPix v1: Design & Fabr. → Test
- AstroPix v2: Design & Fabr. → Test
- AstroPix v3: Design & Fabr. → Test → Test
- AstroPix v4: Design & Fabr. → Test
- AstroPix v5: Design & Fabr.
- AstroPix v5 (production): Production Fab.

v3 has comprehensive test program: benchtop and testbeam, irradiation, quad-chip readout for NASA payload mission (A-STEP), integration with Pb/SciFi for ePIC (R&D studies and test article production)

first v5 wafers used for preproduction

Start of production driven by project fund availability (estimated ~ 1 year after CD2/3)

EIC Project Milestone
New AstroPix version

ePIC BIC Timeline: Design and generic R&D; Final design and EIC R&D; BIC Preproduction; BIC Production

CD0 CD1 CD3a CD3b CD2/3

Start of BIC installation at BNL

AstroPix v1

HV-CMOS MAPS based on ATLASPix3, designed for the AMEGO-X NASA mission, optimized for power dissipation and energy resolution

Nucl.Instrum.Meth.A 1019 (2021) 165795

0.45 x 0.45 cm² chip, 175 µm pixel pitch
18 x 18 pixel matrix
Power dissipation 14.7 mW/cm²

AstroPix v2

1 x 1 cm² chip, 250 µm pixel pitch
35 x 35 pixel matrix
Row/column readout
Power dissipation 3.4 mW/cm²

AstroPix v3

First full-size chip

2 x 2 cm² chip, 500 µm pixel pitch
Row/column readout
Power dissipation <1 mW/cm²
2.5 MHz timestamp, 200 MHz ToT

AstroPix v4

Final design but smaller size

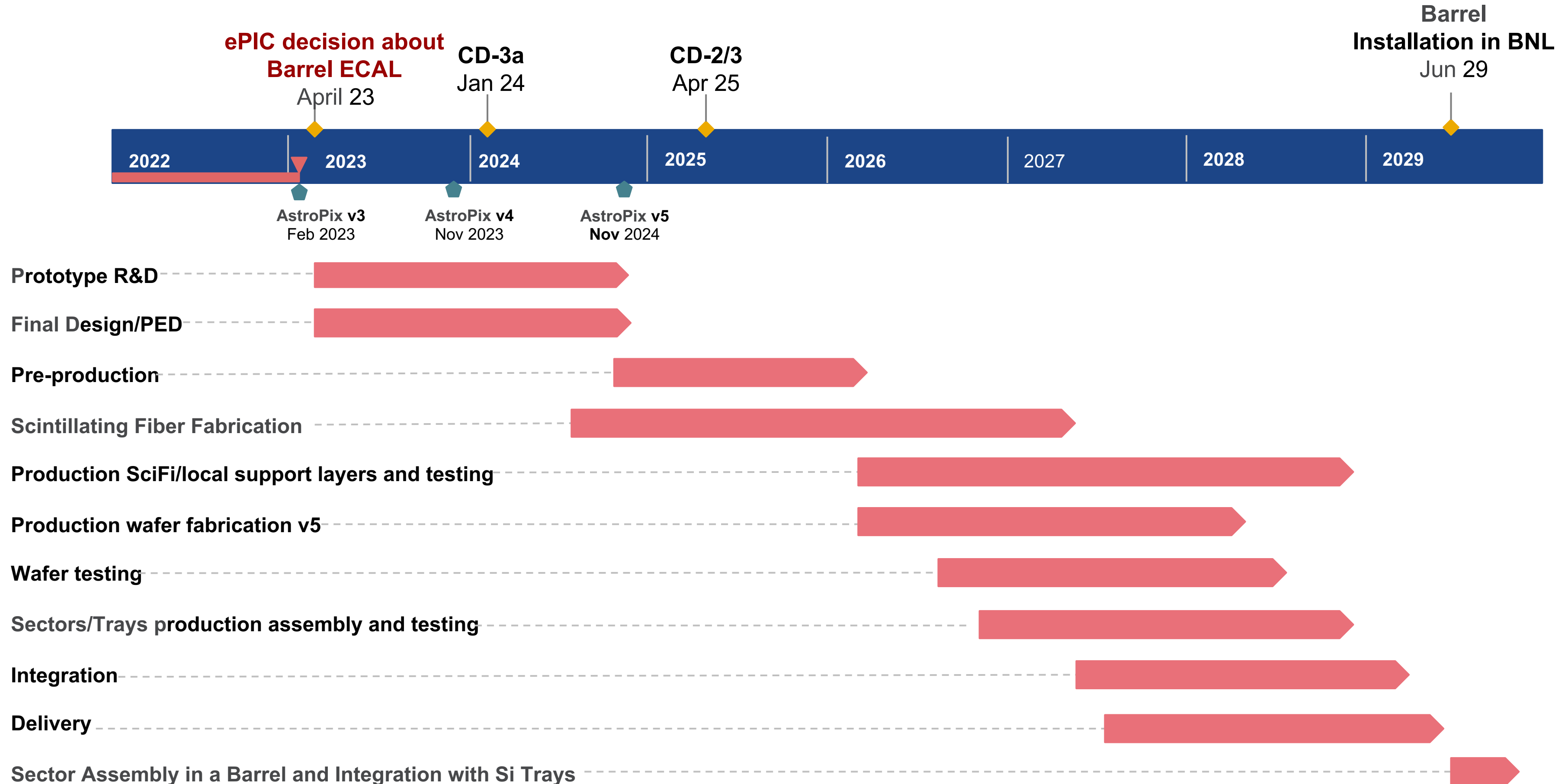
1 x 1 cm² chip, 500 µm pixel pitch
Individual pixel readout
3 timestamps, 3.25ns time resolution
TuneDAC for pixel-by-pixel thresholds

AstroPix v5

Full-size production chip

2 x 2 cm² chip, 500 µm pixel pitch
Design identical to v4 (with bug fixes)

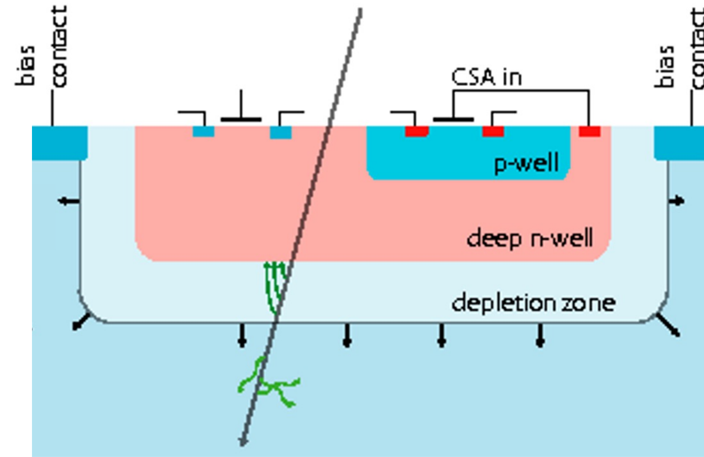
BIC HIGH-LEVEL SCHEDULE



AstroPix

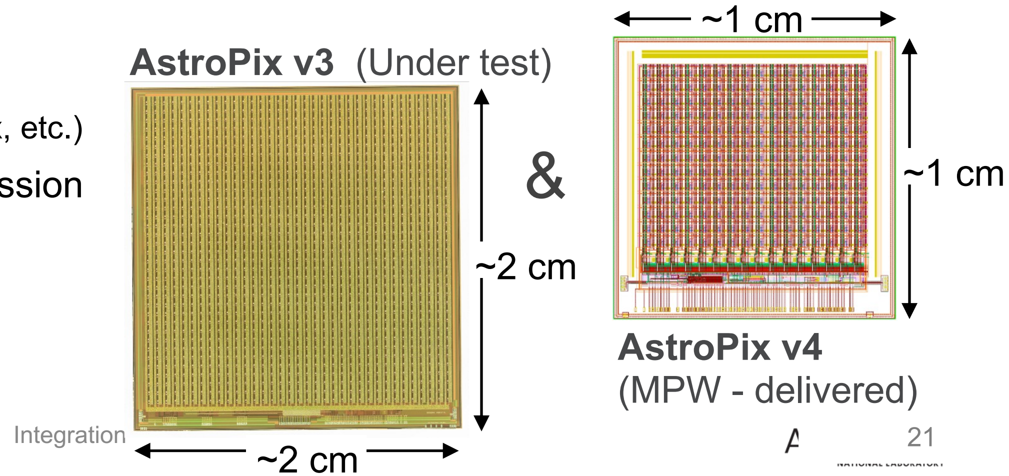
HV-CMOS Monolithic Active Pixel Sensor (MAPS):

- Combination of silicon pixel & Front-End ASIC
- On-pixel charge amplification and digitization
- Technology uses more typical CMOS wafer processing for cost effective mass production
- Fabrication on single wafer enables shorter design cycle
- No need to bump-bond to each pixel - improves yield



AstroPix (based on **ATLASPix3** **arXiv:2109.13409**)

- 180nm HV-CMOS MAPS sensor
  designed at KIT (also designed ATLASPix, MuPix, etc.)
- Developed for AMEGO-X GSFC/NASA mission
  (Upgrade to the Fermi's LAT)
- Power consumption <1.5 mW/cm^2
- Energy resolution target of 2% @ 662keV



AstroPix Developments

AstroPix v1 - January 2021

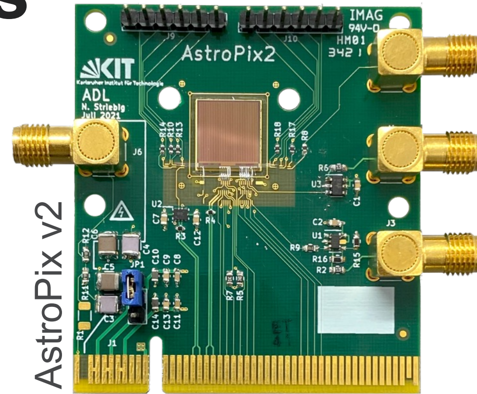
- 0.45 × 0.45 cm^2 chip, 175 μm pixel pitch
- 18 × 18 pixel matrix
- Power dissipation ~14.7 mW/cm^2

AstroPix v2 - December 2021

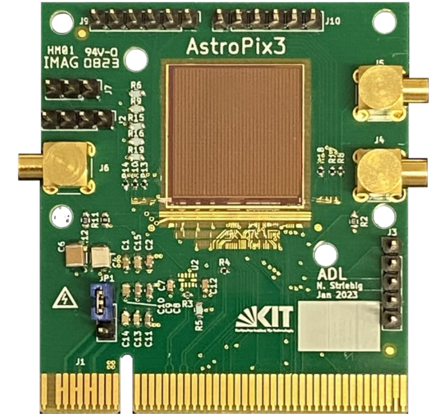
- 1 × 1 cm^2 chip with 250 μm pixel pitch
- 35 × 35 pixel matrix
- Hit identification with Row/Column readout
- Power dissipation ~3.4 mW/cm^2

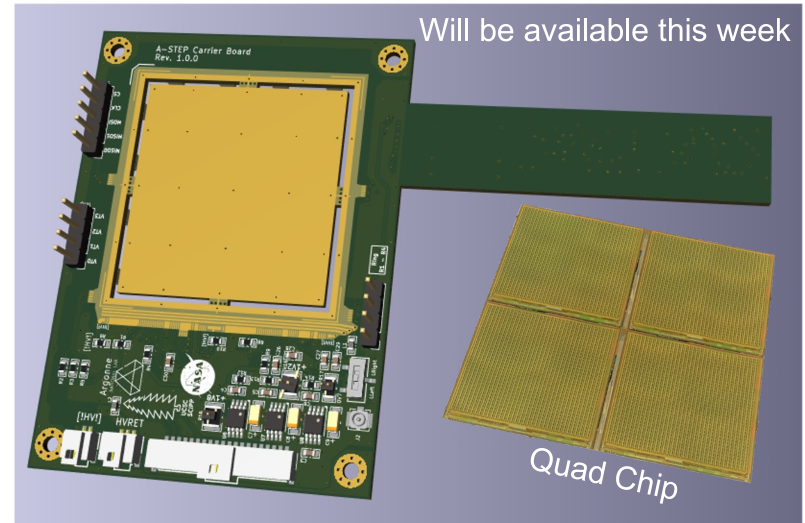
AstroPix v3 - February 2023

- 2 × 2 cm^2 chip with 500 μm pixel pitch
- Power dissipation <1 mW/cm^2 (targeted)
- Timestamp clock 2.5MHz, ToT 200 MHz
- 10 byte data frame per hit



AstroPix v2





AstroPix v3 Quad-chip Carrier Board

AstroPix v4/v5

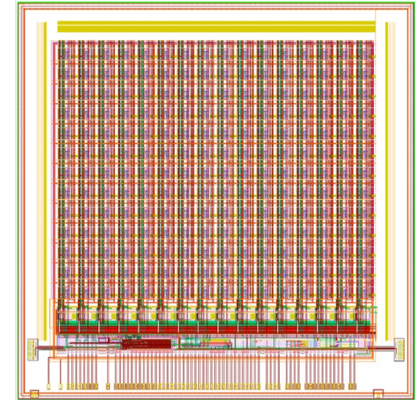
AstroPix v4 : Final design version will small size

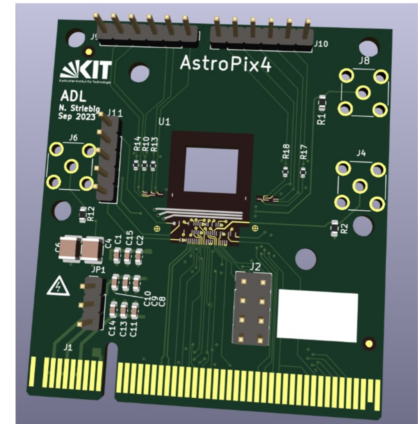
- Chip size 1 × 1 cm^2; Thickness 700 μm, V_{BD} ~ 400V
- Pixel pitch 500 μm with pixel size 300 μm, 16 × 16 pixel matrix
- Individual pixel readout with individual hit buffer
  - No identification issue due to ghost hits
- 3 Timestamps - 2.5MHz (TS), 20 MHz (Fine TS), and 16 bit Flash TDC
  - Fast ToT and Timestamp with 3.125 ns time resolution
- TuneDACs - Pixel-by-pixel threshold tuning and pixel masking
- Daisy Chain readout - pass hits to next chip through QSPI
- Self-triggered (reads out active hits)

AstroPix v5 : Full size final design

- No planned design changes
- Fix any bug from v4
- Full size chip - 2 × 2 cm^2, pixel pitch 500 μm,
- 35 × 35 pixel matrix → 1225 hit buffers

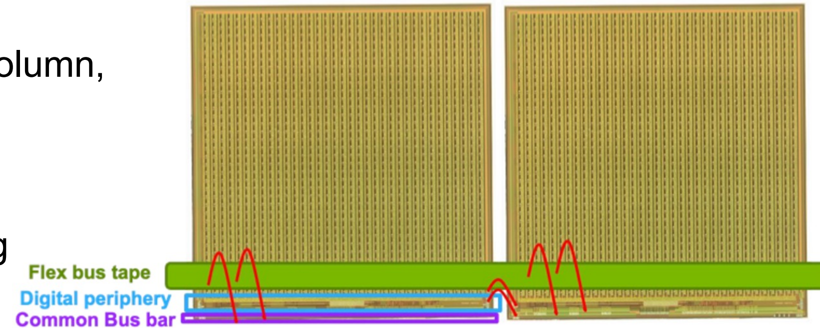
AstroPix v4

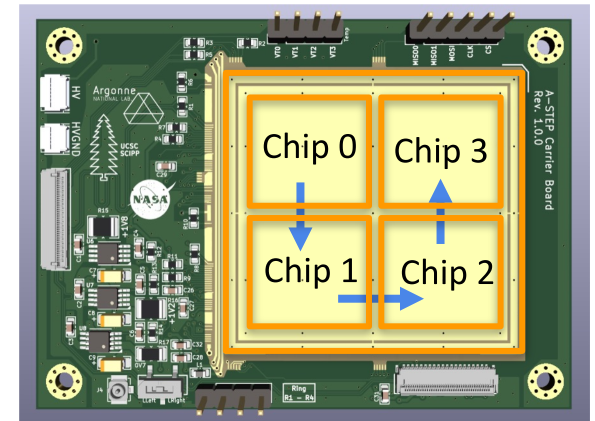




AstroPix Readout

- 8 bytes data per hit - header (chipID, payload), row/column, timestamp, ToT
- SPI I/O daisy chained - chip-to-chip signal transfer
  - signals are digitized & routed out to the neighboring chip using 5 SPI lines via wire bond
- Power/Logic I/O distribution on the module (through a bus tape)
  - 4 power lines (LV, HV), ~20 Logic I/O (SPI, clk, timestamp, interrupt, digital Injection, etc.)
  - HV, VDDA/VDDD(1.8V), VSSA(1.2V), Vminuspix(0.7V)
  - power distribution can be controlled using voltage regulators
  - mostly part of end of the stave services
- Data will be received by FPGA at the end of stave
  - FPGA aggregates data before sending off-detector
- Low heat load at chip, only cooling of end of the stave card
- Operational temperature for AstroPix is at room temperature and considered to be operated at 22 ℃





AstroPix v3 quad-chip carrier board
- Demonstrate required services
- Daisy chaining

AstroPix at ePIC

Low Rates

- The expected hit rate for **all imaging layers together** is well below < 3×10^7 Hz
- This translates to a maximum hit rate per tracker stave (1 x 104 chips) < 36 kHz

Zero-suppression below threshold 20 keV (4 × noise floor) well suited for EIC electromagnetic showers

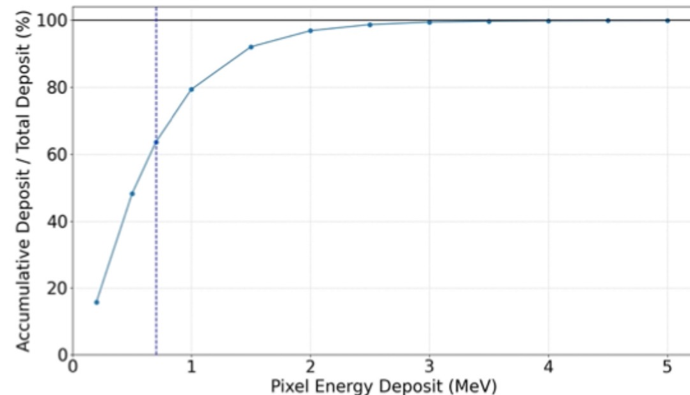
Timing requirement: 3.125 ns (v4/v5) - **driven by 10 ns bunch crossing**

Low Ionization radiation dose and neutron flux

- The maximum **ionizing radiation dose < 1 kRad/year** for the barrel region
- Max neutron flux - order of **10^9 $n_{equivalent}$/cm^2 per year**

Dynamic range (see plot for 2 GeV e^-)

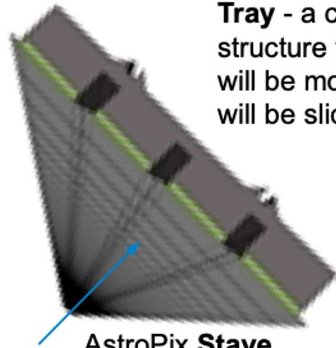
~ 3 MeV



Accumulative energy deposit to the total energy deposit for 2 GeV electrons.

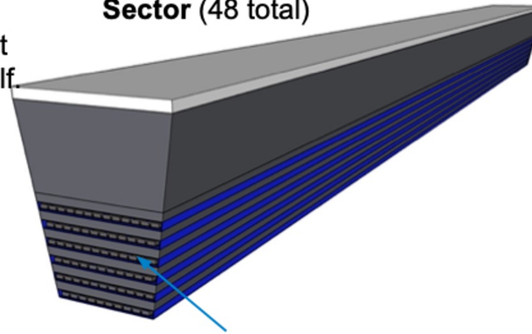
- About 63% of the energy deposit was made through hits with deposit < 700 keV
- hits with deposit < 3 MeV contribute to 99% of the total energy deposit

AstroPix Assembly



Tray - a carbon fiber structure the staves will be mounted on. It will be slid into a shelf.

AstroPix **Stave**
Consists of 1 x 108 chips with the support structure, “turbofanned”
AstroPix **Module**
Subset of chips



Shelf - a carbon fiber structure that is glued to the Pb/ScFi layers, that we will slide trays with AstroPix staves on.

*The designs presented on these slides are not final but for illustration only

Module Strategy

- QC testing with wafer probing + Module and stave level QC testing and tuning
- “Baseline” model of Modules on Stave
  - Module - 8 single chips
  - Stave - 13 Modules - 104 chips
  - 12 or 14 Staves per AstroPix layer per Calorimeter Sector
  - Total 249600 chips
- All staves are identical and gets combined in a separate production step
- Data transmitted to end of the Stave card using flex base tape
- Institutions - ANL, GSFC/NASA, KIT ,UCSC, Korea, Oklahoma State

AstroPix Timeline and Production

v3 full size chip (ongoing testing)

- Test bench characterization (ongoing)
- Testbeam performance studies
- Active and passive irradiation **~10^{15} $n_{equivalent}$/cm^2**
- **Quad-chip readout (ready to test)** for NASA's hosted payload mission (A-Step) - **January 2025**
- Integration with Pb/SciFi - FY2024

v4 new features for better performance (MWP)

- **Final design version**, smaller chip (1cm × 1cm)
- Fabricated wafers **delivered last week**
- Chip carrier board design for bench test is ready for the PCB fabrication

v5 full size final chip

- Fix any bugs from v4
- v5 chips available **November 2024**

GSFC/NASA ComPair-2 AstroPix timeline

Tasks	FY24												FY25											
	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S
Full ComPair Instrument							CDR																PI	
AstroPix Tracker												Tkr-PIR												
AstroPix v3 Quad Chip Testing																								
v3 Depletion Test																								
v3 multi-layer testing (A-STEP)																								
Integrate v3 w/ proto Segment																								
AstroPix v4 MPW design + fab																								
AstroPix v4 carrier board																								
AstroPix v4 testing																								
v4 Depletion Test																								
Standard test procedure dev.																								
AstroPix v5 testing carrier board																								
AstroPix v5 design + fab																								
AstroPix v5 testing																	Deliver to ANL							

BIC@ePIC Timeline

- **Prototype R&D** (v3) Ongoing - till Nov 24
- Pre-Production (v5) chips starts **Nov 2024**

Production

- Fabrication by TSI - with a large production order, AMS is a backup