Basics of serial powering

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Introduction

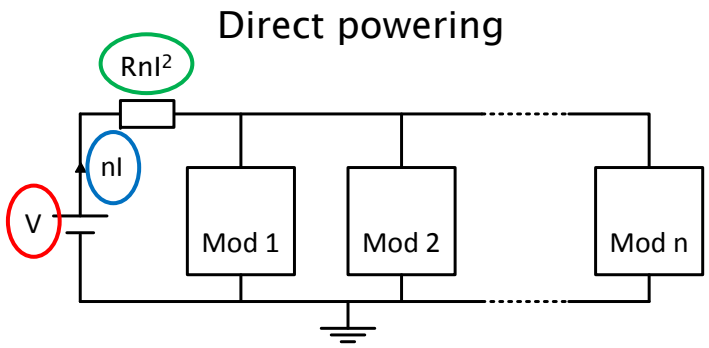
- In the following slides (2 to 4) a module is the detector's active element, that is the sensor with its readout electronics.
- It can be an hybrid pixel detector where sensor and readout electronics are two separate entities bump bonded together, or a MAPS detector where sensor and readout electronics are integrated in the same substrate.

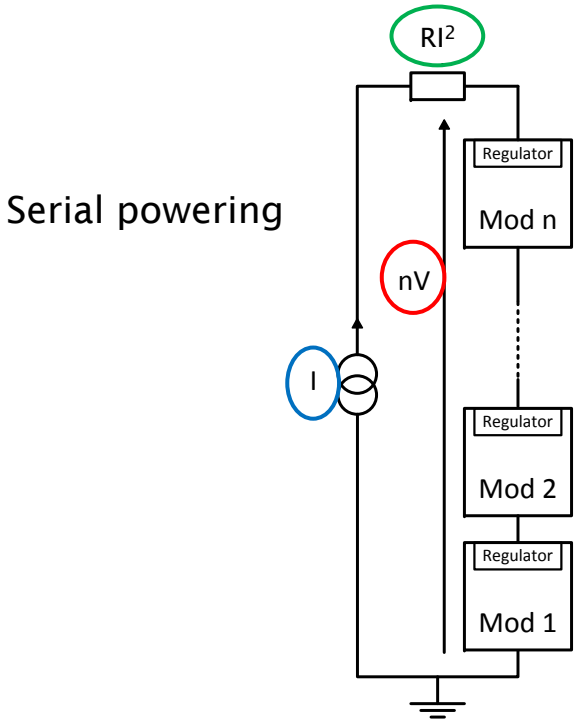
- Serial powering is used to power the readout electronics, not to bias the sensor.
- Power to the readout electronics is typically called "low voltage".

- The choice of serial powering for the low voltage distribution impacts the data transmission scheme and the sensor bias scheme.

Serial powering basics

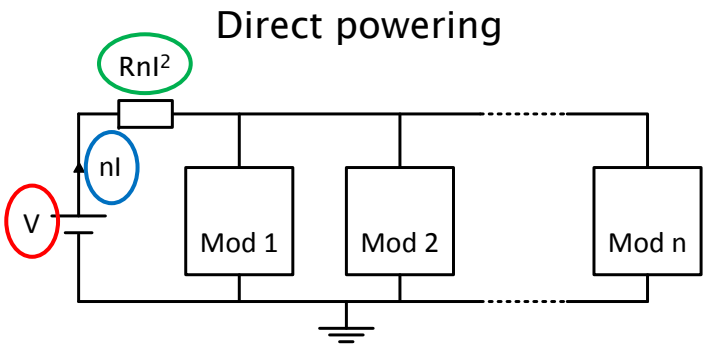
- Serial powering is a current based powering scheme, where modules are powered in series by a constant current.
- The current to voltage conversion is done by regulators close to/on module.
- In a serial powering chain made of n modules, the transmitted current is only the current needed by one module, I.
- For n modules powered in series, the current is reduced of a factor n with respect to a direct powering scheme → Higher power efficiency and reduced cable volume.
  - Cable cross-section and the power losses on the cables scale by the same factor.



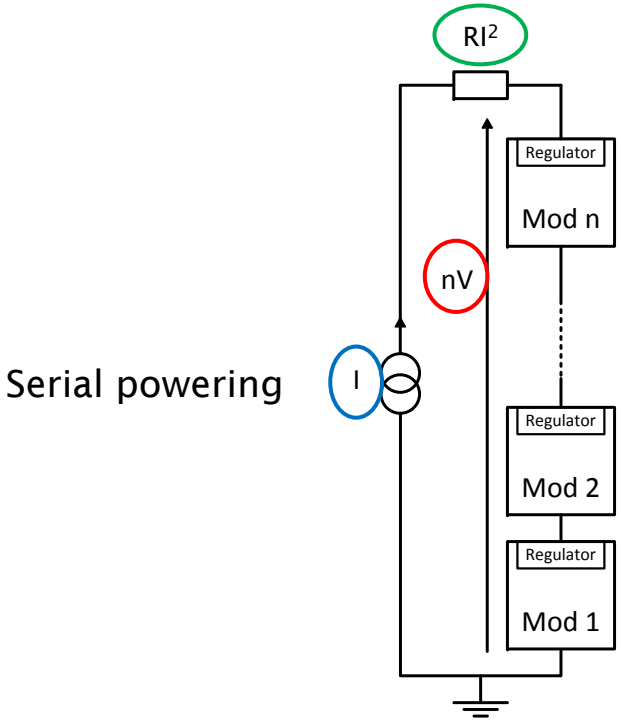


Serial powering basics

- As the modules are powered with a constant current, V_{drop} is not constrained as in a voltage based powering scheme.
  - It can in principle be chosen only depending on the output voltage capability of the current source and of the allowed power density (i.e. cooling capability).



- Higher V_{drop} can be allowed in the active area of the detector to reduce the material budget of the cables.
  - Outside the detector the voltage drop can be reduced to lower the power losses.

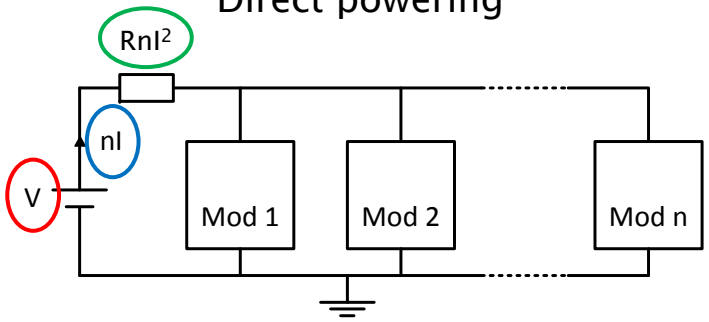


- With respect to voltage based powering schemes (incl. DC-DC), serial powering allows more flexibility in the optimization of material and power efficiency.

Serial powering basics: data transmission

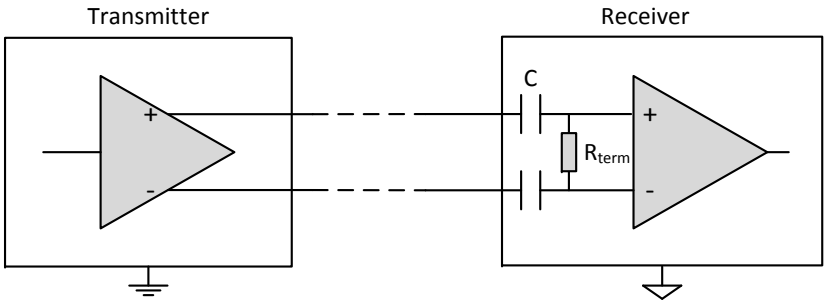
- The voltage across the chain is nV, where V is the voltage on a module.
- Each module sits at a different ground potential.

Direct powering

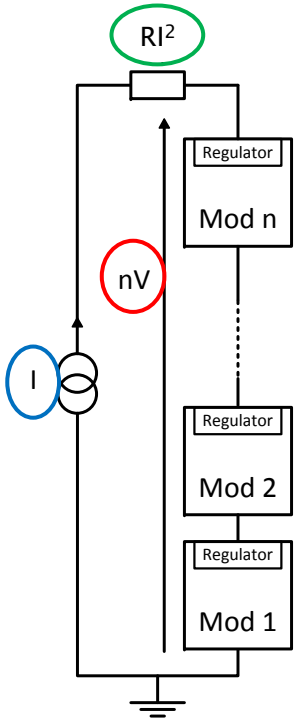


- AC coupled data transmission required.
  - DC balanced data protocol (e.g. 8b10b).
  - Self biased receiver inputs to set the common mode voltage.

Sketch of a AC-coupled LVDS link



Serial powering



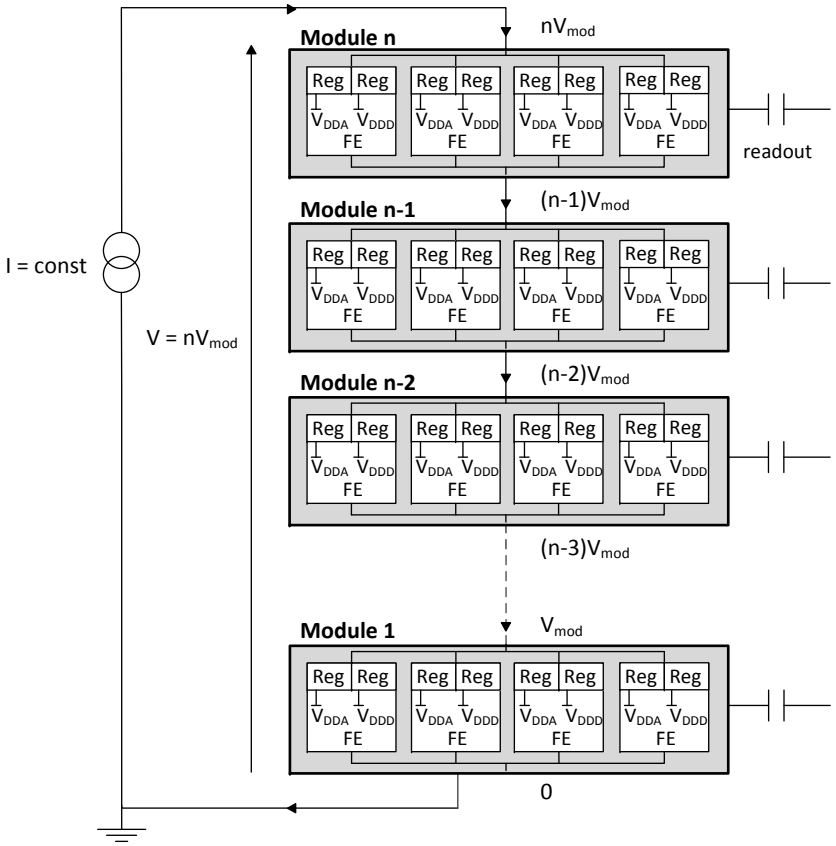
Serial powering basics: sensor biasing

- The voltage across the chain is nV, where V is the voltage on a module.
- Each module sits at a different ground potential.

- A group of sensors can be powered in parallel, i.e. sharing the same bias line + return, if the difference between operational voltage and breakdown voltage is larger then the total voltage drop in the chain.
- This is the case for planar sensors in hybrids pixel detectors biased to 100s volts.
- This is not the case for MAPS detectors where the sensor is biased with a few volts.
  - Direct powering of each sensor, required one floating supply channel per MAPS sensor.
  - Generate the sensor bias from the low voltage.

Example: ATLAS ITk detector

- The ATLAS pixel detector at the HL-LHC adopted serial powering (also the CMS pixel detector).
- Each module is made of a sensor bump bonded to a certain number of readout chips.
  - In the sketch, four readout chips per module (FE).
- The current flows in series between modules and in parallel between readout chips on a module.
- In each chip, two shunt-LDO regulators generate the analogue (V_{DDA}) and digital (V_{DDD}) voltages.

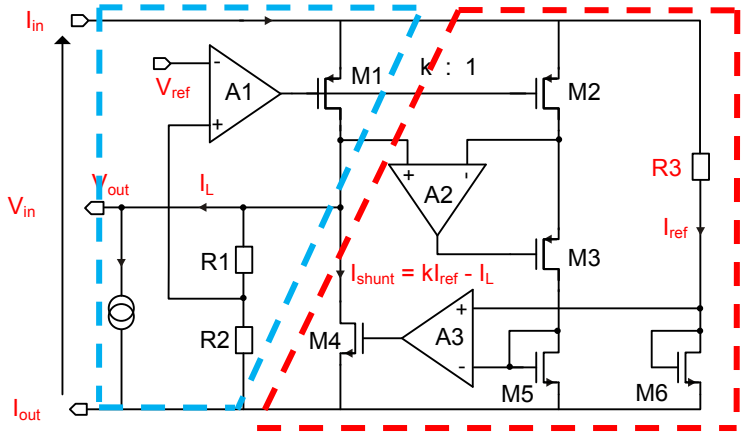


Shunt-LDO regulator

- For this powering scheme, on-chip regulators are needed that can:
  - Operate in parallel;
  - Generate different output voltages out of the current supply;
  - Shunt additional current in case of device failure.

- The Shunt-LDO regulator was designed to match these requirements.
  - First prorotype version in the ATLAS pixel FEI4 chip (180 nm process).
  - Full SP version in the RD53 chip (65 nm process).

- It combines two regulation loops.
  - Shunt regulation circuitry → regulates the current to the chip.
  - LDO (Low Drop Out) regulation loop → generates the voltage for the chip.



Earlier SP regulator configurations

- Initial tests were done with the ATLAS FE-I3 pixel chip using a Shunt regulator to generate a constant voltage out of the input current and then one or two LDO to generate the VDDD and VDDA voltages needed by the pixel chip.
- To add redundancy to the SP chain, all shunt regulators on module are operated in parallel.
- Beneficial for voltage regulation when using shunt regulators as the input resistances are connected in parallel, lowering the total resistance and improving the voltage stabilization.

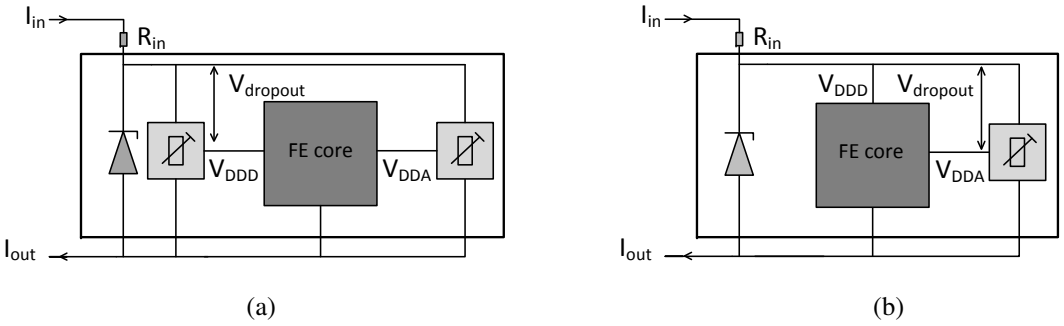
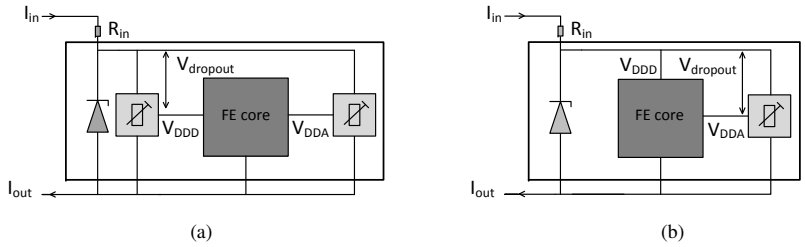


Figure 4.4: Schematic drawings of on-chip shunt and LDO regulators, represented respectively as a zener diode and variable resistors, to convert the input current into two stable voltages. These regulator configurations have been used with FE-I3 modules to generate $VDDD = 2.0\,\mathrm{V}$ and $VDDA = 1.6\,\mathrm{V}$.

Earlier SP regulator configurations

- However, this connection can be critical.
  - Due to mismatch and process variation, the shunt regulators placed in parallel can have different Vthres.
  - As the input characteristics of shunt regulators is very steep, the regulator with lower Vthres can take all current at start- up and burn.
  - This could eventually lead to a chain reaction and destroy all regulators on module.
- Safe parallel operation of shunt regulators requires to choose the value of the input series resistance according to the spread in threshold voltage values, in order to mitigate the I-V characteristics.
- The use of this resistance lowers the power efficiency and decreases the voltage stability.



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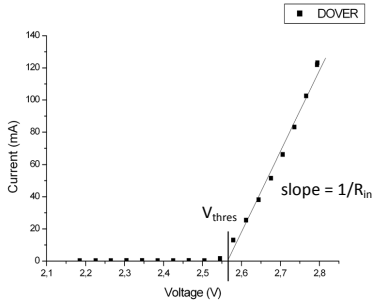
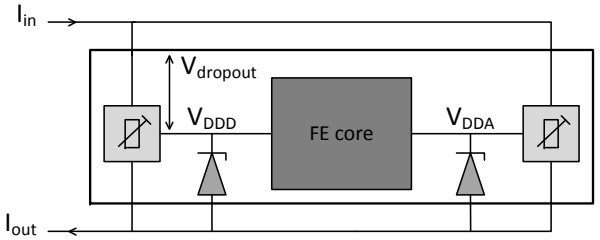


Figure 4.3: I-V characteristics of a shunt regulator integrated in the FE-I3 chip (DOVER). This regulator has V_{thres} = 2.58 V and R_{in} = 1.9 Ω [51].

New regulator concept: Shunt-LDO

- Combination of a Low Drop Out (LDO) regulator and a shunt regulator.
  - Shunt transistor is part of the LDO load.
  - R_{in} of the shunt is replaced by the LDO power transistor.



- LDO regulation loop → constant V_{out}

$$V_{out} = 2 \cdot V_{ref}$$

- Shunt regulation circuitry → const I_{load}
  - I_{ref} set by R3, depends on V_{in} (→ I_{in})
  - I_{M1} mirrored and drained in M5
  - I_{M1} and I_{ref} compared in A3
  - M4 shunts the current not drawn by the load

$$I_{in} \approx kI_{ref} \approx k\frac{V_{in} - V_{thM6}}{R3}$$

$$R_{in} \approx \frac{V_{in}}{I_{in}} \approx \frac{R3}{k}.$$

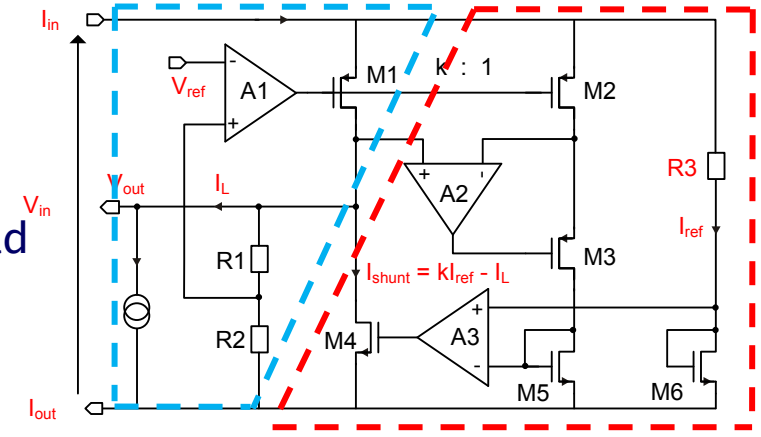
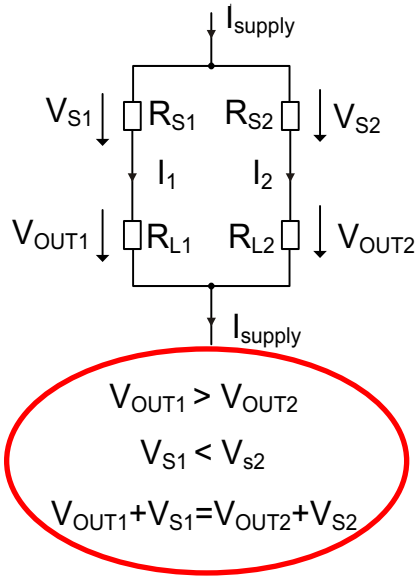


Figure 4.6: Simplified schematics of a Shunt-LDO regulator, explained in the text [46].

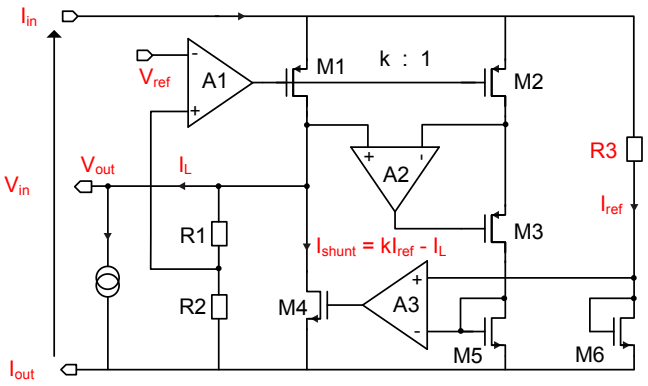
Shunt-LDO regulators in parallel

- The Shunt-LDO has an ohmic I-V characteristics → safe operation of Shunt-LDO regulators connected in parallel.
  - Even for different values of R_{in}, i.e. different R3
- More robust design against process variation and mismatch.
- Differences in the value of R3 lead to different shunt current values but do not destroy the regulator.
- Shunt- LDO regulators can be placed in parallel even if they generate different output voltages: the difference between their output voltages is compensated by the $V_{dropout}$ across the pass transistor of the LDO regulator, M1.
- Finally, should one of the parallelly placed regulators fail, the extra current can be shunted by the other regulators.

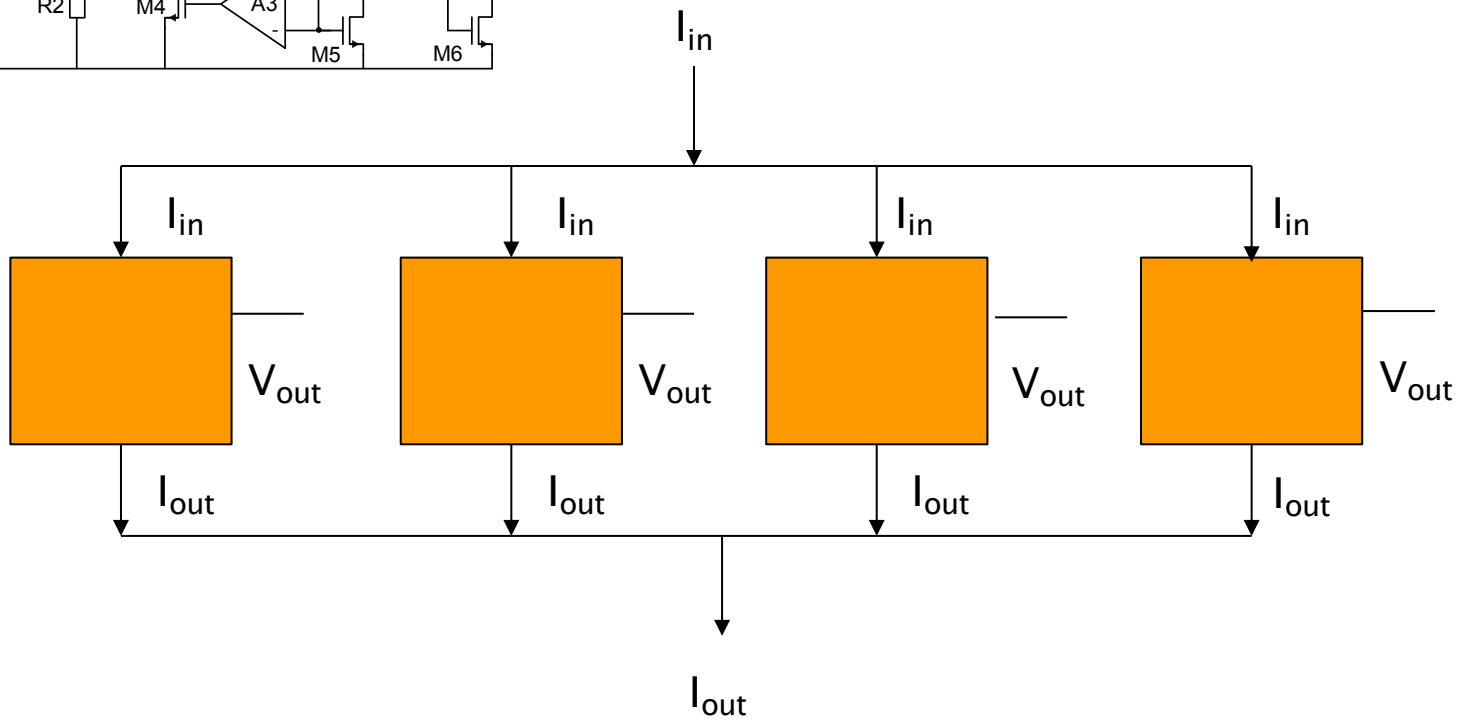
$$R_{in} \approx \frac{V_{in}}{I_{in}} \approx \frac{R3}{k}.$$



Shunt-LDO regulators in parallel



- Parallel connection means that I_{in} and I_{out} are in parallel, not V_{out}



Shunt-LDO in RD53 chips

- The production version of the regulator for the ATLAS ITk pixel detector includes many protection features and addresses all possible regulator failure modes.
- The design is considered robust enough that a bypass element on each module has been deemed not necessary.
- The development time of this regulator was 7 years, with 5 designs submitted.
- More details at
  - M. Karagounis, Shunt-LDO RD53B features, talk, 2020 https://indico.cern.ch/event/879686/contributions/3706455/attachments/1975390/3287622/SLDO_RD53B_Features.pdf
  - M. Karagounis, Evolution of the SLDO Regulator, talk, 2022, (ask Laura for the slides)

Backup

Literature

- ATLAS SP Proof of concept and Shunt-LDO in 180 nm
  - L. Gonella, PhD thesis, https://cds.cern.ch/record/1633150?ln=en
  - L. Gonella, D. Arutinov, M. Barbero et al. **'A serial powering scheme for the ATLAS pixel detector at sLHC'**. In: JINST 5 (2010), p. C12002. doi: 10.1088/1748-0221/5/ 12/C12002.
  - M. Karagounis, D. Arutinov, M. Barbero et al. **'An Integrated Shunt-LDO Regulator for Serial Powered Systems'**. In: Proc. of the European Solid-State Device Conference, ESSCIRC 2009 (2009), pp. 276–279. doi: 10.1109/ESSCIRC.2009.5325974.
  - L. Gonella, M. Barbero, F. Huegging et al. **'The shunt-LDO regulator to power the upgraded ATLAS pixel detector'**. In: JINST 7 (2012), p. C01034. doi: 10.1088/1748-0221/7/01/C01034.
  - L. Gonella et al. **'Performance evaluation of a serially powered pixel detector prototype for the HL-LHC'**. In: JINST 12.03 (2017), P03004. DOI: 10.1088/1748-0221/12/03/P03004.
  - V. Filimonov et al. **'A serial powering pixel stave prototype for the ATLAS ITk upgrade'**. In: JINST 12.03 (2017), p. C03045. DOI: 10.1088/1748-0221/12/03/C03045.

Literature

- Shunt-LDO in 65 nm
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  - M. Karagounis, Evolution of the SLDO Regulator, talk, 2022, (ask Laura for the slides)
  - F. Winkler, Verification of Shunt-LDO, Master Thesis, 2019 https://d-nb.info/1237320216/34
  - J. Kampkötter et al. 'Stabilization and Protection of the Shunt-LDO regulator for the HL-LHC pixel detector upgrades', PoS (TWEPP2019) 067