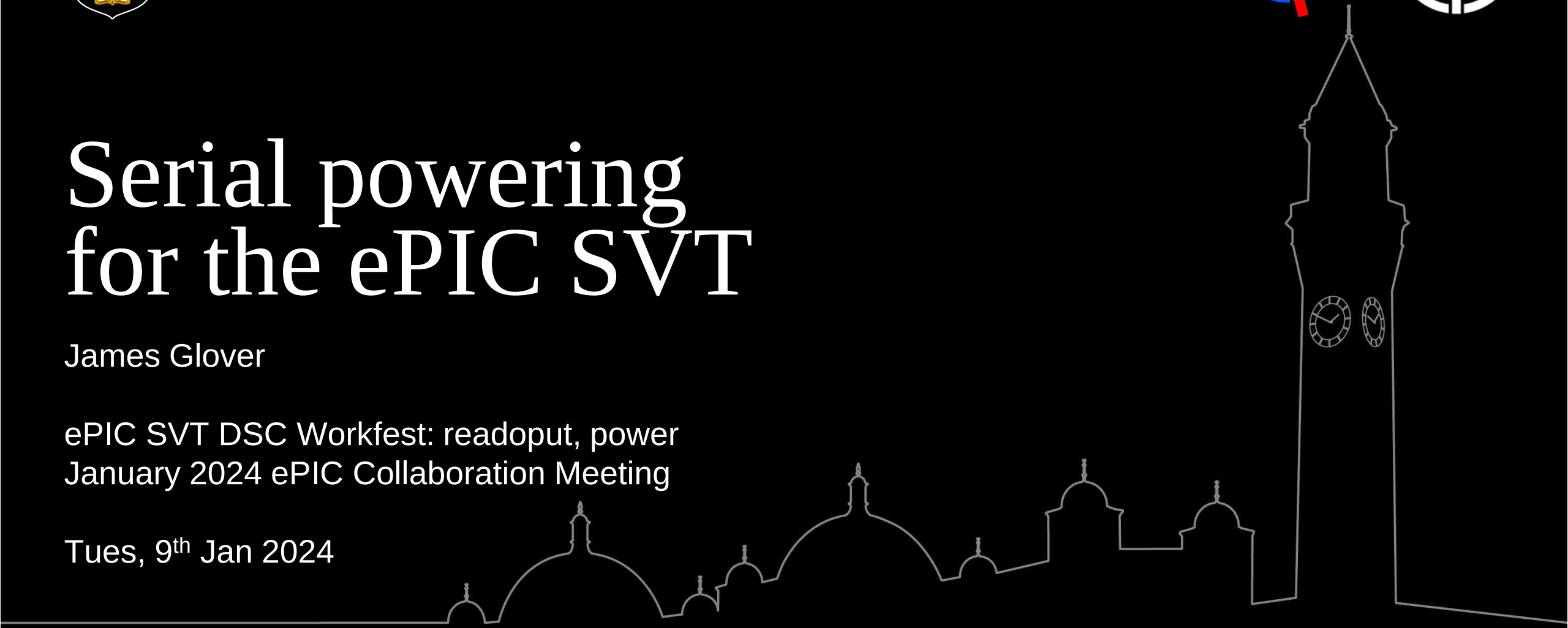


Serial powering for the ePIC SVT

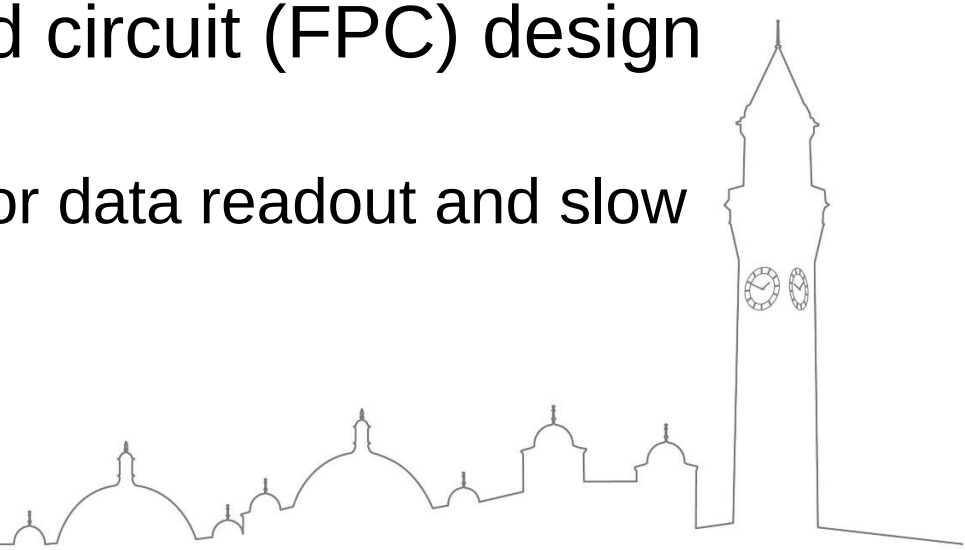
James Glover

ePIC SVT DSC Workfest: readoput, power
January 2024 ePIC Collaboration Meeting

Tues, 9th Jan 2024

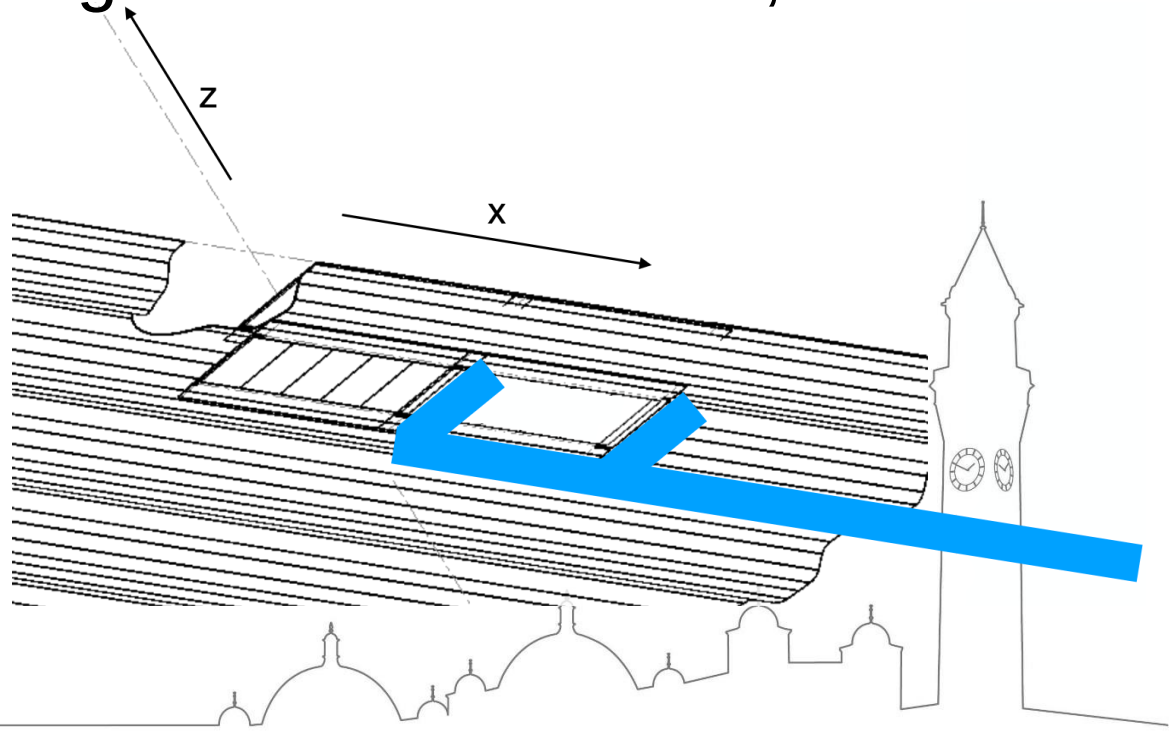
Reminder and prerequisites

- EIC-LAS to be used for OB, EE, and HE.
- Serial powering (SP) to be used for OB, EE, and HE.
- Multiple EIC-LAS needed in a SP chain (reduces material).
- Some redundancy required (e.g. don’t want a whole stave in one SP chain, in case chain is lost).
- SP chains need to fit in with flexible printed circuit (FPC) design requirements.
  - FPC needs to be designed with connections for data readout and slow controls (not just powering).

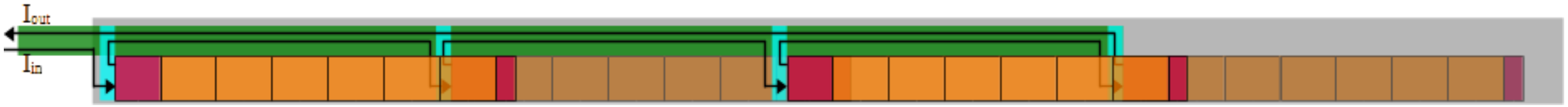


Readout recommends cluster size

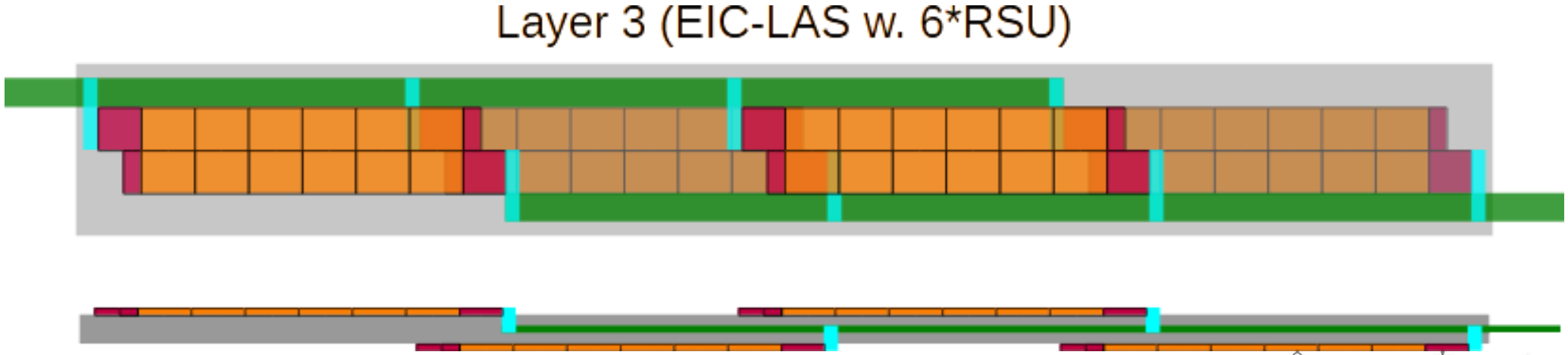
- Recent VTRx+ planning for the readout has showed a preference for clusters of 4 EIC-LAS (each EIC-LAS to have 1 multiplexed data link, for all RSUs, with 4 links available on a single VTRx+).
- (Current) stave designs are considering double-side staves, the width of 2 EIC-LAS.
- FPC designs are preferring clusters 1 EIC-LAS wide (even if interfacing sensors on different sides of the same structure).



SP in these FPCs

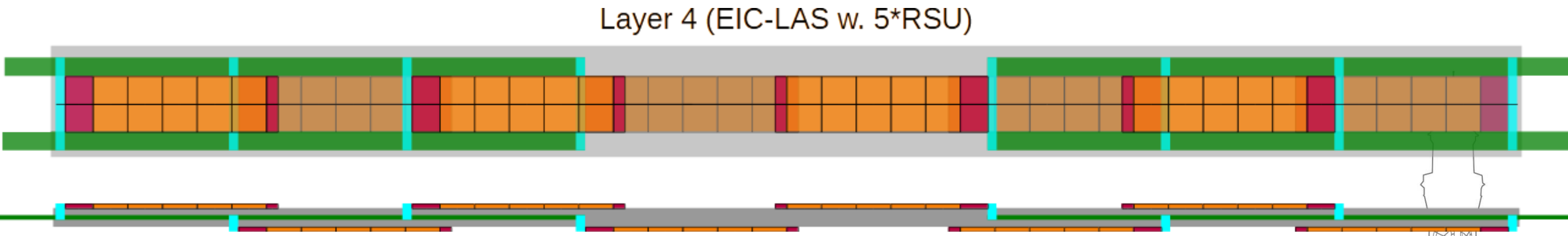


- A serial powering chain could therefore run along a length of a stave (like structure).
- A convenient layout for L3 (with 6 RSUs) could look as follows:

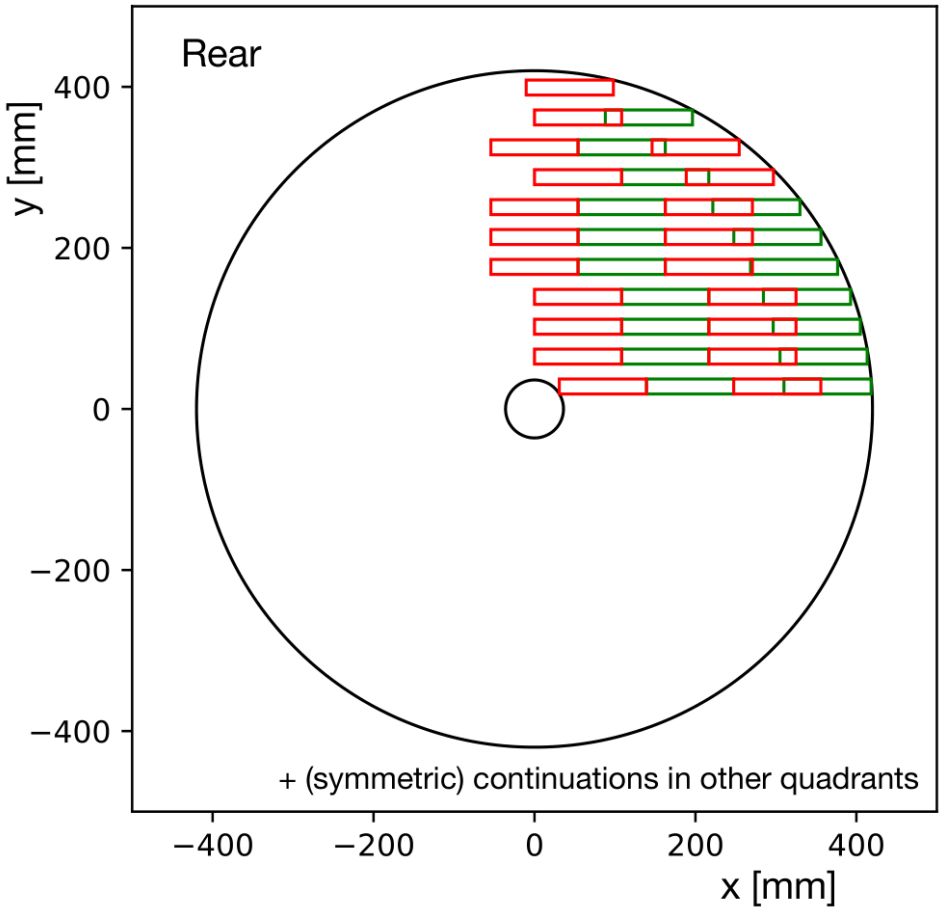


Longer staves

- To optimise the utilisation of readout links and minimise the material needed for SP chains, lengths of 4 EIC-LAS are optimal.
- This may lead to needing some overlap of RSUs to get to the best stave lengths (even if RSUs per EIC-LAS are reduced).



Endcap Disks



Need to consider options when shorter structures are required.

- Larger y coordinates in the plot (←).
- Clusters of < 4 EIC-LAS would be inefficient (less of a benefit from SP).
- Linking neighbouring structures together would increase complexity of the FPC.
  - Multiple FPC designs.
  - Some designs may only be needed in small numbers.

ITS3 ER2 expected power domains

Power Domains and Currents

Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analog	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
Global digital	GDVDD-GDVSS	1.2 to 1.32	1369	Yes	Yes
Serializers	TXVDD-TXVSS	1.8	200	Yes	No
Substrate bias	PSUB	−1.2 to 0			

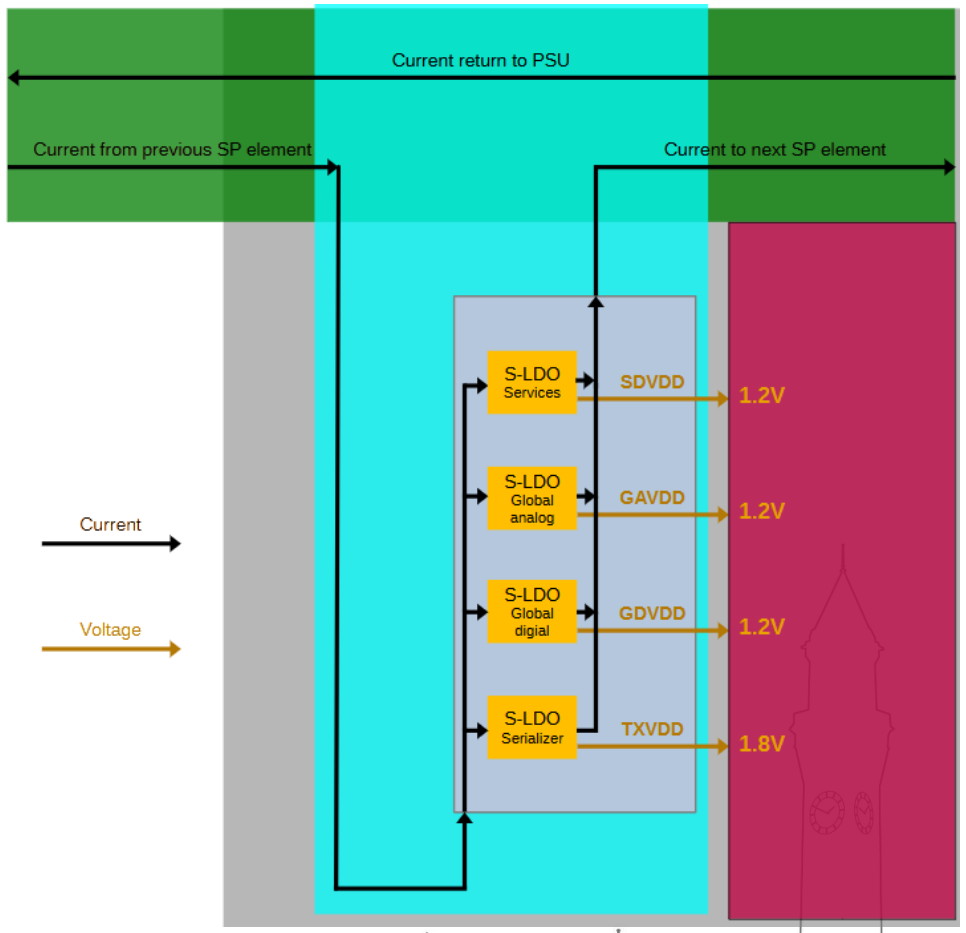
Table 3.11: Power domains of one sensor segment. The substrate bias is common to all the segments composing a sensor. The nominal operating voltage are referred to the potential of the GAVSS input net. The input currents are obtained assuming the maximum estimated power consumption of the LEC and RSU circuits at 25 °C.

From: 20th Nov '23, EP R&D WP 1.2 – G. Rinella, "Design of MOSAIX - ER2 Stitched Sensor Prototype", https://indico.cern.ch/event/1339888/contributions/5680443/attachments/2755393/4797584/20231120-ER2-Stitched-Sensor.pdf

- 3 domains all around +1.2 V.
  - Services
  - Global analog
  - Global digital
- 1 Serializers domain at +1.8 V.
- 1 Substrate bias domain at -1.2 V.

1 S-LDO per (+ve) domain

- 4 S-LDOs would be needed (in parallel).
  - Services (up to 1.32 V and 227 mA).
  - Global analog (up to 1.32 V and 540 mA).
  - Global digital (up to 1.32 V and 1369 mA).
  - Serializers (up to 1.8 V and 200 mA).
- A S-LDO would be needed to run at 1.2(to 1.32) or 1.8 V and be able to shunt (O)1.4 A.
- What about redundancy?
  - Per EIC-LAS and per SP chain.



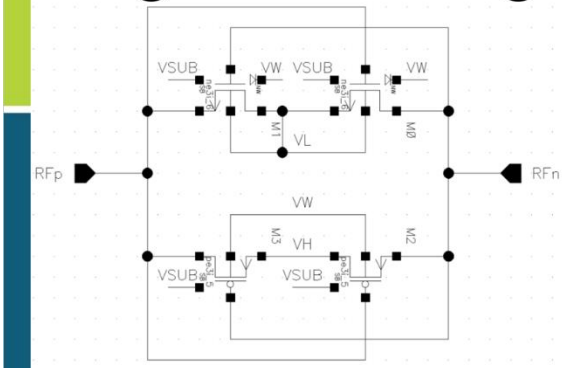
Redundancy options

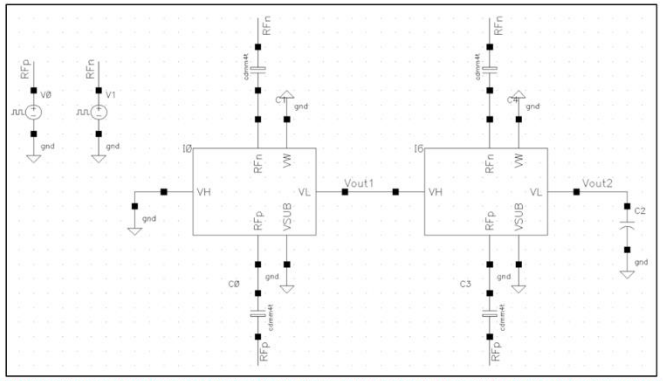
1. 1 S-LDO failure, kills 1 EIC-LAS, but keeps SP chain.
   - 4 S-LDOs per EIC-LAS.
   - If any 1 fails, the EIC-LAS is lost.
   - If all S-LDO can shunt (O)1.4 A, up to 2 (on the same EIC-LAS) can fail before the SP chain is lost.
2. Redundancy for each S-LDO (2 per domain).
   - 8 S-LDOs per EIC-LAS (more material).
   - Master/slave relationship (slave only supplies domain if master has failed).
   - Requires additional circuitry (and material), on top of the additional S-LDO.
   - Any (single) S-LDO failure does not affect the detector performance.
   - 2 S-LDOs (for the same domain) would have to fail before losing an EIC-LAS.
   - Up to 2 domains (on the same EIC-LAS) can fail before the SP chain is lost.

Substrate bias domain

From: 9th Jan ’24, ePIC CM@ANL – G. Deptuch, “EIC-LAS ancillary / support IC”, https://indico.bnl.gov/event/20473/contributions/84985/attachments/51831/88643/ePIC_SVT_MAPS_design_org.pptx

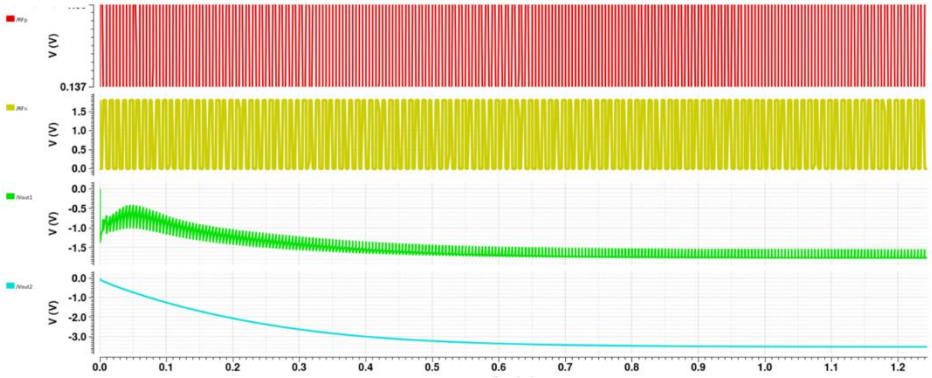
Negative Voltage Generator





Preliminary:

Vout2 = -3.6 V



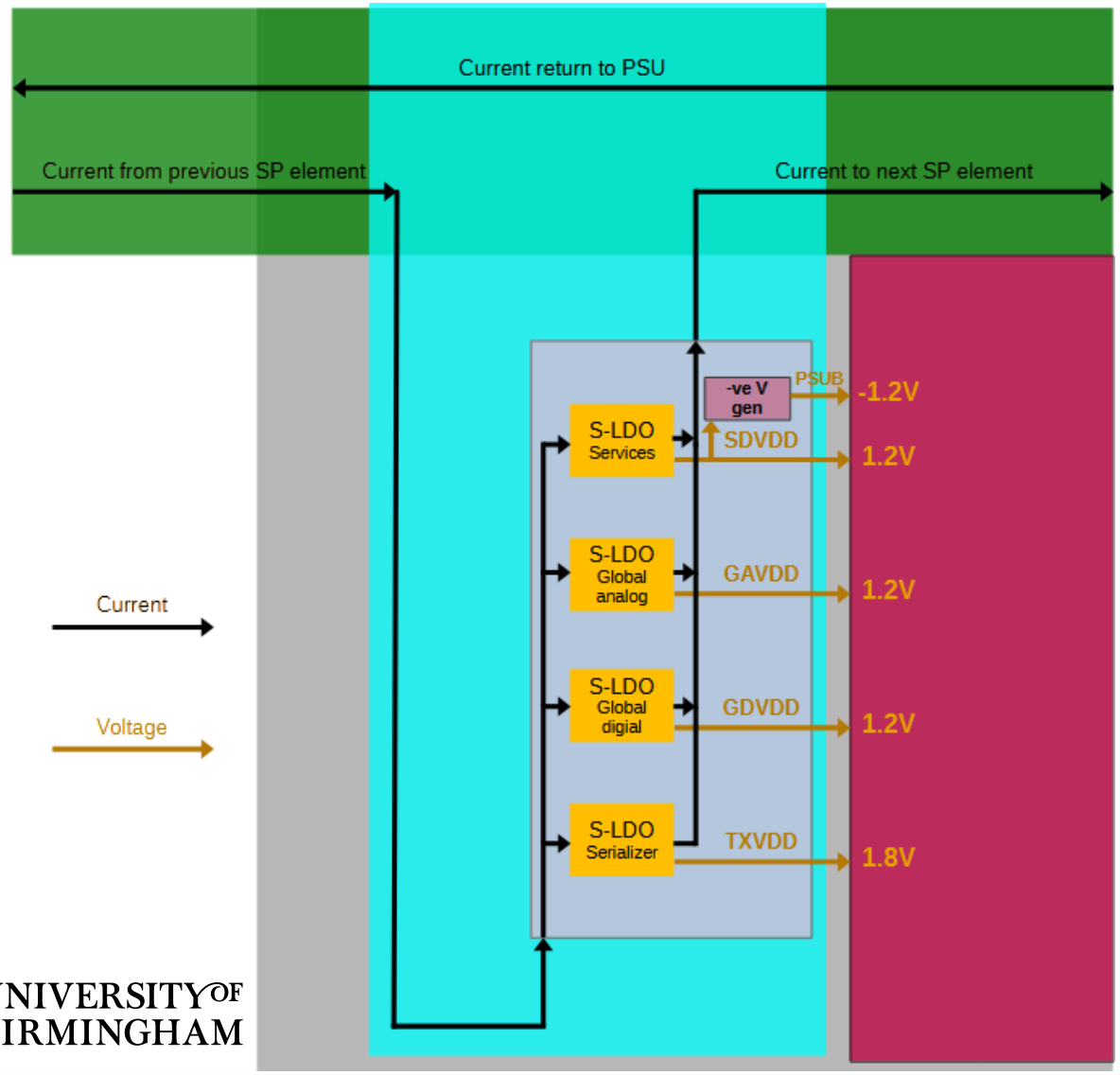
- The S-LDO configurations only cover the positive voltage power domains.
- A -1.2 V domain is needed for the substrate of the chip.
- Can not be supplied in a parallel powering scheme.
  - Each EIC-LAS in the SP chain will have a difference ground reference.
  - The -1.2 V must be referenced to the specific EIC-LAS’s ground.

4

Brookhaven National Laboratory

UNIVERSITY OF BIRMINGHAM

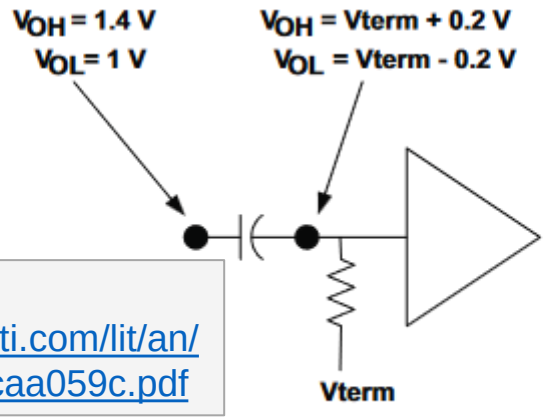
S-LDO config per EIC-LAS



- Basic configuration overview (no redundancy shown).
- Negative voltage generator could run from any of the 4 S-LDO domain voltages.
  - Just shown on Services as this is lowest power.

AC-coupled data transmission

- Due to SP (separate ground reference per EIC-LAS), data transmission will need to be AC-coupled (to separate the DC offset from the signal).
- Details of the proposed scheme are still a work in progress and many questions are still to be checked and answered.
- This should only affect the OB, EH, and HH (where the EIC-LAS and SP are used).
- The IB is looking to repeat the DC-coupled scheme as used by ITS3 (the details of which are still be worked out).



From: https://www.ti.com/lit/an/scaa059c/scaa059c.pdf

Figure 1. AC-Coupling to Shift Common-Mode Voltage

AC-coupled data transmission Qs

- What is a realistic distance the signal needs to travel without the signal integrity degrading?
  - To be answered. Aim to have some tests done prior to TDR.
- Do we have anyone (already in the collaboration) with hands-on experience that can assist with design and testing? If not, who (outside the collaboration) could be good to bounce ideas off?
  - Some ideas for people in UK to ask, but not all part of the collaboration.
- Do we have DC-balanced protocols for data and slow control and self-biased receivers?
  - Also effects the DC-coupled readout (in IB). DC-balancing is a feature of lpGBT (so already part of the chip design from ITS3). Slow controls are undecided as whether to use the lpGBT as well (current default solution) or a custom protocol through an FPGA.

Time to start setting priorities

Must balance:

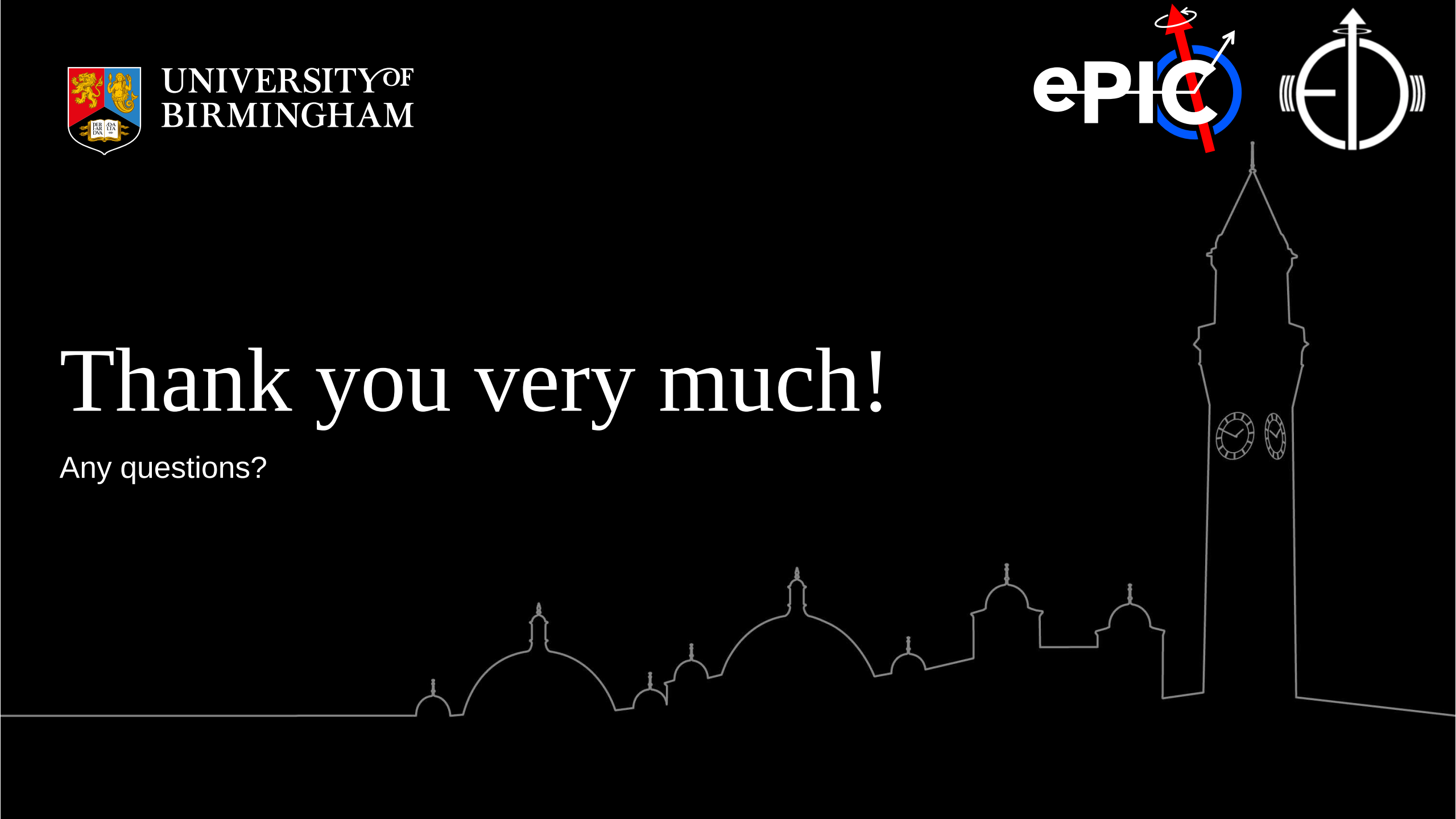
- Material budget.
- Redundancy.
- Power density (heat).
- Design (FPC, staves and disks) requirements and complexity.
- Number of unique configurations.

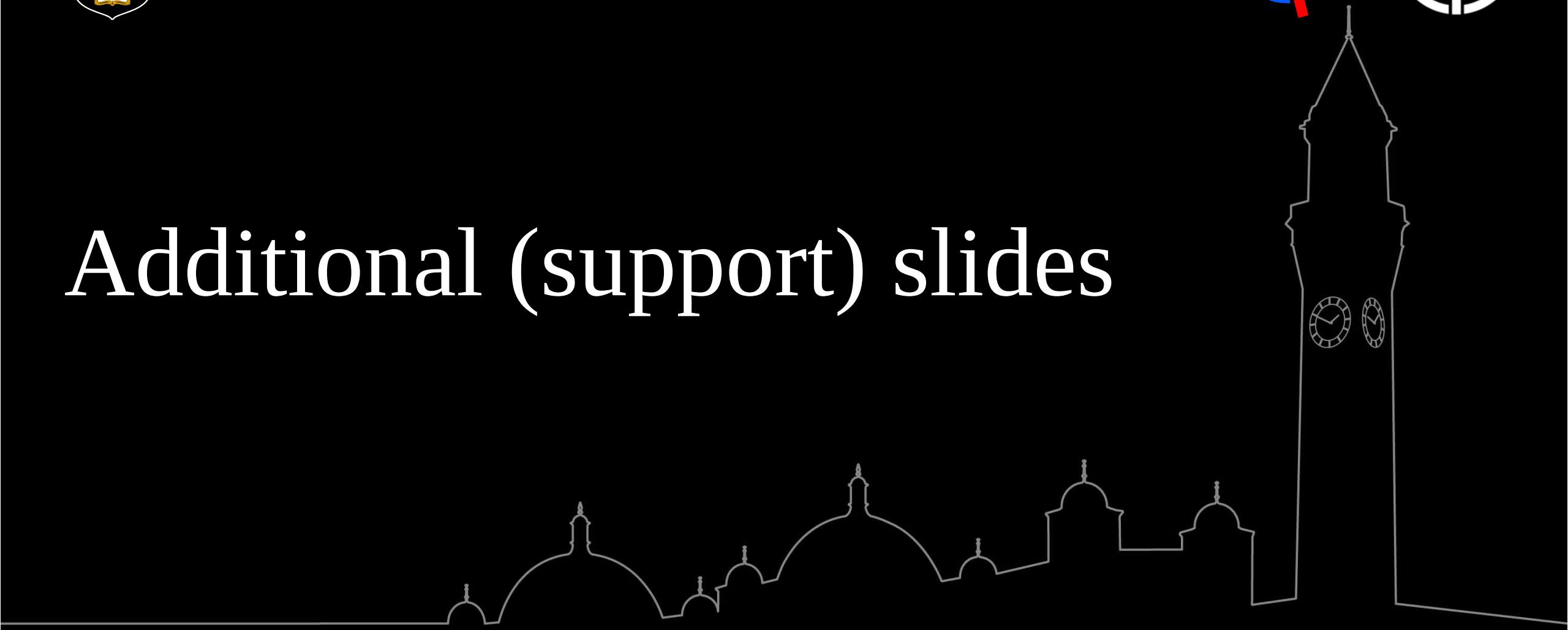
It is not currently clear which of these should be the highest priority.

Summary

- SP scheme for the ePIC SVT is progressing.
- Many questions still need to be answered.
- Many things need to be balanced with other areas of the SVT:
  - Readout system
  - Chip design.
  - Local mechanics.
  - FPC development.

- The SP requires AC-coupled data transmission. It should be a priority to have for a potential scheme prior to the TDR.


UNIVERSITY OF BIRMINGHAM
ePIC
Thank you very much!
Any questions?



Additional (support) slides

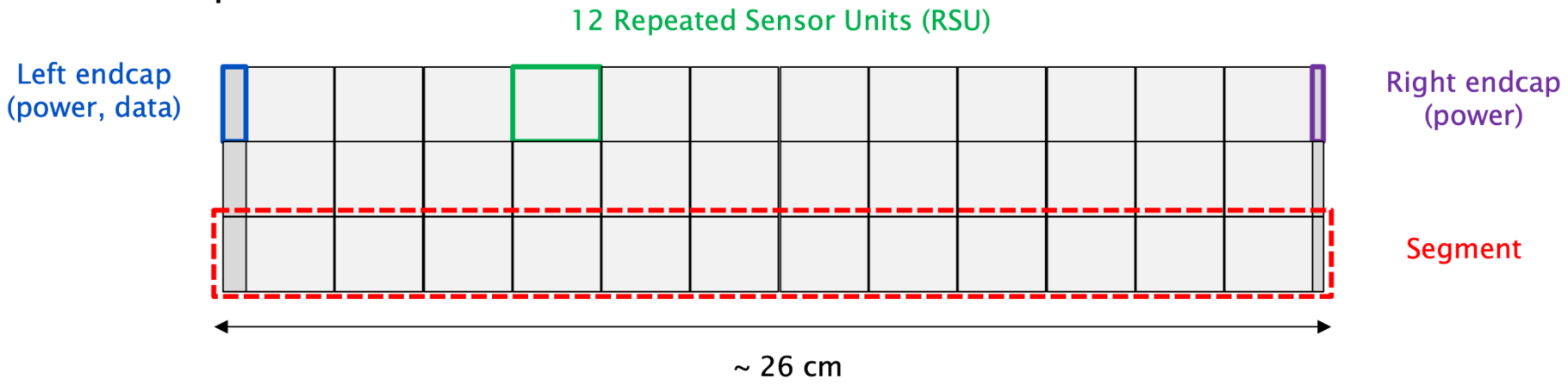
Background Studies

Brings together material from multiple previous meetings, in particular:

- 30th Jan ’23, SC meeting – L. Gonella, “Powering scheme for the ePIC SVT”, https://indico.bnl.gov/event/18202/
- 29th Mar ’23, UK SVT SP meeting, https://indico.cern.ch/event/1269506/
- 8th Aug ’23, SVT meeting – P. Jones, “Update on outer barrel and endcaps (disks) tiling study”, https://indico.bnl.gov/event/20219/
  - Updated, 22nd Aug ’23, SVT, https://indico.bnl.gov/event/20336/
- 19th Jul ’23, EIC-UK WP1 – J.Glover, “Status and plans for powering studies - updates on sensor design”, https://indico.bnl.gov/event/19981/
- 22nd Aug ’23, SVT meeting – E. Sichtermann, “Update on disks and tiling”, https://indico.bnl.gov/event/20336/
- 14th Nov ’23, SVT meeting – J. Schambach, “SVT Readout”, https://indico.bnl.gov/event/21207/
- 20th Nov ’23, UK EIC-LAS & S-LDO discussion, https://indico.bnl.gov/event/21215/
- 28th Nov ’23, SVT meeting – J. Glover, “Outer Barrel Layout Considerations”, https://indico.bnl.gov/event/21355/
- 28th Nov ’23, SVT meeting – E. Sichtermann, “Update on disks”, https://indico.bnl.gov/event/21355
- 12th Dec ’23, SVT meeting – J. Glover, “Serial powering architecture”, https://indico.bnl.gov/event/21518/

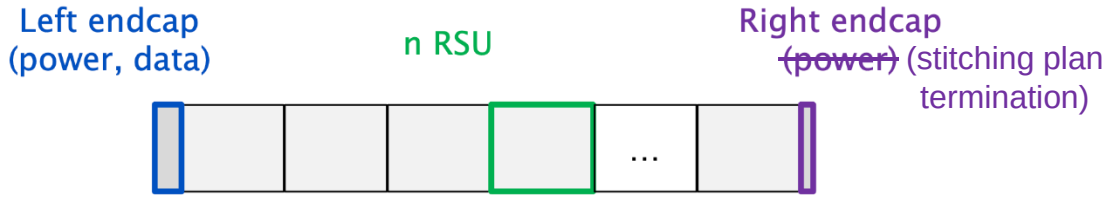
Chip structures and layouts

Example: L0 sensor

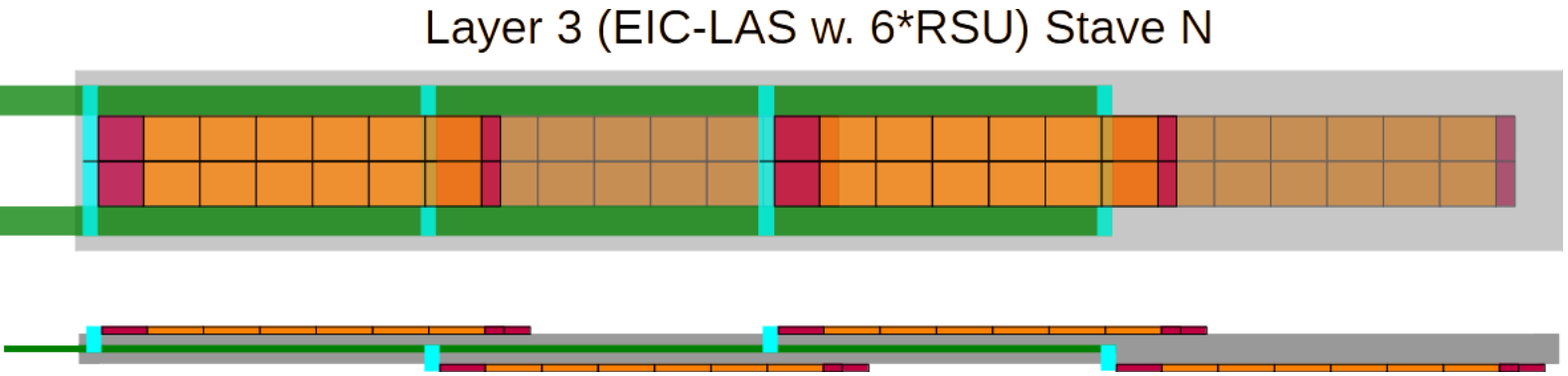


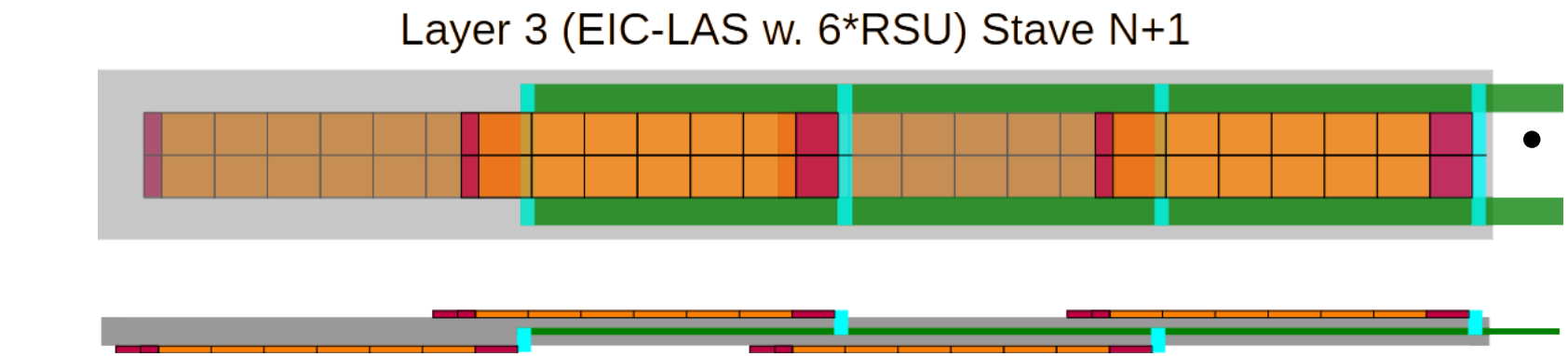
From:
https://wiki.bnl.gov/EPIC/index.php?title=Si_Vertex_Tracker

EIC LAS



More likely L3 (6RSU) layout





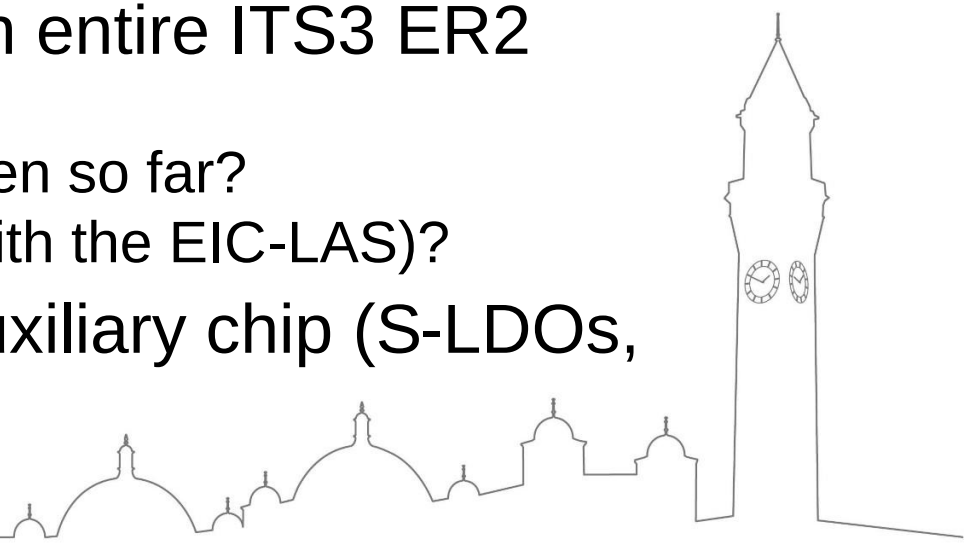
- EIC-LAS may be diced 2 segments wide (easier mounting).
- Therefore, both FPCs need to come from the same stave edge.
- Alternating staves would need to be connected to from opposite sides (to balance material).

Power consumption

- 4 S-LDOs (domains):
  - Services (up to 1.32 V and 227 mA) → ~0.30 W
  - Global analog (up to 1.32 V and 540 mA) → ~0.71 W
  - Global digital (up to 1.32 V and 1369 mA) → ~1.81 W
  - Serializers (up to 1.8 V and 200 mA) → ~0.36 W
- 1 extra domain for substrate bias.
  - -1.2 V at < 1 mA → ~1 mW

Total ≈ 3.2 W

- These power values are assumed to be for an entire ITS3 ER2 segment (12RSUs with both endcaps).
  - How does this fit with power density estimates given so far?
  - How much does this reduce for fewer RSUs (as with the EIC-LAS)?
- Some additional power will be used for our auxiliary chip (S-LDOs, negative voltage generator & multiplexer).

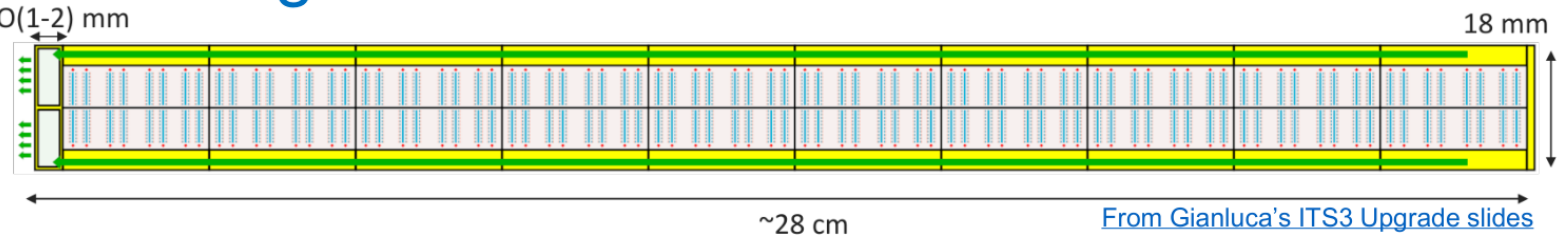


Ground reference per EIC-LAS

UNIVERSITY OF BIRMINGHAM

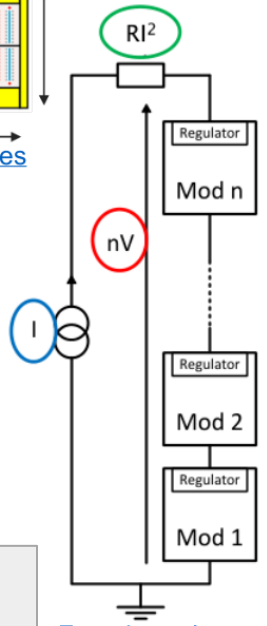
Birmingham Instrumentation Laboratory for Particle physics and Applications (BILPA)

Things to remember.



From Gianluca's ITS3 Upgrade slides

- Serial powering (SP) requires all modules in the SP chain to have a different ground reference to the other modules in the chain (GND of Mod_N becomes V_{in} of Mod_{N+1}), with only the final module in reference to the power supply ground.
- Each RSU in the MOSS is not electrically isolated, therefore the whole MOSS must have the same GND reference.
  - ∴ The 2 endcaps cannot be in series to each other!
  - How do you get power to both endcaps (in a SP scheme)?



From Laura's EIC SC slides

From: 19th Jul '23, EIC-UK WP1 – J.Glover, "Status and plans for powering studies - updates on sensor design", https://indico.bnl.gov/event/19981/contributions/78770/attachments/48692/82811/23-07-19_Serial_Powering_JGlover_V3.pdf

- 1 of the reasons why EIC-LAS should contain fewer RSUs than ITS3.
- Explains issue of ground reference per Mod (EIC-LAS) in a SP chain.
- Based on information from ITS3's ER1 submission (not ER2).

Alternative to 1 S-LDO per domain

Instead of needing 4 S-LDOs (+ redundancies, shunting (O)1.4 A) per EIC-LAS. 1 S-LDO (+ redundancy, shunting > 2.5 A) could supply the whole EIC-LAS (all domains).

- Would require regulators to generate the different voltages requires (+1.2, +1.8, -1.2 V) and split up supply for the different domains.
- These regulators would also need some redundancy.
- This S-LDO would have a very high power density (the power for the whole EIC-LAS in a chip likely to be < 1 cm^2) and therefore very hot.
  - Could be a big challenge for the cooling system.

Complex lengths

- Lengths of EIC-LAS that do not contains a multiple of end up being less efficient in terms of utilised read-out links and SP chain length.