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Flexible Printed Circuits (FPCs) for ePIC-SVT: considerations on design

WP3: Electrical interfaces

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Outline

- Overview of WP3 Electrical Interfaces.
- Material budget.
- Inner Barrel (IB), Outer Barrel (OB) and Disks layout.
- Sensor design and auxiliary components enabling a low material budget FPC.
- Case study of an FPC layout.
- Manufacturing technology.
- Conclusions

Reporting a snapshot
of the evolutionary development
of the SVT & FPC

Overview of WP3 Electrical Interfaces

Work package (WP) description:

- Inner Barrel:
  - wire-bonding of bent sensors to FPC, incl. tooling;
  - FPC from end of bent sensors to readout boards;

- Outer Barrel and Disks:
  - wire-bonding of sensor to FPC, incl. tooling;
  - FPC from sensors to end of stave/disks;
  - FPC from end of stave/disks to readout boards;

WP3 started in Sept.2023

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Work break-down structure

WP3: Electrical interfaces		
3.1	Hybrid integrated circuits (HICs) for IB, OB and disks	
3.1.1	IB HIC (L0-2)	
3.1.1.1		Specifications of IB HICs (flexible printed circuits (FPCs), mechanical to
3.1.1.2		Design of FPCs and mechanical tools
3.1.1.3		Suppliers evaluation and procurement
3.1.1.4		Prototyping, including testing
3.1.1.5		Iterative improvements of HIC design & assembly techniques
3.1.1.6		Pre-production, including testing
3.1.1.7		Production of detector grade HIC, including QC
3.1.2	OB HIC (L3-4)	
3.1.2.1		Specifications of OB HIC (flexible printed circuits (FPCs), mechanical to
3.1.2.2		Design of FPCs and mechanical tools
3.1.2.3		Suppliers evaluation and procurement
3.1.2.4		Prototyping, including testing
3.1.2.5		Iterative improvements of HIC design & assembly techniques
3.1.2.6		Pre-production, including testing
3.1.2.7		Production of detector grade HICs, including QC
3.1.3	Disks HIC (ED0-4, HD0-4)	
3.1.3.1		Specifications of ED/HD HICs (flexible printed circuits (FPCs), mechani tools)
3.1.3.2		Design of FPCs and mechanical tools
3.1.3.3		Suppliers evaluation and procurement
3.1.3.4		Prototyping, including testing
3.1.3.5		Iterative improvements of HIC design & assembly techniques
3.1.3.6		Pre-production, including testing
3.1.3.7		Production of detector grade HICs, including QC

Material budget

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Material budget (1/2)

- Considering the material budget as the main constraint for the FPC design.
- This is because the material budget impacts the physics performance of the detector (e.g. angular resolution of tracks).
- The material budget sets limitations on FPC like no. of layers, and thickness and material of conductors and insulators deployed in manufacturing.
- The break-down of the material budget from ALICE ITS2 and ITS3 is taken as reference.

Material budget (2/2)

EIC SVT target material budgets

Wafer scale sensor

IB	r [mm]	l [mm]	X/X0 %
L0	36	270	0.05
L1	48	270	0.05
L2	120	270	0.05

Only 50um Si

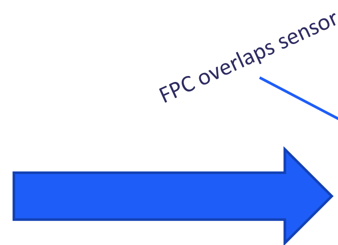
LAS T5

OB	r [mm]	l [mm]	X/X0 %
Layer 3	270	540	0.25
Layer 4	420	840	0.55

LAS T5

DISKS	+z [mm]	-z [mm]	r_out [mm]	X/X0 %
Disk 0	250	-250	240	0.25
Disk 1	450	-450	420	0.25
Disk 2	700	-650	420	0.25
Disk 3	1000	-850	420	0.25
Disk 4	1350	-1050	420	0.25

J. Glover
Current and future tracking and vertexing detectors
7 Nov 2023



FPC overlaps sensor

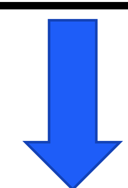
B Abelev et al and The ALICE Collaboration 2014 J. Phys. G: Nucl. Part. Phys. 41 087002

Table 4.1: Estimated contributions of the Inner Layer Stave to the material budget.

Stave element	Component	Material	Thickness (μm)	X_0 (cm)	X_0 (%)
HIC	FPC Metal layers	Aluminium	50	8.896	0.056
	FPC Insulating layers	Polyimide	100	28.41	0.035
	Pixel Chip	Silicon	50	9.369	0.053
Cold Plate		Carbon fleece	40	106.80	0.004
		Carbon paper	30	26.56	0.011
	Cooling tube wall	Polyimide	25	28.41	0.003
	Cooling fluid	Water		35.76	0.032
	Carbon plate	Carbon fibre	70	26.08	0.027
	Glue	Eccobond 45	100	44.37	0.023
Space Frame		Carbon rowing			0.018
Total					0.262

ITS2 IB stave length ~270mm, width ~1.5cm, ALPIDE PWR <40m W/cm2

Target material budget HIC: 0.144 % X/X0



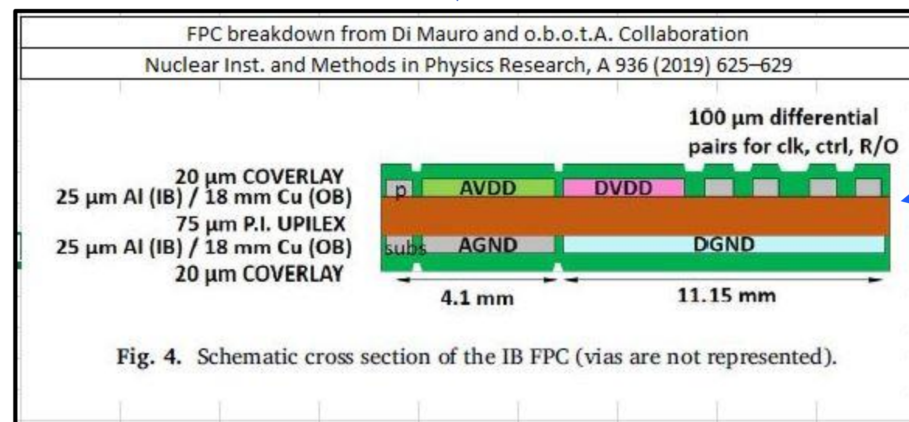


Fig. 4. Schematic cross section of the IB FPC (vias are not represented).

Target material budget FPC: 0.096 % X/X0

Two layers FPC, w Al tracks, w impedance matched tracks

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Material budget & impedance matching

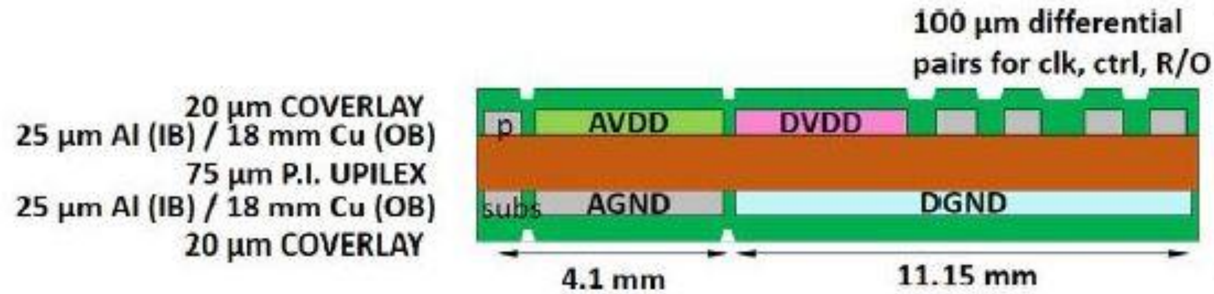
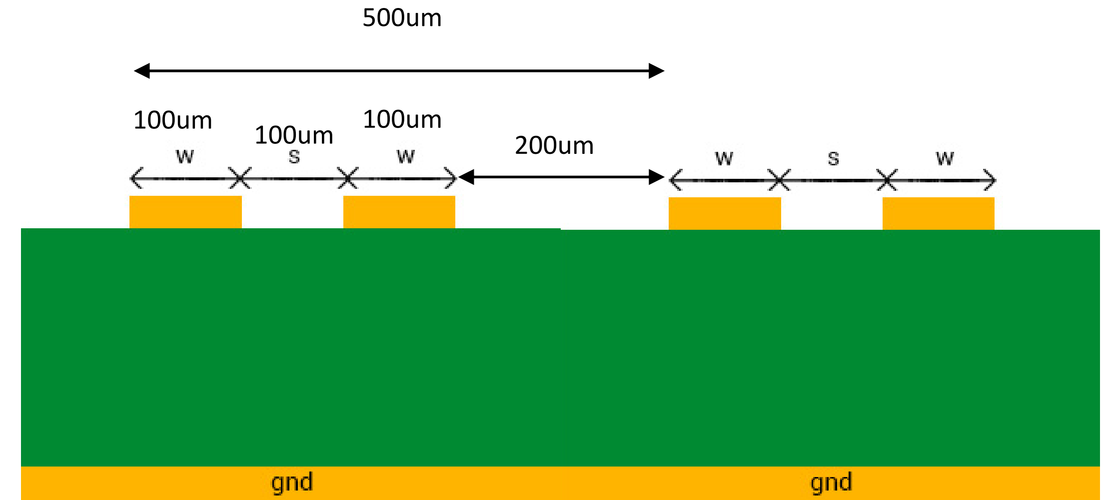

FPC breakdown from Di Mauro and o.b.o.t.A. Collaboration
Nuclear Inst. and Methods in Physics Research, A 936 (2019) 625–629

Fig. 4. Schematic cross section of the IB FPC (vias are not represented).

Differential pair dimensions for ALICE ITS2 IB FPC



Sanity check on impedance

OK ~100 ohm impedance for 100um diff pairs

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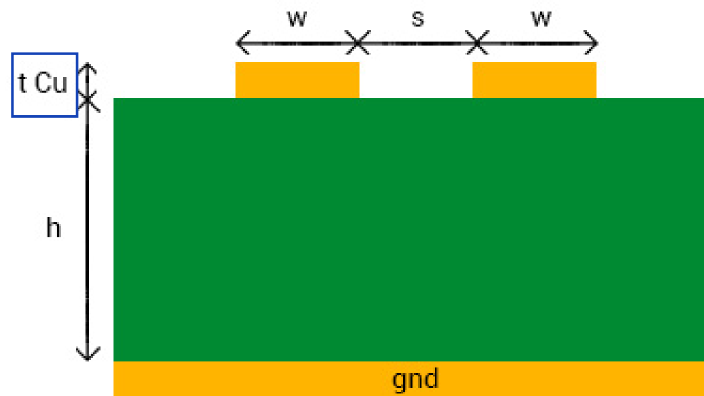
Edge-Coupled Surface Microstrip



s	100	um	Track space
w	100	um	Track width
t Cu	25	um	Track height
h	75	um	Isolation height
Er	3.5		Dielectric constant (FR4 - Standard: 4.3)
Z_0	61.7	Ω	Impedance ca.
Z_{Diff}	123.4	Ω	Impedance ca.

IB, OB and Disks layout

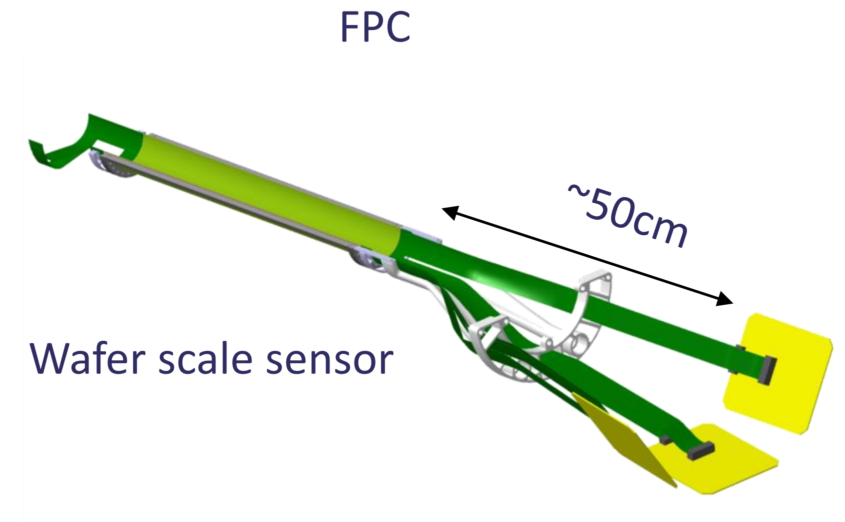
Images from several ALICE ITS3 contributions

IB: L0, L1, L2 – barrel layout

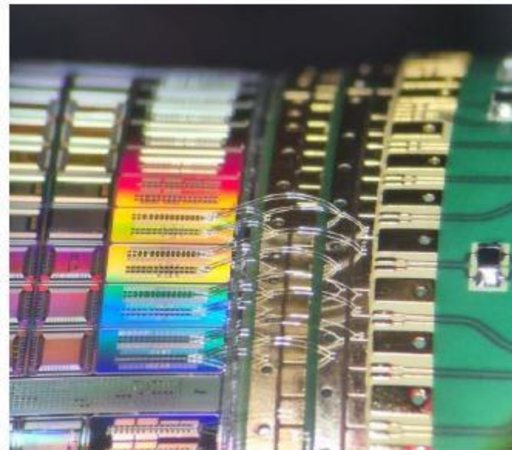
- L0,L1,L2 only 50um Si:
  - No FPC overlapping sensor;
    - No restrictions in no. of conductive layers in the FPC;
  - FPC made of **Cu tracks and planes**.

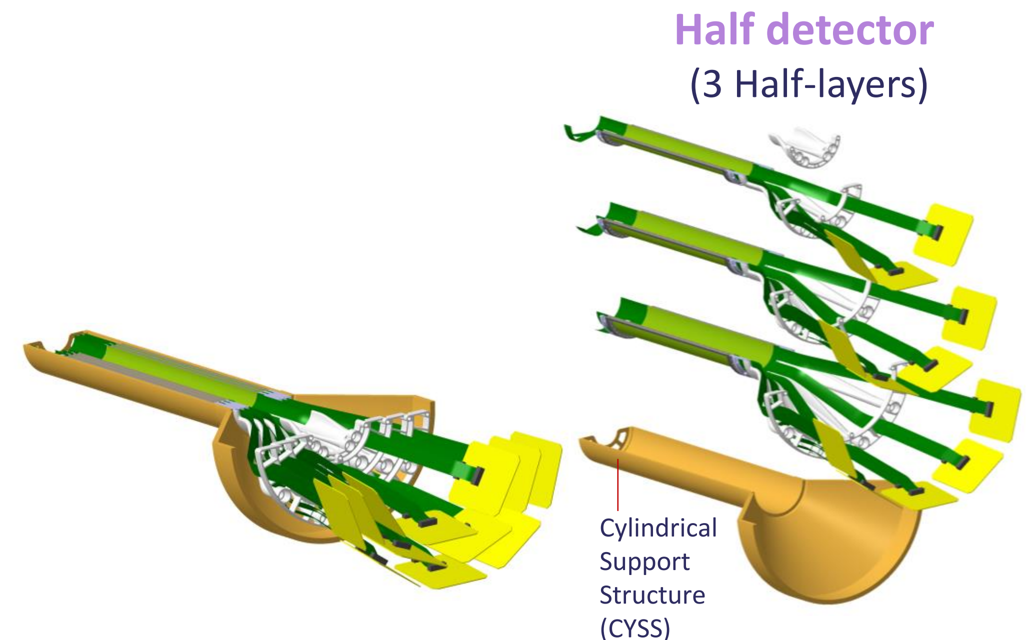
- FPC interconnected via wire-bonding to sensor end caps:
  - Left end cap: data, ctrl, clk, pwr, gnd;
  - Right end cap: pwr, gnd;

- Rationale: to **re-use** as much as possible the design from ALICE ITS3;
- If mods to FPCs are required:
  - access FPC design files (Cadence Allegro) and modify them;



FPC wire bonded to curved sensors





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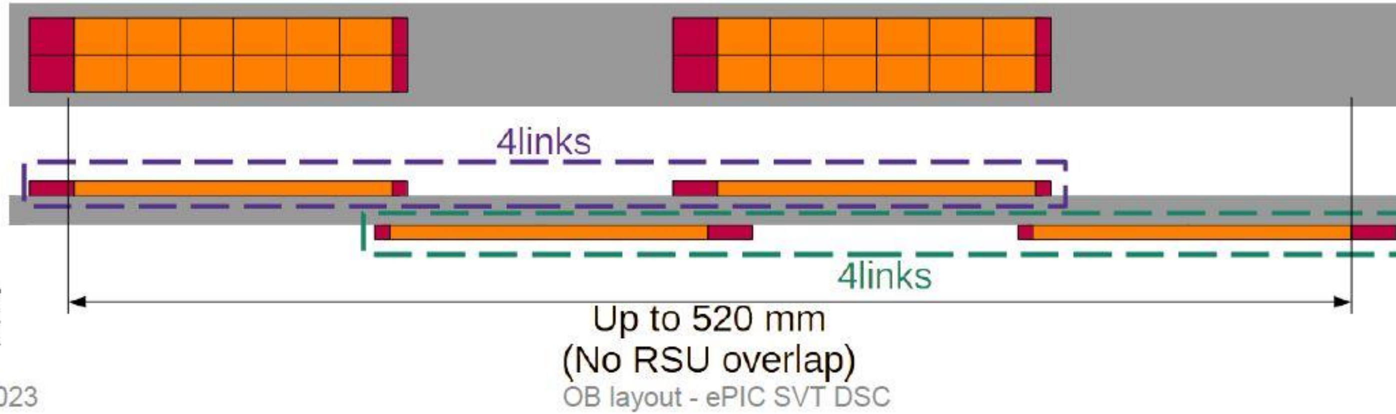
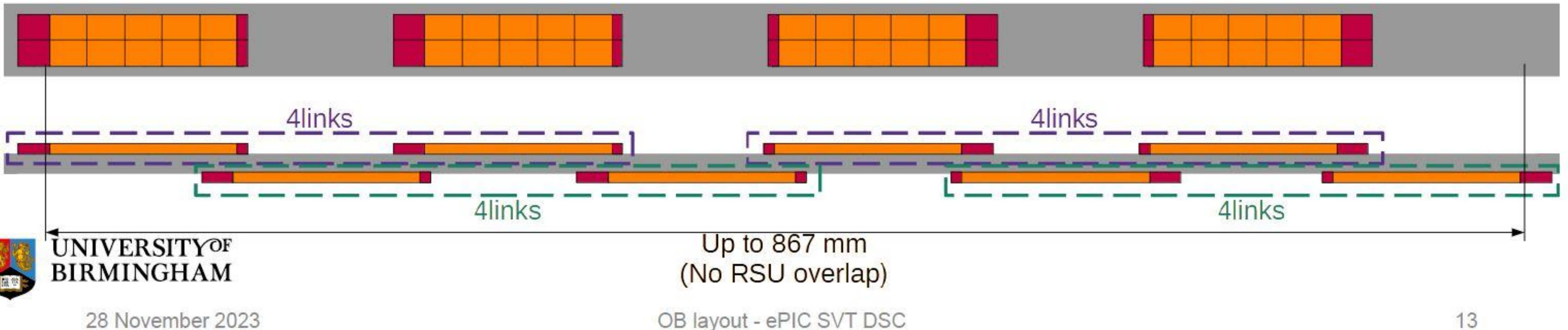
OB: L3, L4 - stave layout

Credit J.Glover



Assumptions:

- Sensor mounted on front and back sides of the cold plate;
- LEC overlaps REC;
- Services to the stave from the left and right sides;



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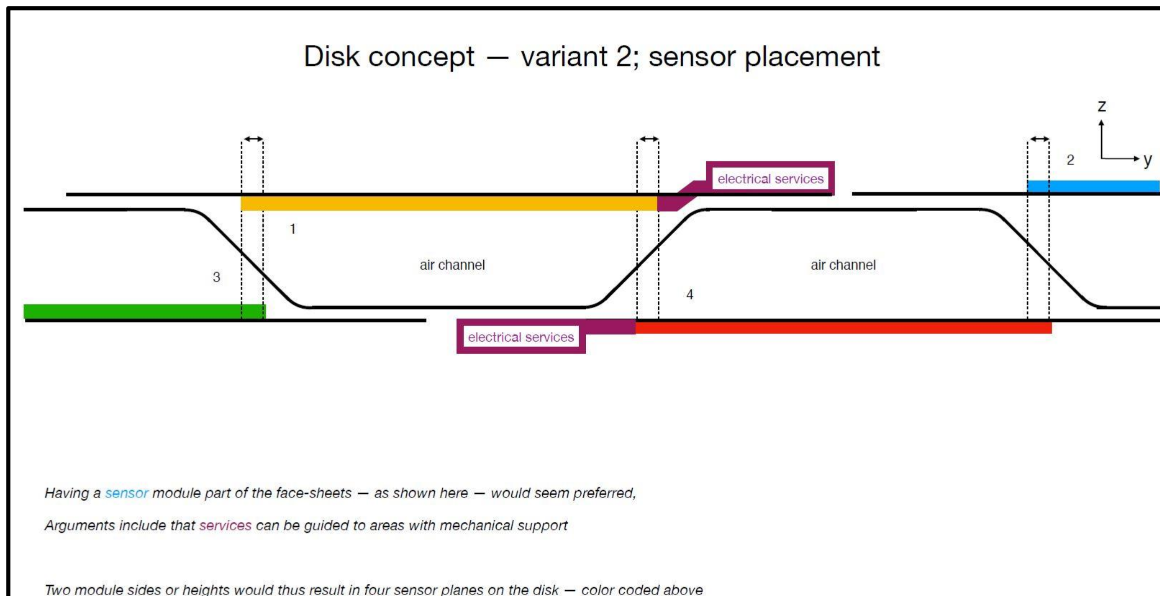
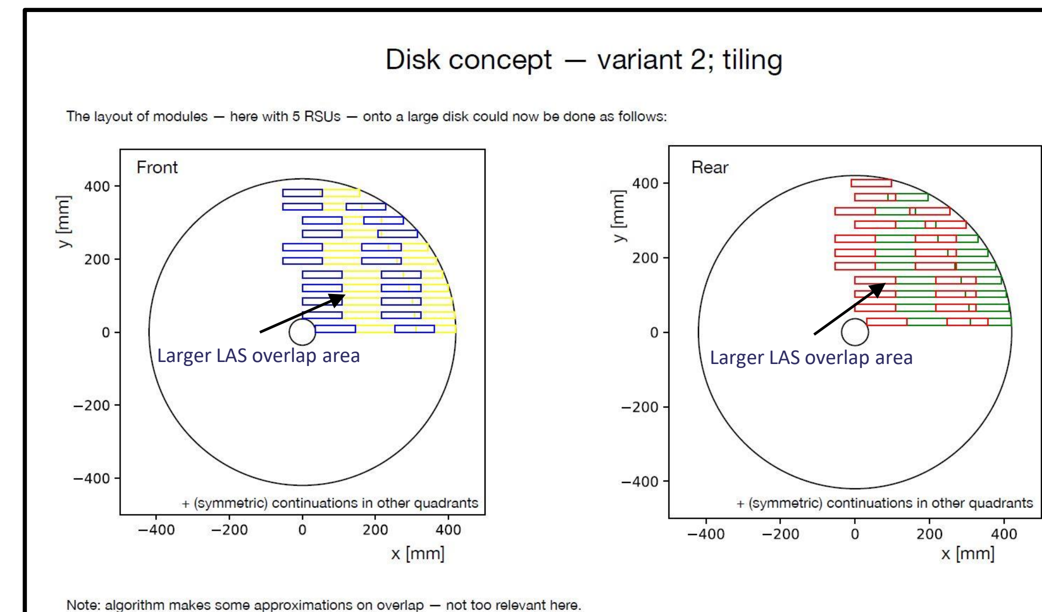
FPC will overlap the active area of sensors and
it will impact the material budget of the active area of the Si tracker

Disks: Electron and hadron - layout configuration

Credit E.Sichtermann, N.Apadula

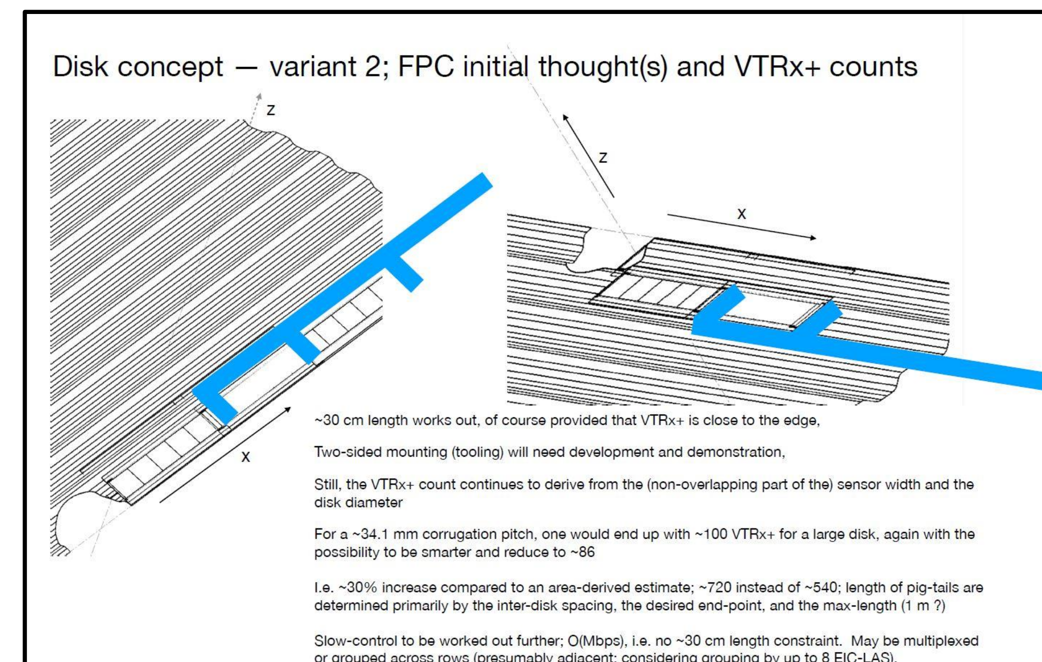




Assumptions:

- Sensor mounted on front and back sides of the cold plate;
- LEC overlaps REC;
- Services to the disks from outer radius;

Note:
Only T5 LAS considered for tiling disks;



FPC will overlap the active area of sensors and
it will impact the material budget of the active area of the tracker

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Sensor design and auxiliary components enabling a low material budget FPC

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FPC overview (only OB and Disks)

- We achieve a low material budget by:
  - designing a 2 layers FPC w a width <=19mm;
  - manufacturing the FPC w Al tracks and planes;

- This is dependent on the activities related to:
  - sensor design (i.e. internal data multiplexing)
  - design of auxiliary components to optimise power and control signal distribution.

- Multiplexing:
  - MOSAIX has a total of 8 diff lines for data transmission.
  - MOSAIX has a total of 8 diff lines for control and clock:
    - Power Management (PM), Slow Control (SC), Synchronisation (SYNC), Global Reset (GRTS), Global Clock (GCLK), Reserve;

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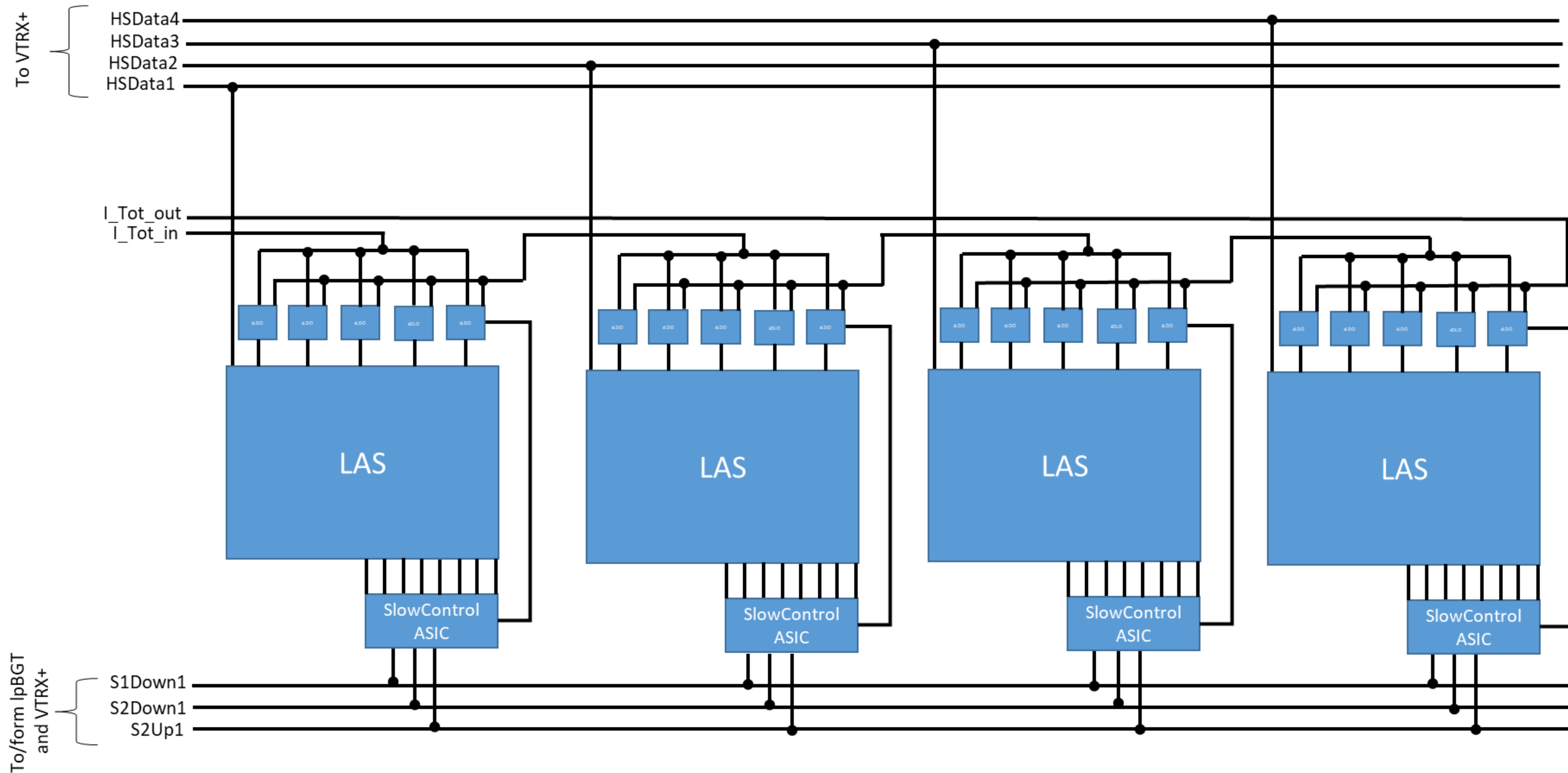
- Foot-print per LAS: (16 diff lines) x (500 um/diff line) = 8 mm/LAS
- **Foot-print 4 LAS: 8mm x 4 = 32 mm (~1.7 x LAS width (19mm))**

Block diagram for a sequence of 4 LAS (1/2)



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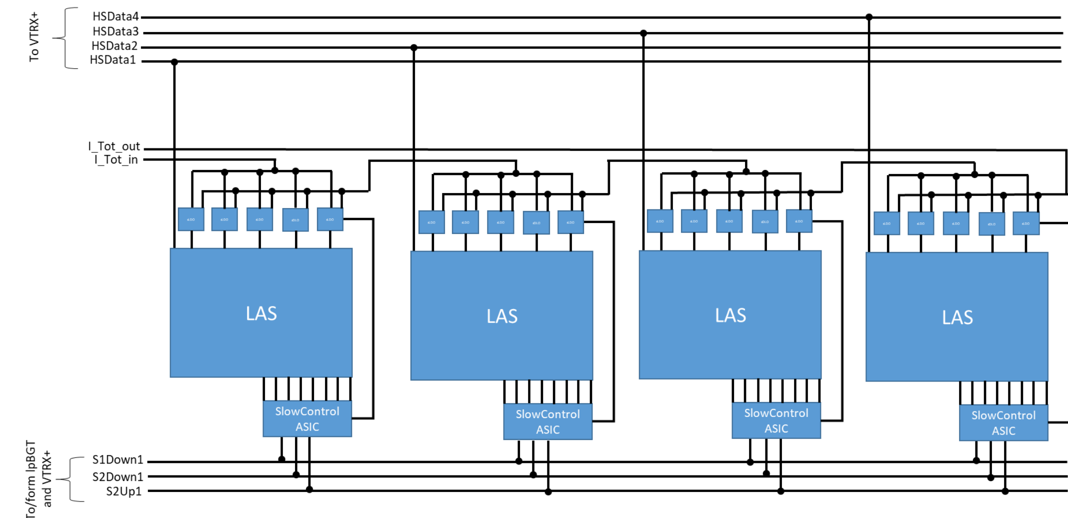
Block diagram for a sequence of 4 LAS (2/2)

- A total of 7 differential lines every 4 LAS:
    - 2 diff lines for control;
    - 1 diff line for global clock;
    - 4 diff lines for HS data:
- **Foot-print 4 LAS: (7 diff lines) x (500um/diff lines) = 3.5mm**
- % fill factor of LAS width (19mm): (3.5/19)*100 = 18%
    - It was 84%+84%=168% originally!

- Signal ratings considerations:
    - Slow control: 5Mb/s (or 10Mb/s);
    - Global clock: 160MHz (or 320MHz);
    - Data speed 5.12 Gb/s (or 10Gb/s TBC);
    - Expected highest ΔV ~10V ((~2.5V /LAS) x (4 LAS));
    - Highest current ~2.5 A;



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Case study of an FPC layout

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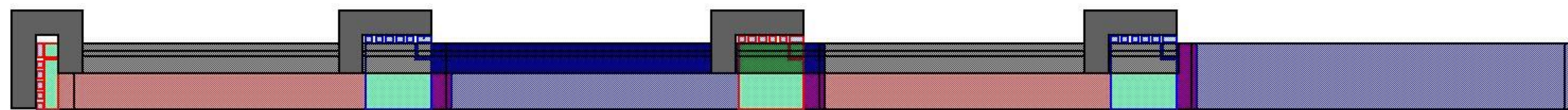
FPC overview (mainly focussing on OB L4)

- To aim is to produce a semi-quantitative sketch of the layout implementing the circuit described above.
- A sequence of 4 LAS is considered: longest sequence of sensors in the entire SVT.
- Product break down:
  - 4 LAS T5 (2 front; 2 back);
  - Auxiliary ASICs (per LAS: 5 sLDO; 1 SlowControl ASIC);
  - Interposer FPC per LAS
  - Common bus FPC



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Disclaimer: I made an assumption on the implementation of the auxiliary ASICs, mainly form the factor.

BOM (so far)

LAS: notes

Supplies and I/Os

Supplies
I/Os
Supplies
I/Os
Supplies
I/Os
Supplies
Supplies
Supplies

Slow control
down
up
down
down
down
down
down
up

PSUB
GAVDD/GAVSS
GDVDD/GDVSS
HSDATATOP[0]
HSDATATOP[1]
HSDATATOP[2]
PSUB
GAVDD/GAVSS
GDVDD/GDVSS
PMWR
PMRD
GCLK
GRST
SYNC
RESERVE
SCWR
SCRD
PSUB
GAVDD/GAVSS
GDVDD/GDVSS
HSDATABOT[2]
HSDATABOT[1]
HSDATABOT[0]
PSUB
GAVDD/GAVSS
GDVDD/GDVSS

All I/Os are differential

6x 5.12 Gb/s data outputs
1x clock at 160 MHz (possibly 320 MHz?)
2x slow control at 5 Mbps (possibly 10 Mbps?)
(slow controls via lpGBT: 1 clk, 4 elink down, 2 elink up, 1 spare)

Global analog and digital supplies per *segment*

On-chip supply segmentation and control

Reverse biasing of substrate (PSUB)

Oak Ridge National Laboratory

Power Domains and Currents

CERN

Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analog	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
Global digital	GDVDD-GDVSS	1.2 to 1.32	1369	Yes	Yes
Serializers	TXVDD-TXVSS	1.8	200	Yes	No
Substrate bias	PSUB	−1.2 to 0			

NEW, EXTRA PADS? THERE IS NO REFERENCE T THESE IN PREVI US LEC CONNECTION SCHEMES.

Table 3.11: Power domains of one sensor segment. The substrate bias is common to all the segments composing a sensor. The nominal operating voltage are referred to the potential of the GAVSS input net. The input currents are obtained assuming the maximum estimated power consumption of the LEC and RSU circuits at 25 °C.

Assuming:

- LAS is T5 only
- 1 high speed data line
- 5 power domains

“My datasheet”

Pin-out description

LAS	S_GLCK+	Input	down	160MHz (or 320MHz)	Clk
	S_GLCK-	Input	down		
	S_PMWR+	Input	down	5Mbps (10Mbps)	Slow ctrl
	S_PMWR-	Input	down		
	S_PMRD+	Output	up	5Mbps (10Mbps)	
	S_PMRD-	Output	up		
	S_SCWR+	Input	down	5Mbps (10Mbps)	
	S_SCWR-	Input	down		
	S_SCRD+	Output	up	5Mbps (10Mbps)	
	S_SCRD-	Output	up		
	S_GRST+	Input	down		
	S_GRST-	Input	down		
	G_SYNC+	Input	down		
	G_SYNC-	Input	down		
	G_RESERVE+	N/A			
	G_RESERVE-	N/A			
	HSDATA+	Output	up	5.12 Gb/s	Data
	HSDATA-	Output	up		
	SDVDD	Input		1.2 to 1.32 V (services) (227mA)	Pwr
	SDVSS	Input			
	GAVDDS	Input		1.2 to 1.32 V (global analogue) (540mA)	
	GAVSS	Input			
	GDVDD	Input		1.2 to 1.32 V (global digital) (1369mA)	
	GDVSS	Input			
	TXVDD	Input		1.8 V (serialisers) (200mA)	
	TXVSS	Input			
	PSUB	Input			Sensor bias
	PSUBGND	Input			

Physical layout

	l (mm)	w (mm)
RSU	21.666	19.564
LEC	4.5	19.564
REC	1.5	19.564
T5 LAS	114.33	19.564
T6 LAS	135.996	19.564

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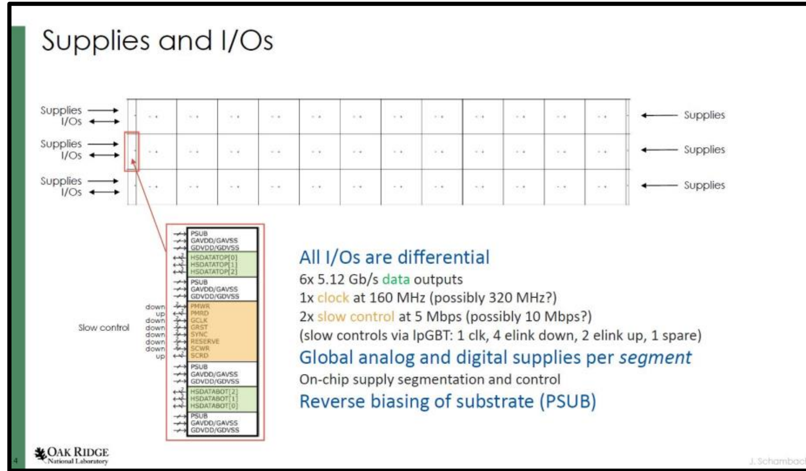
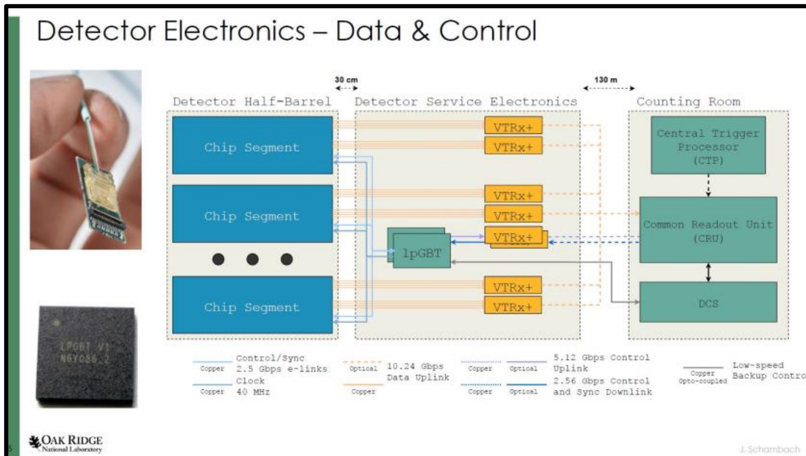
SlowControl ASIC





Assuming:

- 1 SlowControl ASIC per LAS
- The SlowControl ASIC is pwr'd via one of the existing sLDOs
- SlowControl ASIC size: 4mm x 2mm

"My datasheet"

Pin-out description

	Pin	Type	Direction	Description
slowCtrlChip	S1down+	Input	down	1 CONTROL link (down) carries MUX'd: (PMWR, SCWR, RST, SYNC)
	S1down-	Input	down	
	S2down+	Input	down	1 link for GCLK Assuming that global clock gets buffered
	S2down-	Input	down	
	S1up+	Output	up	1 Ctrl link (up) carries MUX'd PMRD(up) and SCRD(up)
	S1up-	Output	up	
	S_GLCK+	Output	down	160MHz (or 320MHz)
	S_GLCK-	Output	down	
	S_PMWR+	Output	down	5Mbps (10Mbps)
	S_PMWR-	Output	down	
	S_PMRD+	Input	up	5Mbps (10Mbps)
	S_PMRD-	Input	up	
	S_SCWR+	Output	down	5Mbps (10Mbps)
	S_SCWR-	Output	down	
	S_SCRD+	Input	up	5Mbps (10Mbps)
	S_SCRD-	Input	up	
	S_GRST+	Output	down	
	S_GRST-	Output	down	
	G_SYNC+	Output	down	
	G_SYNC-	Output	down	
	G_RESERVE+	N/A	N/A	
	G_RESERVE-	N/A	N/A	
	VDD	Input		supplied locally from sLDO multiple pads Supply voltage and power?
	GND	Input		

Physical layout

To/From lpGBPT
S1down+
S1down-
S2down+
S2down-
S1up+
S1up-
From local sLDO
VDD
GND

To/From LAS
S_GLCK+
S_GLCK-
S_PMWR+
S_PMWR-
S_PMRD+
S_PMRD-
S_SCWR+
S_SCWR-
S_SCRD+
S_SCRD-
S_GRST+
S_GRST-
S_SYNC+
S_SYNC-
RESERVE+
RESERVE-

foot print 4 mm x 2 mm

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sLDO: notes

“My datasheet”

Pin-out description

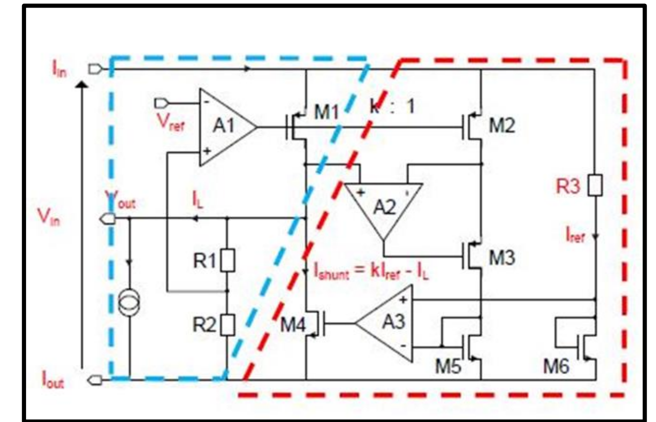
SLDO	Signal		
	I_in	input	2.5 A (or 1.7 A) (Id+ Ia) worst case scenario
	I_out	input	2.5 A (or 1.7 A) (Id+ Ia) worst case scenario
	Vout	output	4 options: SDVDD/SDVSS = 1.2 to 1.32 V (services) (227mA) GAVDD/GAVSS = 1.2 to 1.32 V (global analogue) (540mA) GDVDD/GDVSS = 1.2 to 1.32 V (global digital) (1369mA) TXVDD/TXVSS = 1.8 V (serialisers) (200mA)
			Note: PSUB -1.2 to 0 V not included

Physical layout

I_in		I_out
		Vout
foot print	2mmx2mm	

Assuming:

- 1 sLDO per pwr domain:
  - total of 5 domains
- PSUB current not specified
- sLDO size: 2mm x 2mm



Power Domains and Currents

Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analog	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
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Substrate bias	PSUB	−1.2 to 0			

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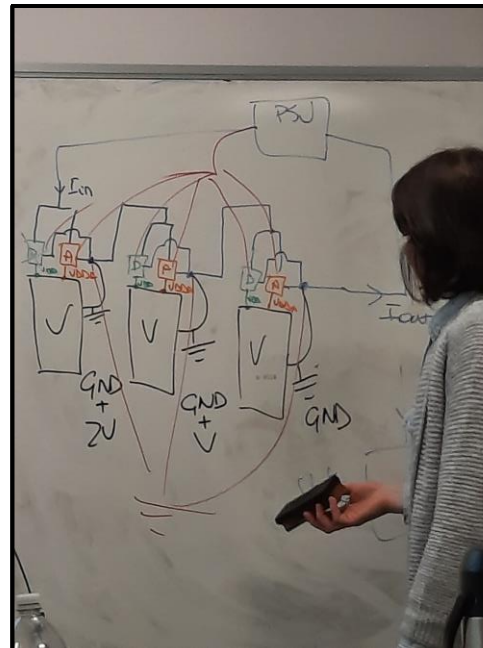
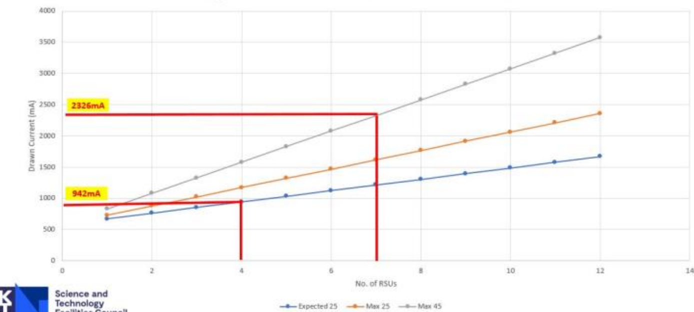
NEW, EXTRA PADS? THERE IS NO REFERENCE T THESE IN PREVIUS LEC CONNECTION SCHEMES.





Layout (so far)

LAS placement on OB L4 stave.

LAS1 back

LAS1 front

LAS2 back

LAS2 front

A sequence of 4 sensors, 0.25 of OB stave.

LAS back: (face down)
mounted on the back side of the stave;
LAS front: (face up)
mounted on the front side of the stave;

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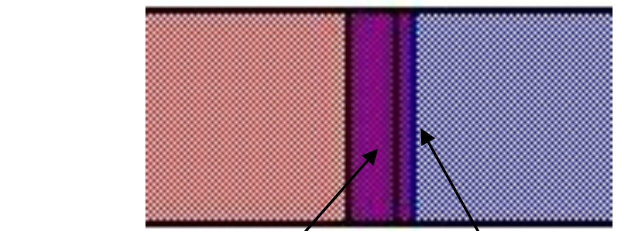
Overlap between **LAS back** and **LAS front** to reduce dead area

Zoom-in

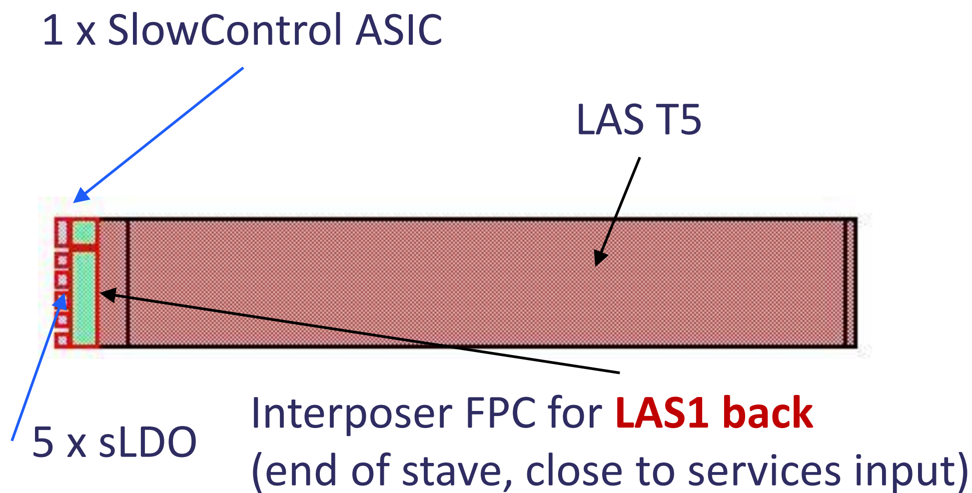


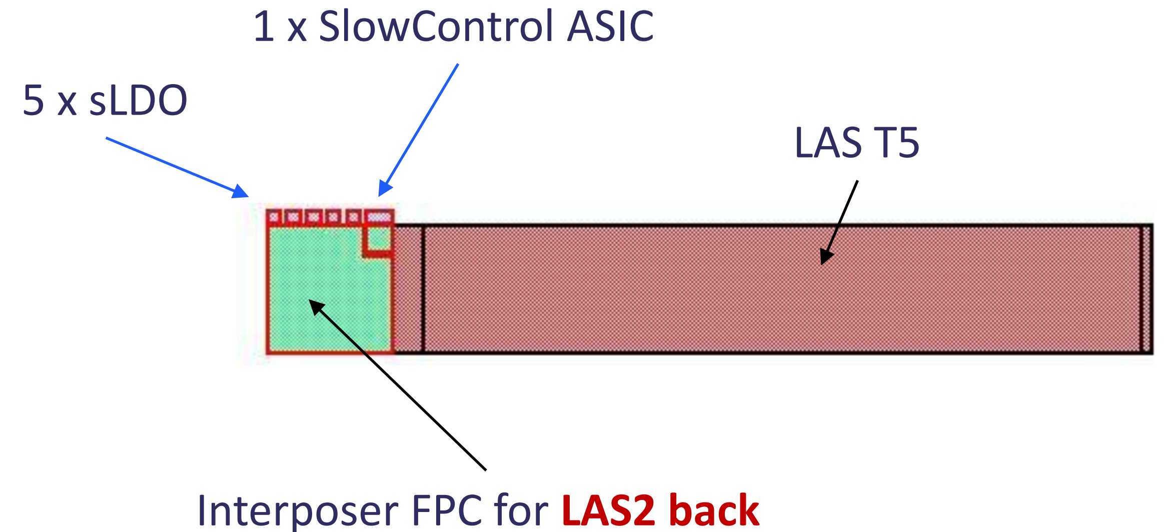
LAS1 front LEC: 4.5mm

LAS1 back REC: 1.5mm

Interposer FPC

- The interposer FPC connects the LAS to the auxiliary components
- Assumption: the auxiliary components are mounted directly onto the cold plate (less material budget)
- Assumption: the auxiliary components are mounted mainly on the side of stave for possible cooling optimisations (e.g. cooling pipe underneath)





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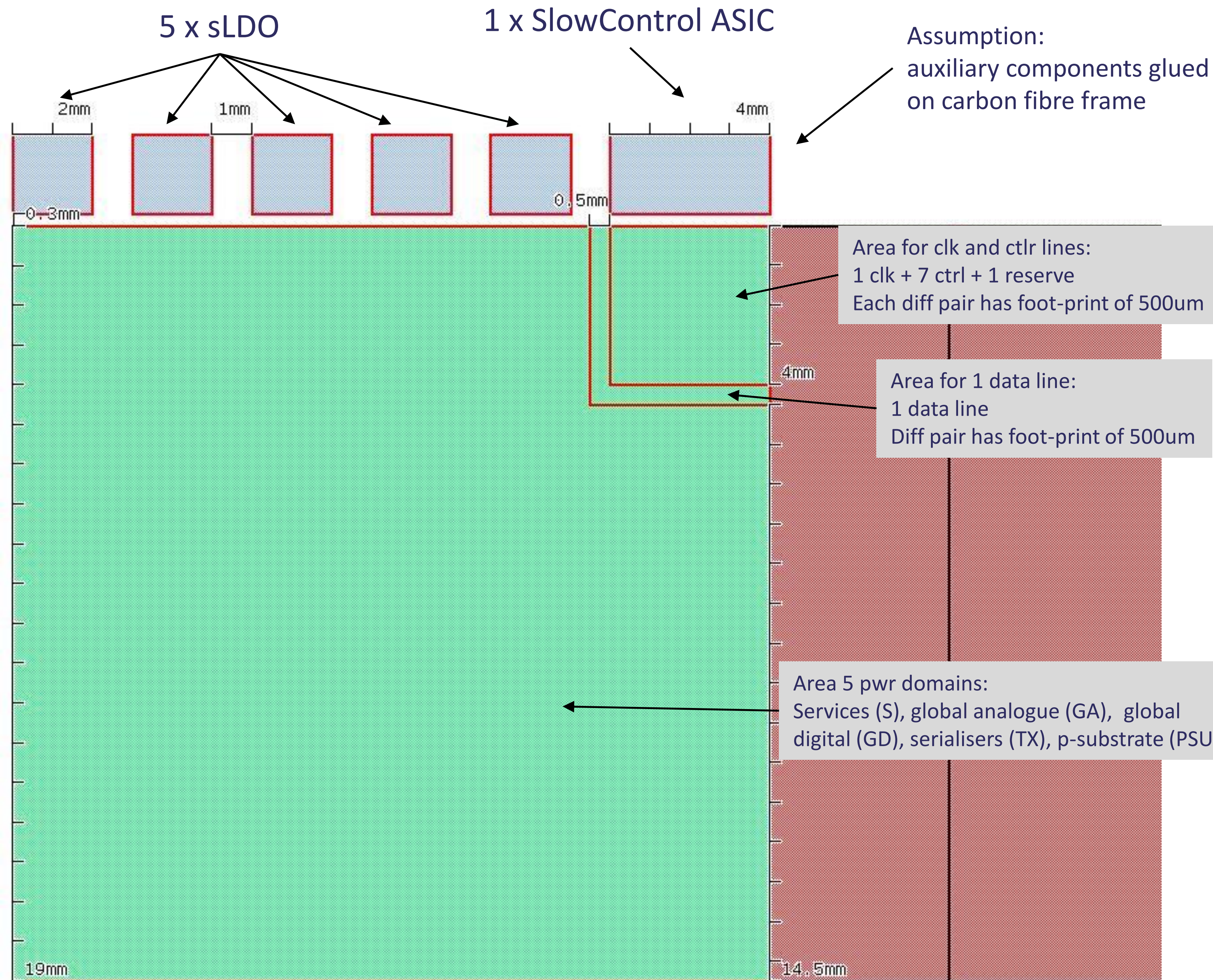
Interposer FPC

clk+ctrl: ~21% of LAS width (19mm)

data: ~2.6% of LAS width (19mm)

S+GA+GD+TX+PSUB pwr domains:
~76% of LAS width (19mm)



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Interposer FPC – voltage drops

Voltage drops for interposer FPC										
Total avaialble width [mm]		14.5	Total avaialble width w/o PSUB [mm] :			13.5				
	V (min)	V (max)	I (mA)	Al resistivity (ohm*m)	Al tickness (m)	Al length (m)	Width (m)	Al resistance (ohm)	Voltage drop (V)	% wrt V (min)
SDVDD/SDVSS	1.2	1.32	227	2.65E-08	2.50E-05	3.80E-02	1.41E-03	2.86E-02	6.49E-03	5.41E-01
GAVDD/GAVSS	1.2	1.32	540	2.65E-08	2.50E-05	3.80E-02	3.35E-03	1.20E-02	6.49E-03	5.41E-01
GDVDD/GDVSS	1.2	1.32	1369	2.65E-08	2.50E-05	3.80E-02	8.50E-03	4.74E-03	6.49E-03	5.41E-01
TXVDD/TXVSS	1.8		200	2.65E-08	2.50E-05	3.80E-02	1.24E-03	3.24E-02	6.49E-03	3.61E-01
PSUB	1.2	6	0.01	2.65E-08	2.50E-05	3.80E-02	1.00E-03	4.03E-02	4.03E-07	3.36E-05
Total w/o PSUB	N/A	N/A	2336	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Negligible voltage drops (<1%) assuming:

- Track width for PSUB 1mm;
- Track width for S,GA,GD,TX split proportionally wrt the specified current;
- 25um Al;
- Longest path in interposer 19*2mm=38mm;

Note:
Values of current refer to 12 RSU

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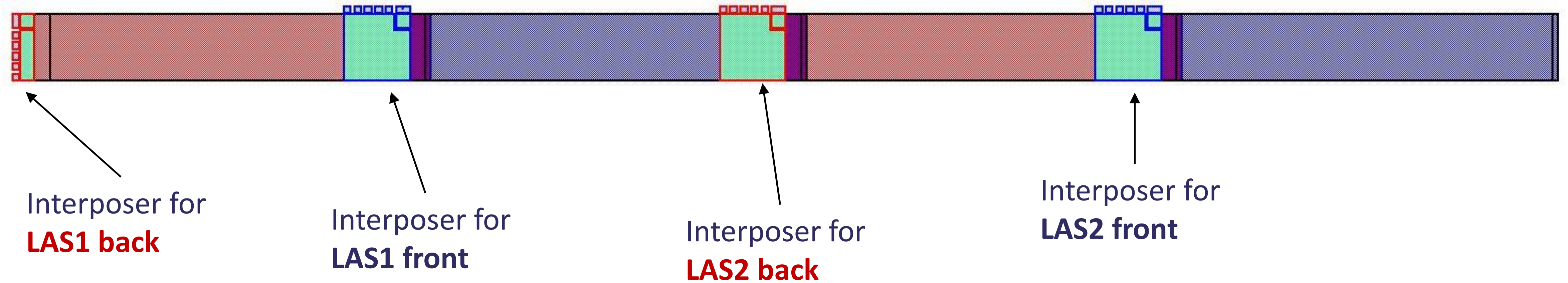
all LAS +
interposer FPC +
all auxiliary components +



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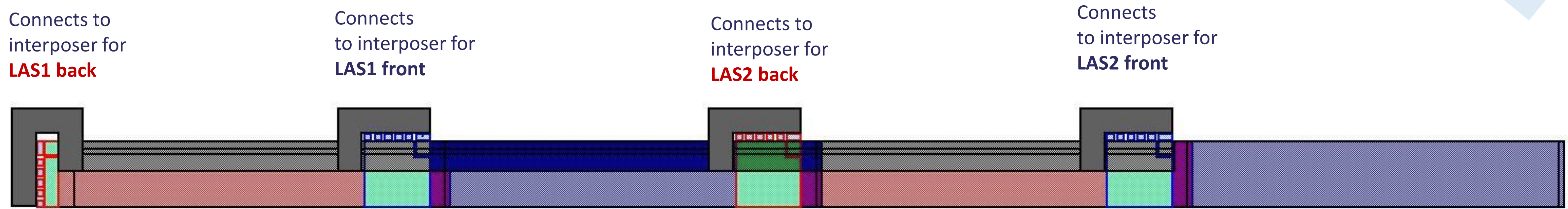
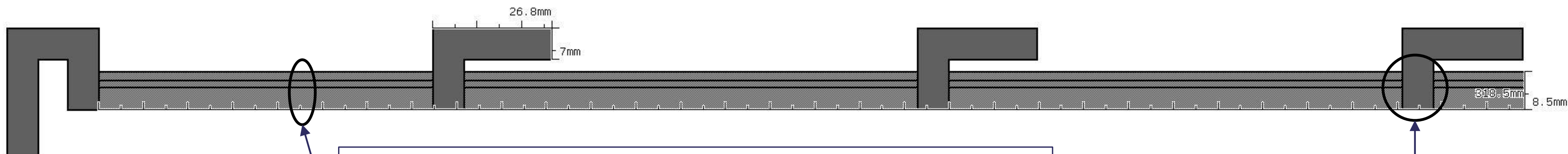
Common bus FPC

Note: no FPC bending in entire design

- The common bus FPC connects the auxiliary components to the end of stave connections.
- For the Outer barrels, it runs on top of the sensors (shown here);



Showing only common bus FPC:



Axial part of the bus:

- length 325mm
- width 8.5mm: **(<0.5 LAS width (19mm))**
  - (7 diff lines) x (500um/diff lines) = 3.5mm
  - 5.0mm for i_sLDO track

Bridges:

- on top of the axial part of bus,
- above material budget

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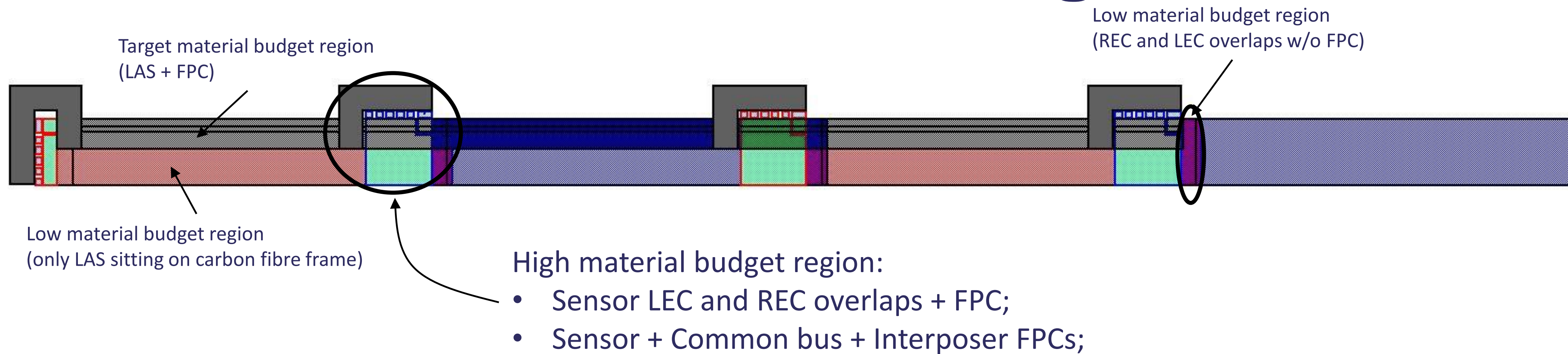
Common bus FPC: i_sLDO track

Assumptions for the selection of the i_sLDO track width:

- 5mm track width leading to ~3% voltage drop over over a lenght of 150mm (i_sLDO = 2.5A)

Voltage drops for common bus FPC										
sLDO	V (target)	V (max)	I (A)	Al resistivity (ohm*m)	Al tickness (m)	Al length (m)	Width (m)	Al resistance (ohm)	Voltage drop (V)	% wrt V (target)
Opt.1	2.5	TBC	2.5	2.65E-08	2.50E-05	1.50E-01	1.00E-03	1.59E-01	3.98E-01	1.59E+01
Opt.2	2.5	TBC	2.5	2.65E-08	2.50E-05	1.50E-01	2.00E-03	7.95E-02	1.99E-01	7.95E+00
Opt.3	2.5	TBC	2.5	2.65E-08	2.50E-05	1.50E-01	3.00E-03	5.30E-02	1.33E-01	5.30E+00
Opt.4	2.5	TBC	2.5	2.65E-08	2.50E-05	1.50E-01	4.00E-03	3.98E-02	9.94E-02	3.98E+00
Opt.5	2.5	TBC	2.5	2.65E-08	2.50E-05	1.50E-01	5.00E-03	3.18E-02	7.95E-02	3.18E+00

Considerations on material budget



The majority of the area is equal to or lower than the target material budget.

Improvements are possible for the regions above the target material budget:
exploit synergy w mechanics layout, improved design maturity of auxiliary components, consider Si interposer etc…

	Components	Thickness (um)	Material	X0 (cm)	X0 (%)	Comment
HIC	FPC metal layers	50	Al	8.897	0.056	25um/layer x 2 layers = 50um
	FPC insulating layers 1	75	UPILEX-S75	28.57	0.026	UPILEX-S75 is a type of polyimide
	FPC insulating layers 2	40	Coverlay	28.57	0.014	20um/layer x 2 layers = 40um, coverlay is polyimide
	Pixel Chip	50	Si	9.37	0.053	
	Glue	50	Araldite2011	39.07	0.0128	ATLAS assumes phenol epoxy C6 H6 O
Total (FPC + Pixel chip + glue)					0.163	
Total w/o glue (FPC + Pixel chip)					0.150	
Total FPC only					0.096	consider Si interposer as option: Si 50um thin equates to X0 (%) 0.053. N.B. ~45% saving in material budget

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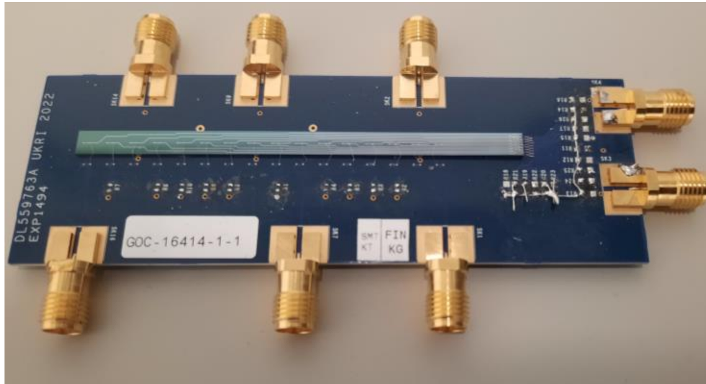
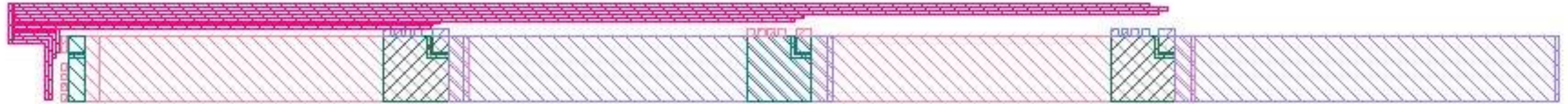
Si interposer (1 layer): examples

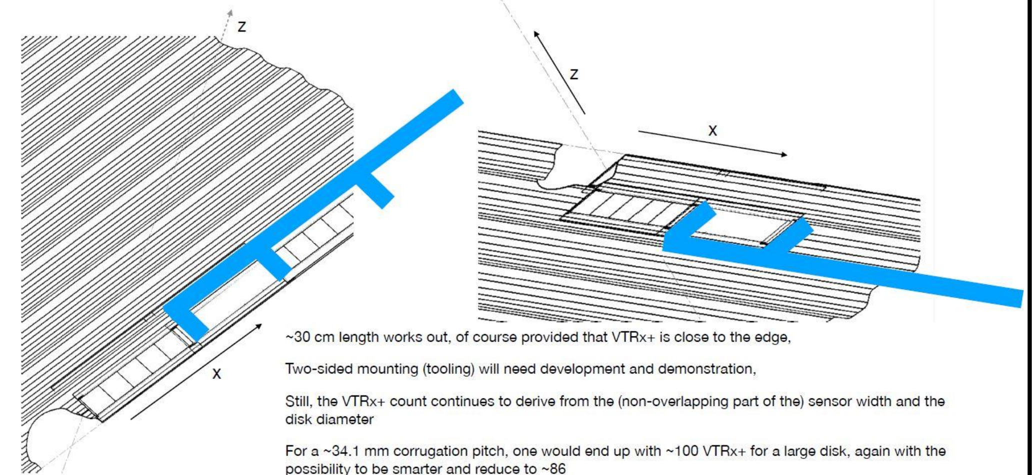


Common bus FPC (disk)

- For the disk, it runs aside the sensors (shown here);
- Dog leg approach, not considers here (yet…).



- In dog leg approach, the common bus FPC is spitted into shorted segments;
- Each shorter segment is merged with the interposer FPC;
- This approach could lead to better modularity.



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Technology

Technology

- Limited supplier choice for Al based FPCs:
  - CERN;
  - LTU (UKR);

- LTU:
  - Talk by LTU to ePIC SVT community on 03 Oct 2023;
  - Established track record in Al FPCs for Si trackers;
  - [TBC]no vias, tab bonding instead to connect tracks across layers;
  - LTU is keen to get involved;
  - Ad-hoc meeting with LTU & Daresbury Lab on 26/01/2024;

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Materials for ultra-low mass flexible interconnection elements

6

Aluminium-polyimide adhesiveless foiled dielectrics

Materials developed by LTU

Material	Layer	Thickness
FDI-A-50	polyimide	– 20 um
	aluminium foil	– 30 um
FDI-A-24	polyimide	– 10 um
	aluminium foil	– 14um
FDI-A-20 (under development)	polyimide	– 10 um
	aluminium foil	– 10um
LTU-2-100	polyimide	– 20 um
	aluminium foil	– 100 um
LTU-2-50	polyimide	– 20 um
	aluminium foil	– 50 um
LTU-3-50	polyimide	– 10 um
	aluminium foil	– 50 um
	polyimide	– 10 um

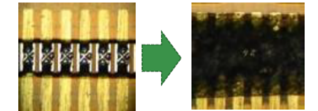
Note: all abovementioned Al-Pi adhesiveless materials now producing by RPE LTU

October 03, 2023 viatcheslav.borshchov@cern.ch, ihor.tymchuk@cern.ch

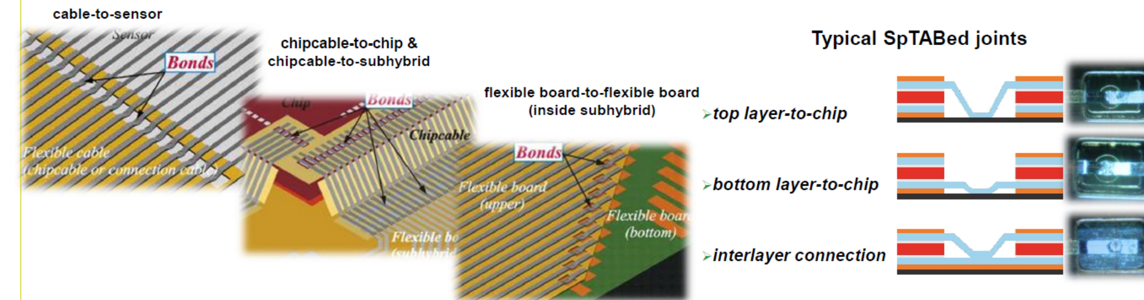
Some features of assembly process

7

Main process at assembling components of modules is an ultrasonic Single point TAB bonding (SpTAB, manual or automatic) of aluminium traces to aluminium contact pads on chip, sensor or flexible cable with further encapsulating by glue



Schematic close-up views of some different SpTAB areas



Note: SpTAB technique allows to have two times less bonds (comparing to wire bonding) - higher reliability

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Outlook

- Prototype of common bus:

  - Design first prototype similar to what presented today
    - Material of FPC <0.096 % X/X0
    - Mtg w LTU on 26/01/2024, to use LTU for prototype.

  - Finalise test plan:
    - High speed data: signal propagation (inc. signal attenuation over XX lenght);
    - CLK propagation (inc. jitter);
    - Some kind of comparison w and w/o electrical bridges;
    - Some kind of comparison w and w/o bending;
    - Max voltage and current Vs dielectric insulation limits;

  - Finalise test set-up:
    - FR4 interface board to connect to KCU105?
    - Select suitable oscilloscope.
    - Some scripting…

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Conclusion

- WP3 Electrical Interfaces is working towards the specification and design of the FPCs.
- FPC dependency on material budget and stave/disk mechanical layout requirements was presented.
- The benefits of multiplexing and serial powering were introduced.
- A prototype will be produced and tested to include results in the TDR.
- Most likely LTU will be the supplier for the first prototype for TDR.

Thank you

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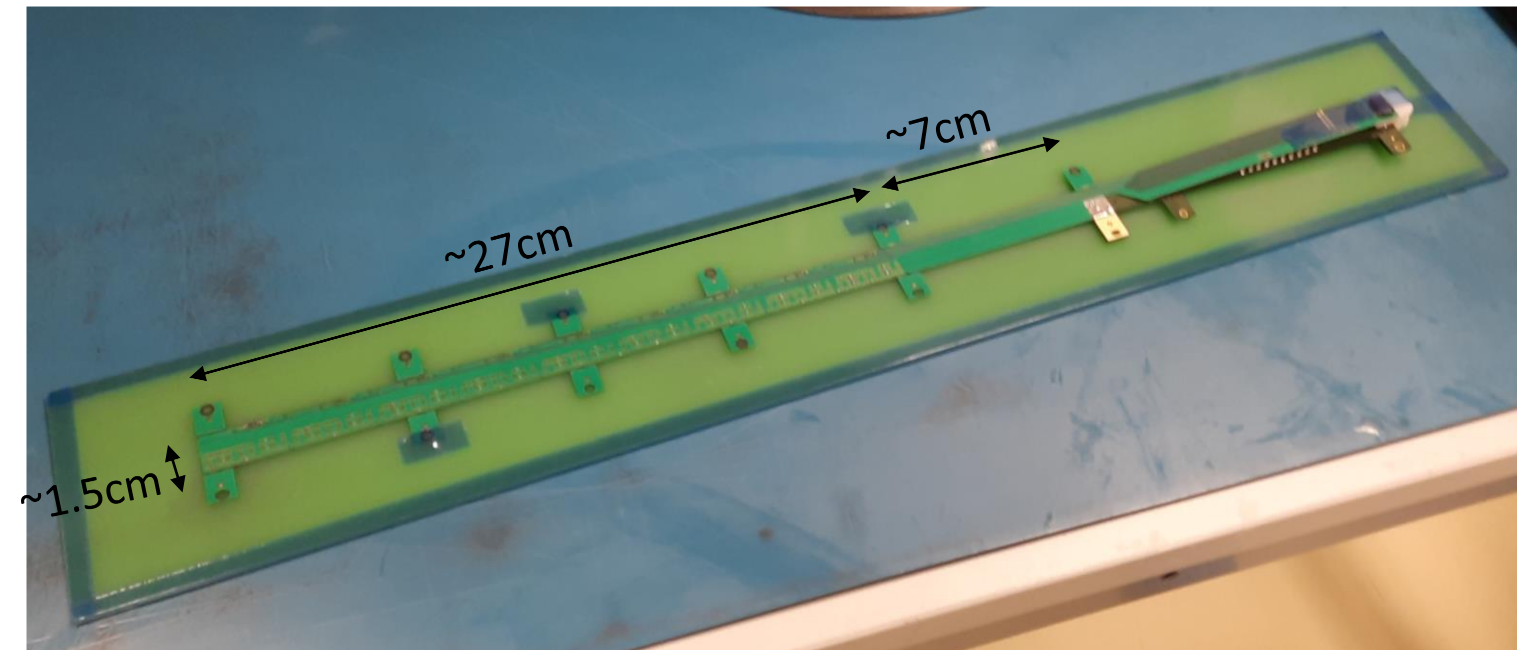
Back up

Points to discuss but not included

- Modularity of a potential sensor module:
  Modularity important for fault detection and early rejection. Beneficial for an efficient production flow.
  Modularity to be addressed as part of design for manufacturing.

- Is wire-bonding the preferred interconnection technique?
  i.e. Is the interconnection know-how mainly on wire bonding in our community?

Points to discuss but not included



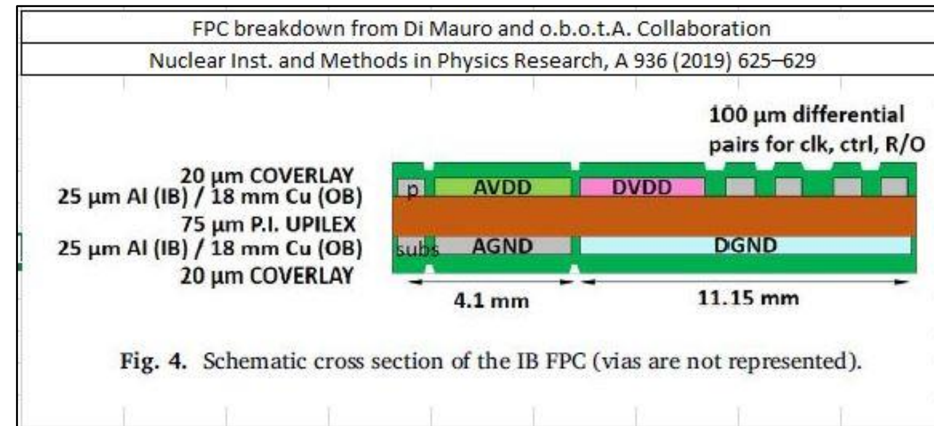
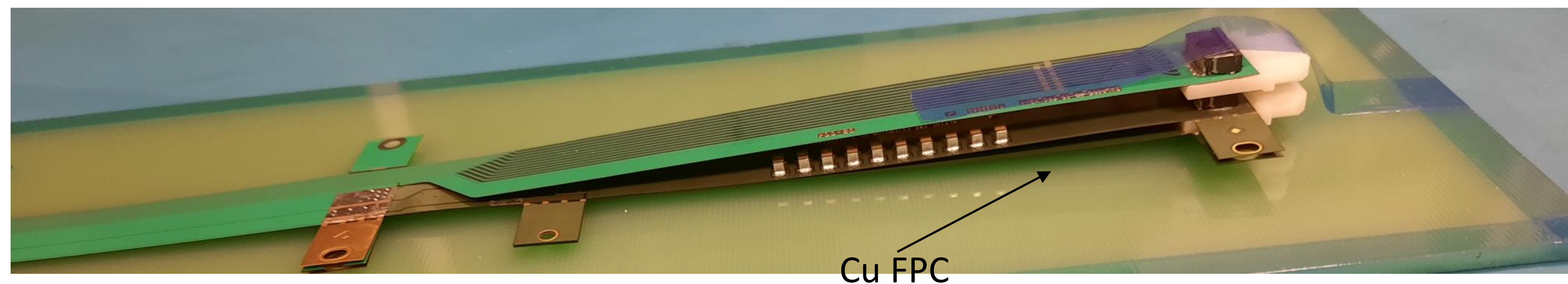


Fig. 4. Schematic cross section of the IB FPC (vias are not represented).



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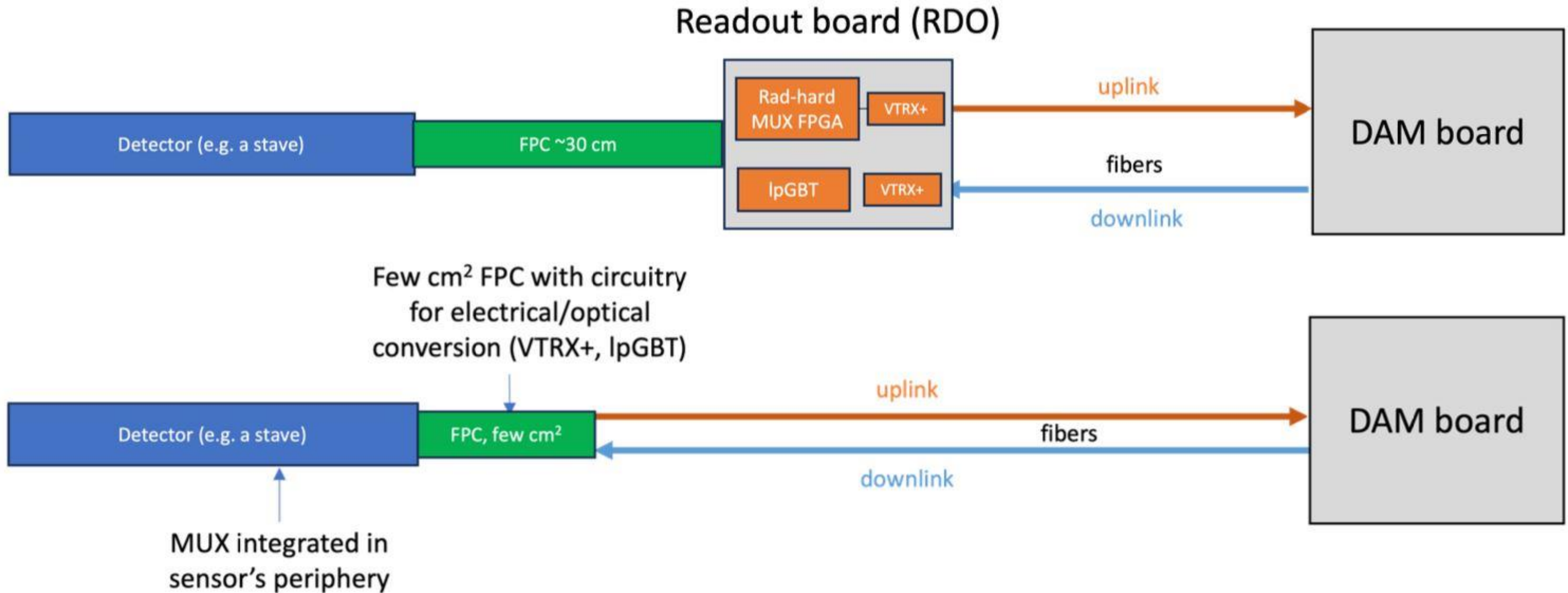
SVT Readout (inspired by ITS3 Readout)



Oak Ridge National Laboratory

J. Schambach