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U.S. DEPARTMENT OF ENERGY

AC-LGAD sensor production at BNL

Gabriele Giacomini

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@BrookhavenLab

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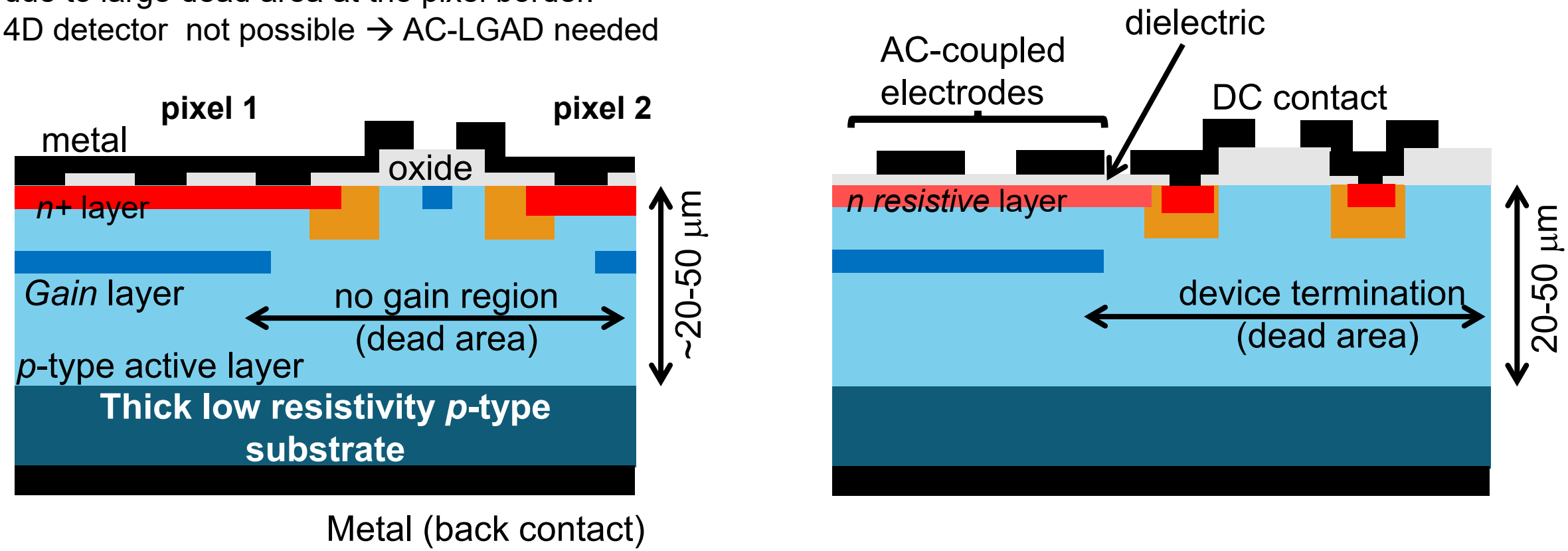
DC-LGAD vs AC-LGAD

Low-Gain Avalanche Diodes show good timing resolution (30ps) but poor spatial resolution, due to large dead area at the pixel border.
4D detector not possible → AC-LGAD needed



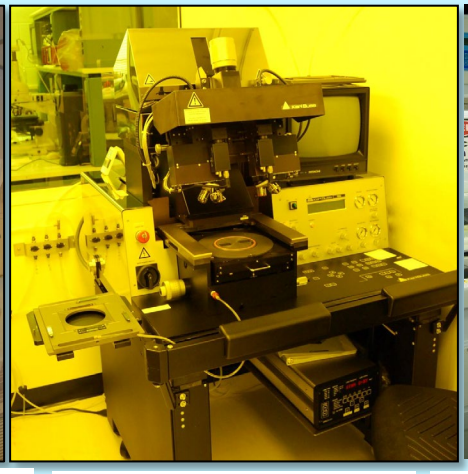
Capacitively-Coupled Low-Gain Avalanche Diodes have large uniform area for 100% fill factor (no dead areas), and same timing resolution. Excellent spatial resolution when signal sharing is used to interpolate hit position.
Process modification needed to pass from LGAD to AC-LGAD but still feasible in standard Clean Room.

BNL Clean Room for silicon sensors

LGAD and AC-LGAD can be fabricated at BNL, using standard tools.
Ion Implantation is outsourced: paramount importance process step that dictates gain.

All silicon process done in BNL Instrumentation Division Class-100 Clean Room

Furnaces for high-quality SiO_2 growth and annealing



Double-sided mask aligner

Wet bench (HF, RCA I & II, piranha, …)

Sputtering (Al, Al1%Si, Ti)

RTA for sintering

Laser dicing

Design + TCAD + process flow: all in house

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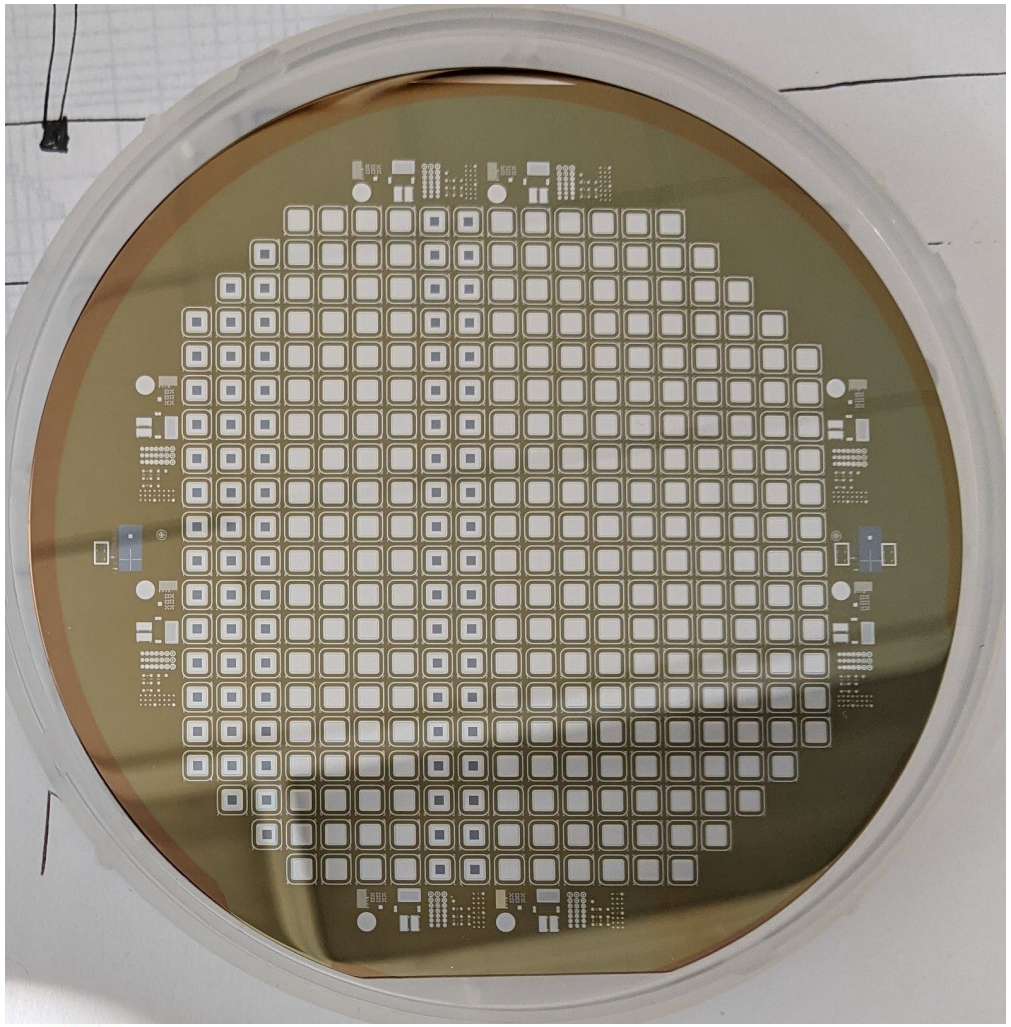
DC-LGAD

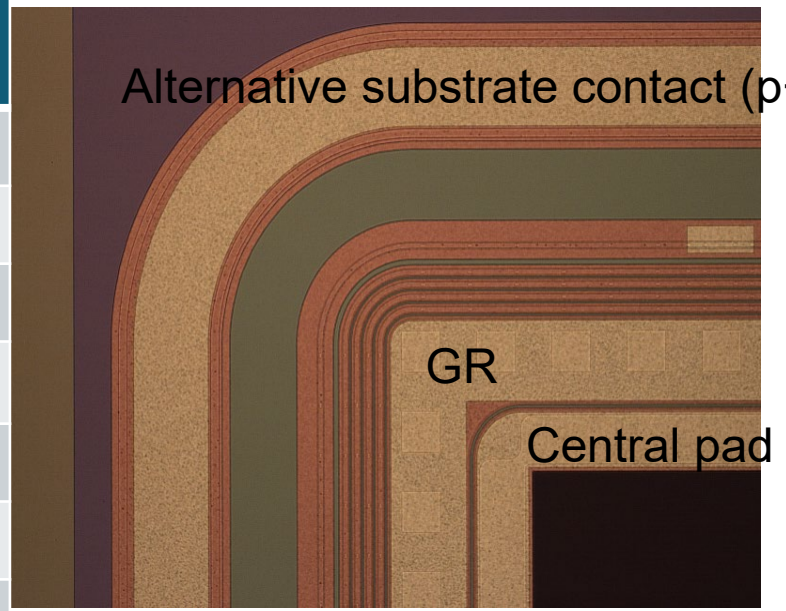
In parallel to AC-LGAD, DC-LGAD wafer fabrication for test purpose.
- existing photomask set.



Test on small devices:

- Single channel LGADs (1.3 mm x1.3mm) – and diodes
- 20, 30, 50um thick wafers

Wafer #	Thick (um)		VBD (V)
3055	50	1MeV	280
3106	30	1MeV	250
3078	20	1MeV	140
3058*	50	380keV	200
3057	50	380keV	170
3109*	30	380keV	130
3108	30	380keV	110
3082*	20	380keV	80
3079	20	380keV	90



*small furnace

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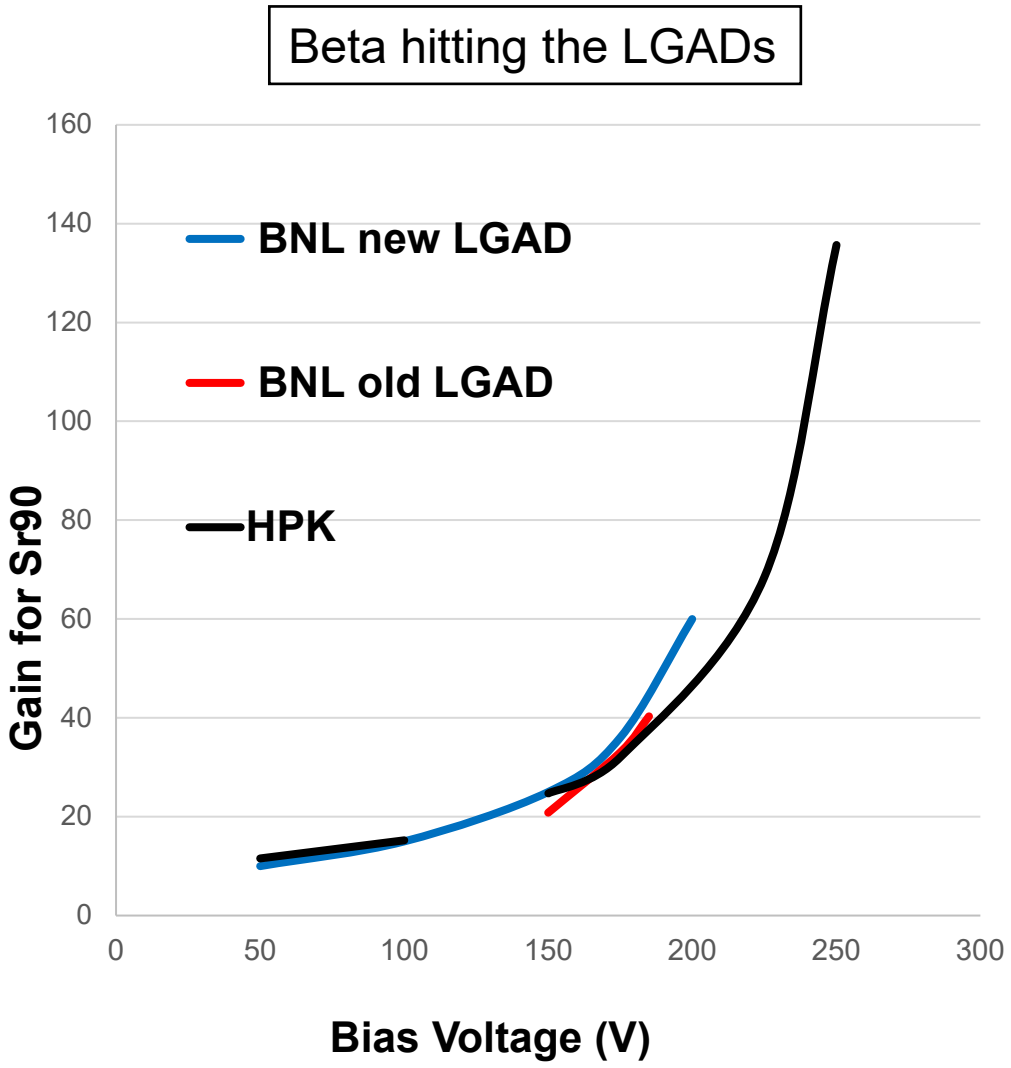
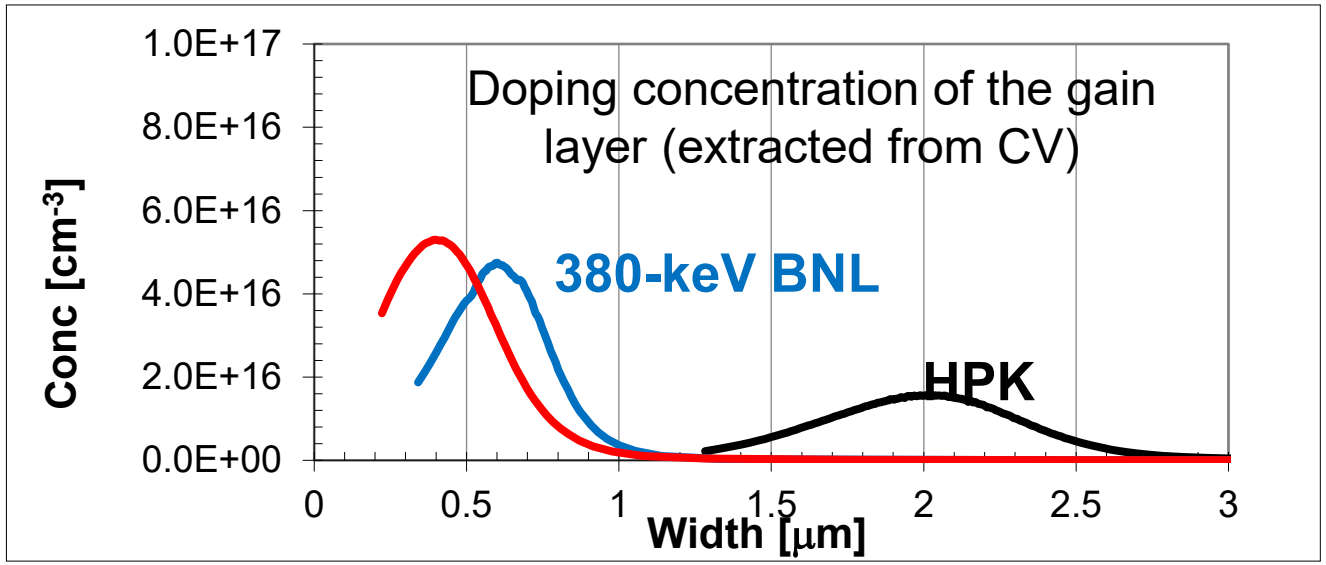
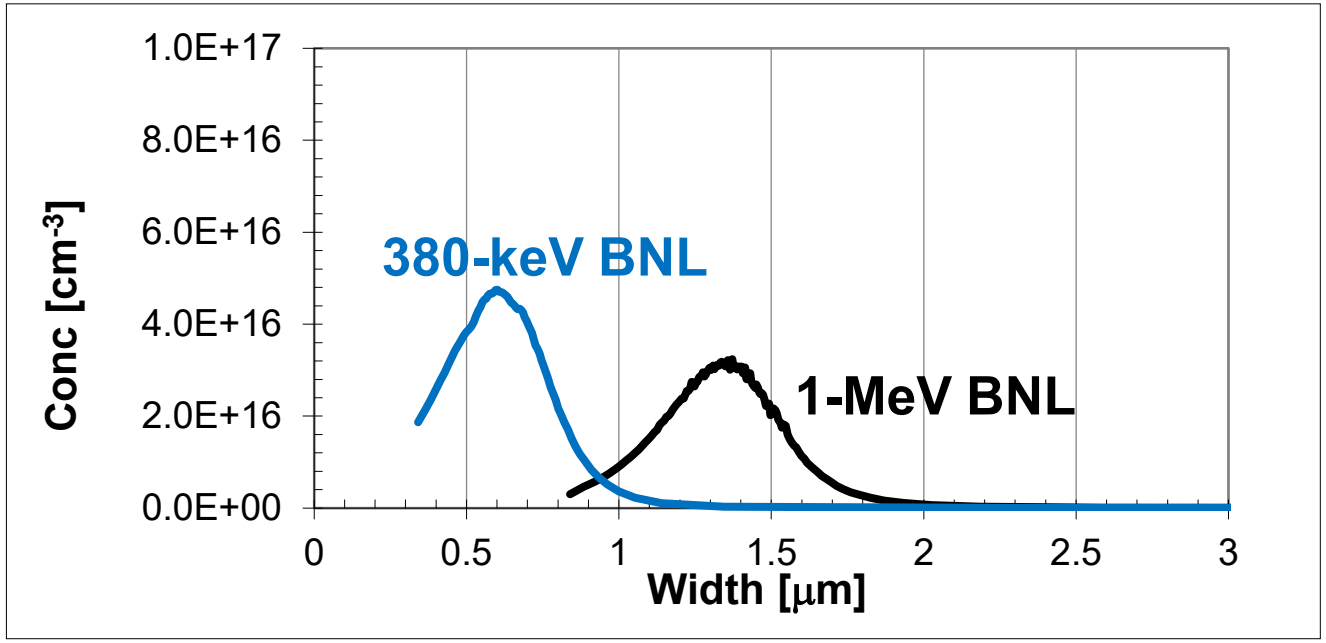
Gain measurements

Low-noise charge measurements with charge sensitive preamplifier (shaping time ~ 1us)







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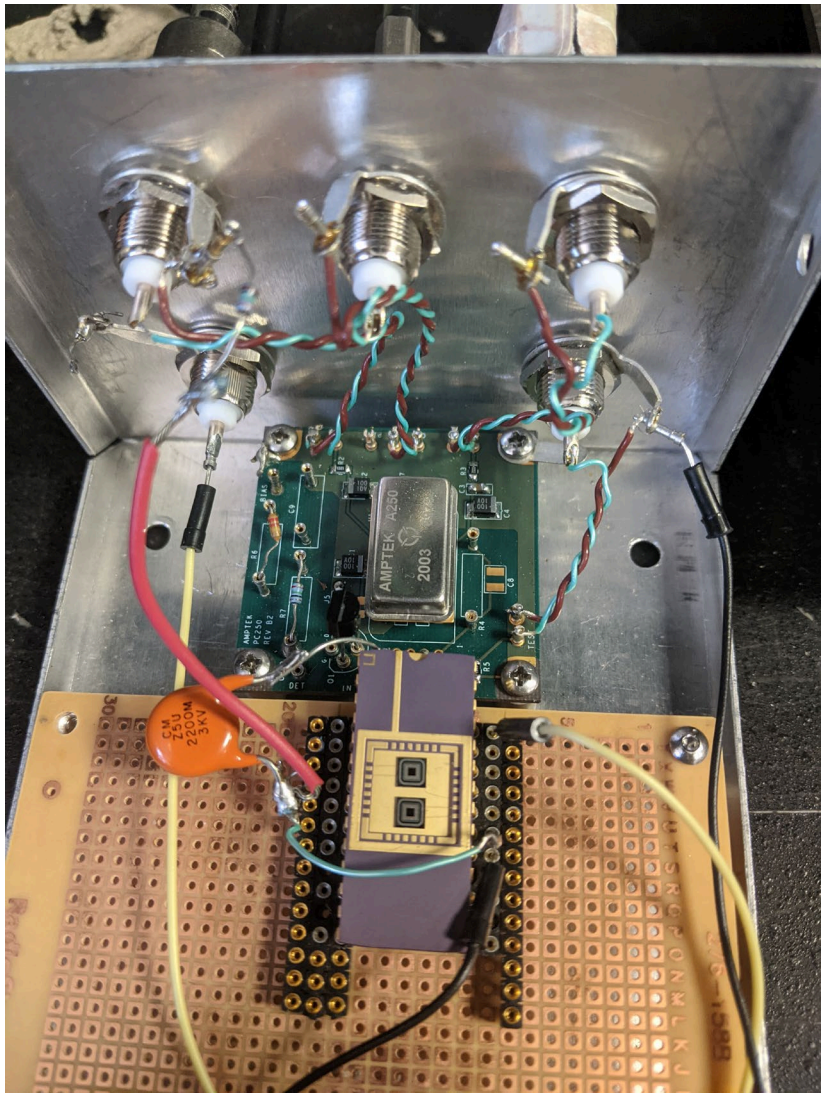
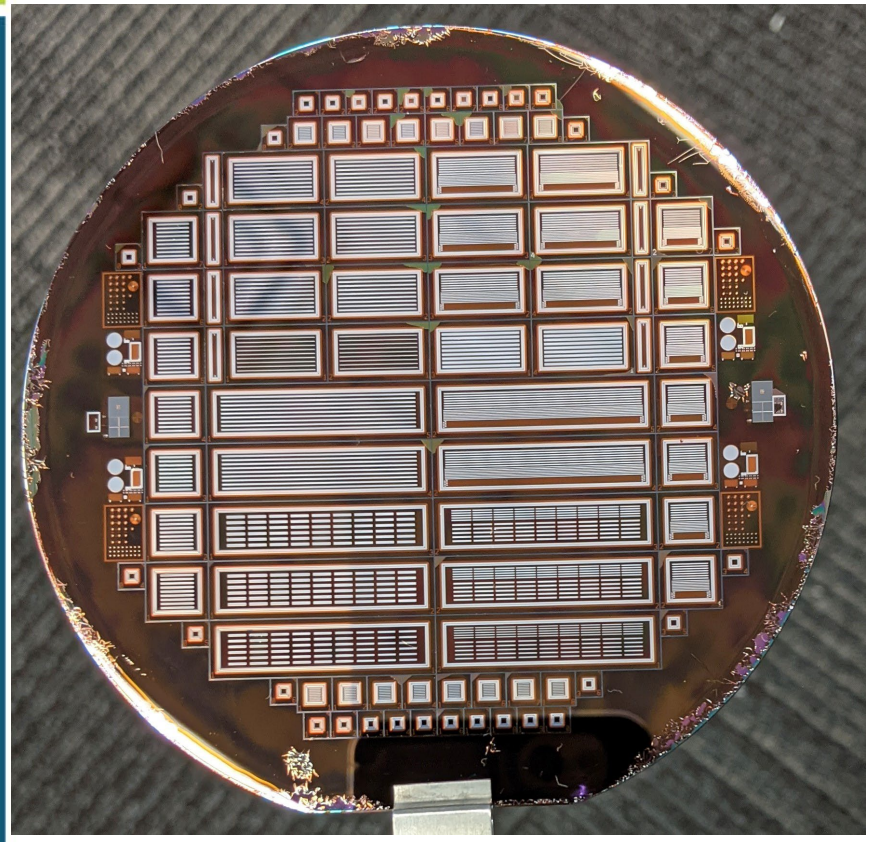
Gain measurements



- Low-noise by CSA read-out (external MCA)
- LGADs/diodes tested with 90Sr (and other particles)
  - From $V_{depletion}$ to V_{BD}
- Running 24/7 (due to low-activity of sources)
- 1MeV- LGADs are being mounted on ceramic carrier
- UCSC and FNAL board are used as well

AC LGAD strip



multiplicity	mm x mm	Pitch (um)	Gap (um)
7	5x5	500	400
7	5x5	500	450
4	5x10	500	400
4	5x10	500	450
4	5x10	700	600
4	5x10	Zig Zag	
5	5x25	500	400/450
5	5x25	500	400 (l=2 or 2.5cm)

Wafer #	Thick (um)		VBD (V)
3051	50	380keV	170
3052	50	380keV	180
3074	20	380keV	100
3075	20	380keV	90

Uniformity of gain was improved starting from this batch

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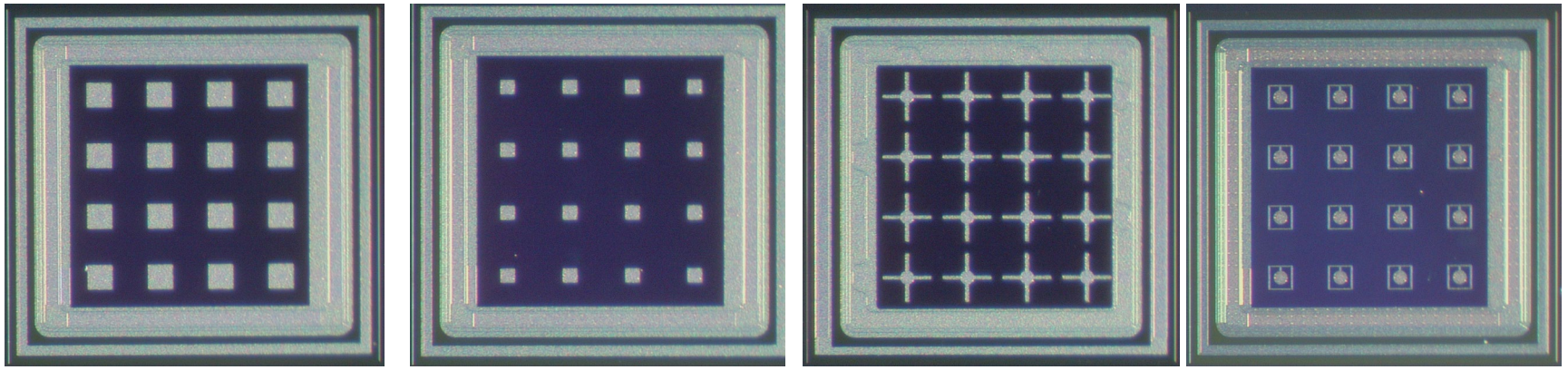
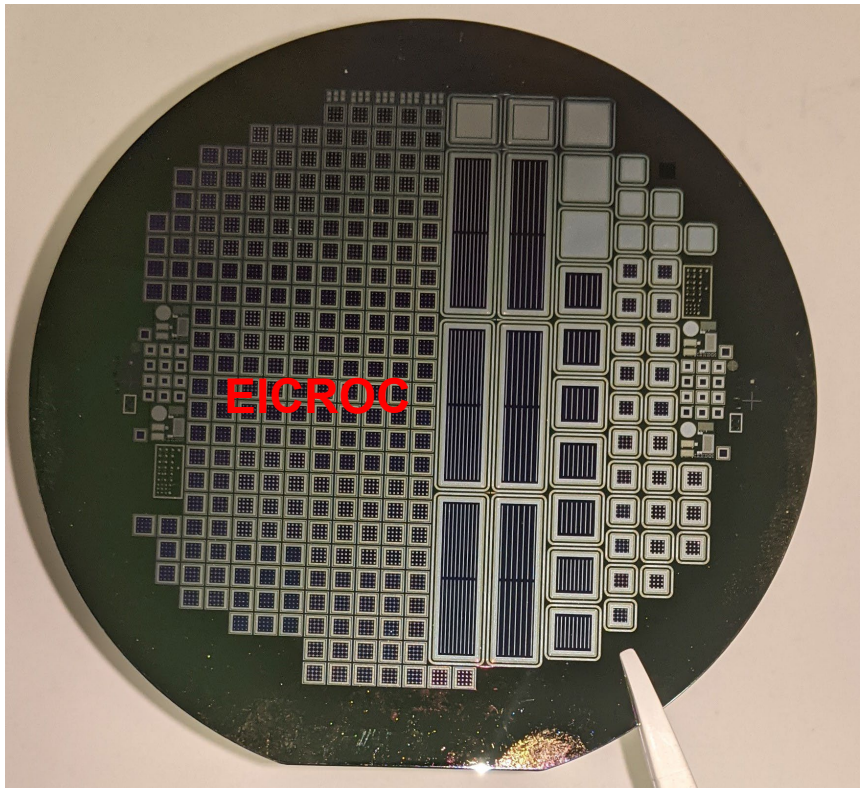
EICROC AC-LGAD





Wafer #	Thick (um)		VBD (V)
3053	50	380keV	160
3054*	50	380keV	380
3056	50	1 MeV	TBC
3080	20	380keV	80
3081*	20	380keV	160
3077	20	1MeV	160
3104	30	380keV	110
3105*	30	380keV	200
3107	30	1MeV	TBC

*long annealing

As for DC-LGAD, gain layer dose (which sets the VBD) comes by TCAD simulations (Y. Zao, UCSC): SIMS profiles of n+ + gain layer simulated implant.

New mask

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New Metal mask for EICROC AC-LGAD

Requires the redesign of just two masks: METAL and passivation opening.

- 4x4 array Pitch 500um : cross, circle, squares W=100, 200, 300, 400 um
- 3x3 array Pitch 700um: cross, circle, squares W= 100, 200, 300, 400 um
- 4x4 array Pitch 400um: cross, circle, triangular arrays
- … and larger devices

Some parameters:

C_{AC} ~ 300pF/mm^2
R_nres ~ 1.4kOhm cm

Outlook

- Fabrication of optimized AC-LGADs
  - Obliging inputs from collaborators
    - Higher gain
    - Higher yield
    - Double-metal
  - TCAD simulations (UCSC)

- Test (TCT/gain)
  - Preliminary I-V & C-V tests before device distribution

- Q&A – stress test
  - Cycling through large temperature range
    - Irradiation in collaboration with UNM and LANL

- Mounting PC boards for collaborators
  - Tests on site
    - EICROC tests