

Barrel Module Assembly Ideas

Matthew Gignac

January 10th 2024



SCIPP

SANTA CRUZ INSTITUTE
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- CD 2/3 review expected at the end of 2024, and we are expected to demonstrate ~70-90% of the design
- Over the next year, it's critical that we start assembly efforts with available components and strengthen institutional collaboration
- Leading up to this review, we propose to demonstrate the module design for thermal and AC-LGAD signal characterization, to confirm performance obtained with standalone mini-components

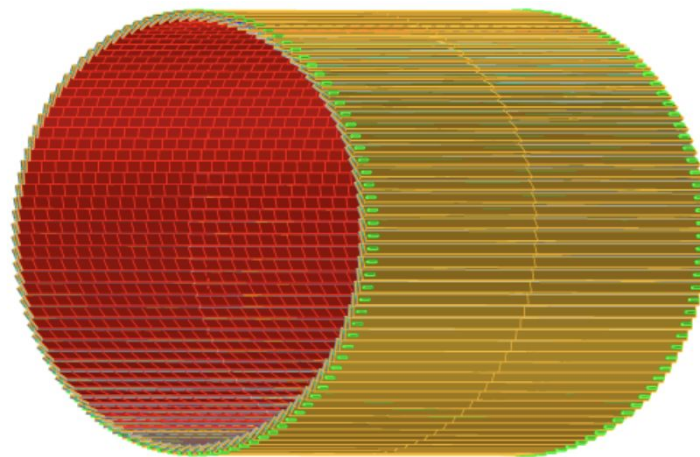
Schedule and Timeline

Charge #4



Barrel TOF detector

- BTOF is a main particle identification detector covering low pT at mid-rapidity
- Planning to use AC-LGAD strips sensors with 3.2 x 4cm (four 1 cm segment)
- Nominal plan is to use FCFD chip for readout of the sensors



	Area (m ²)	Channel size (mm ²)	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10	0.5*10	2.4M	35 ps	30 μm in $r \cdot \phi$	0.01 X ₀
Forward TOF	1.4	0.5*0.5	5.6M	25 ps	30 μm in x and y	0.05 X ₀
B0 tracker	0.07	0.5*0.5	0.28M	30 ps	20 μm in x and y	0.05 X ₀
RPs/OMD	0.14/0.08	0.5*0.5	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.
Lumi Tracker						

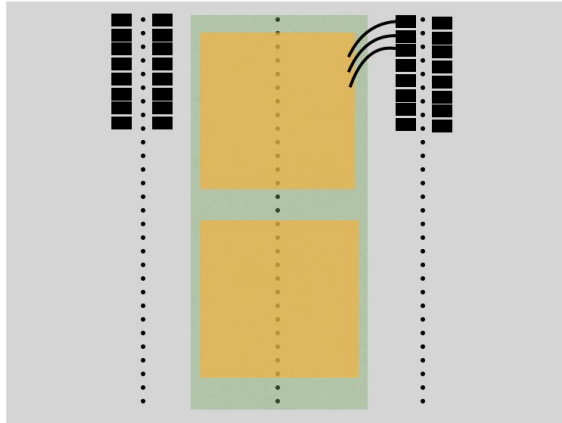
- Possible plan for the barrel module assembly program:
 - a. **Thermal mechanical modules [FY24]**
 - Aim to demonstrate the preliminary design in preparation for CD 2/3
 - Focus is on the mechanical assembly & thermal performance, while waiting for ASIC design a mature. “By hand” assembly

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 - b. **Semi-electrical modules: preliminary design [FY25]**
 - FCFDv2 submission in 2024 Q4, feed into this program.
 - Expecting reduced channel count
 - Preliminary assembly tooling, informed from experience with the thermal assembly program, to be developed for this period
 - c. **Fully electrical modules: pre-production [FY26]**
 - Assume close to final version chip leading into this period

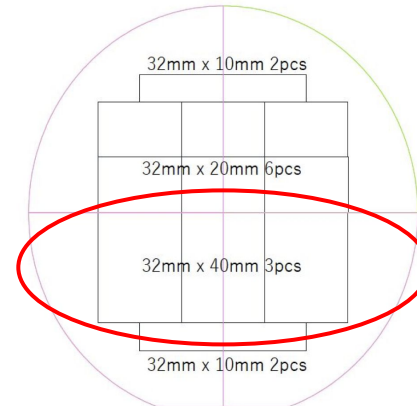
Possible barrel module stack-up

- **Full-sized sensors** planned in an upcoming HPK production
 - Presumably sensors will be used for studies (laser TCT, beta-source, test beam) throughout first half of 2024. Afterwards could be used for assembly
- Placement of ASICs and interconnection **still an outstanding R&D issue**
 - In order to maintain timing resolution, don't see how this can be off sensor
 - For thermal mechanical program, suggest to place onto a **readout hybrid PCB**

Sensor
Chip
Readout
hybrid
Wirebonds

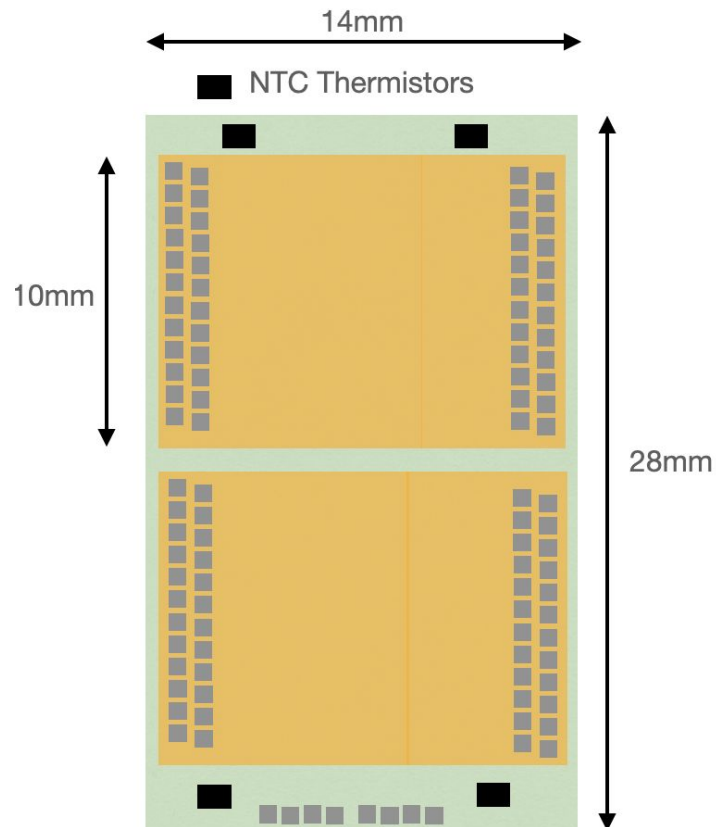


Wafer layout plan



Thermal readout hybrid

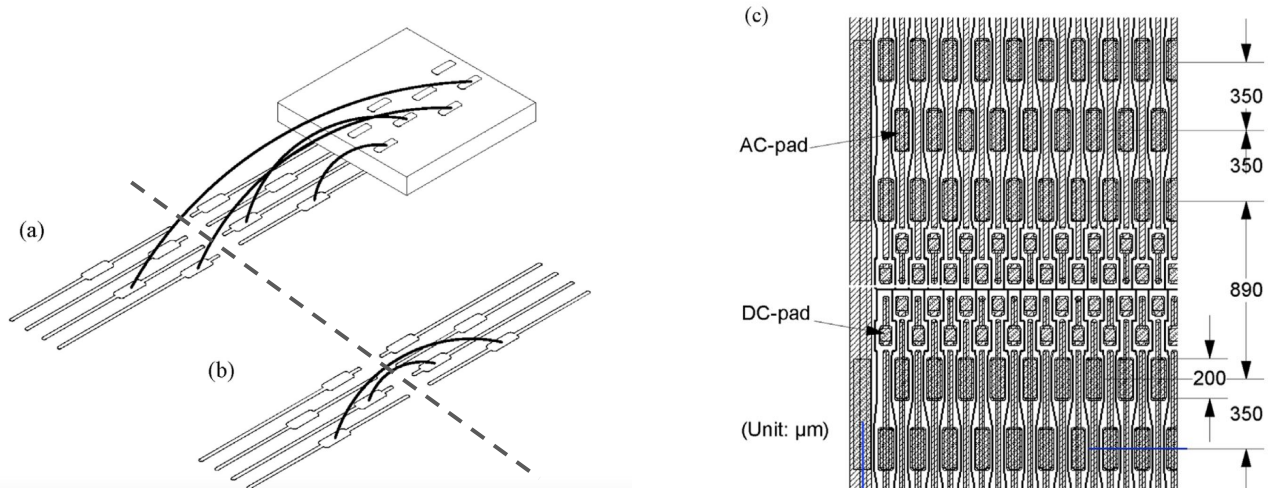
- Simple PCB based readout hybrid would serve as a thermal load, preferably with a design that matures towards intended electrical design
- A resistive trace on the readout hybrid below ASICs to simulate thermal load:
 - Target nominal power of 1 mW/channel
 - Also produce a high power version? Do we have a realistic estimate for power consumption for FCFD chip?
- Dimensions of readout hybrid constrained to allow it to fit onto 2 sensor segments to allow wirebonding between ASIC and sensor
- Two (non-electrical) glass-patterned dummy “ASICs” per readout hybrid to demonstrate sensor-to-ASIC interconnection



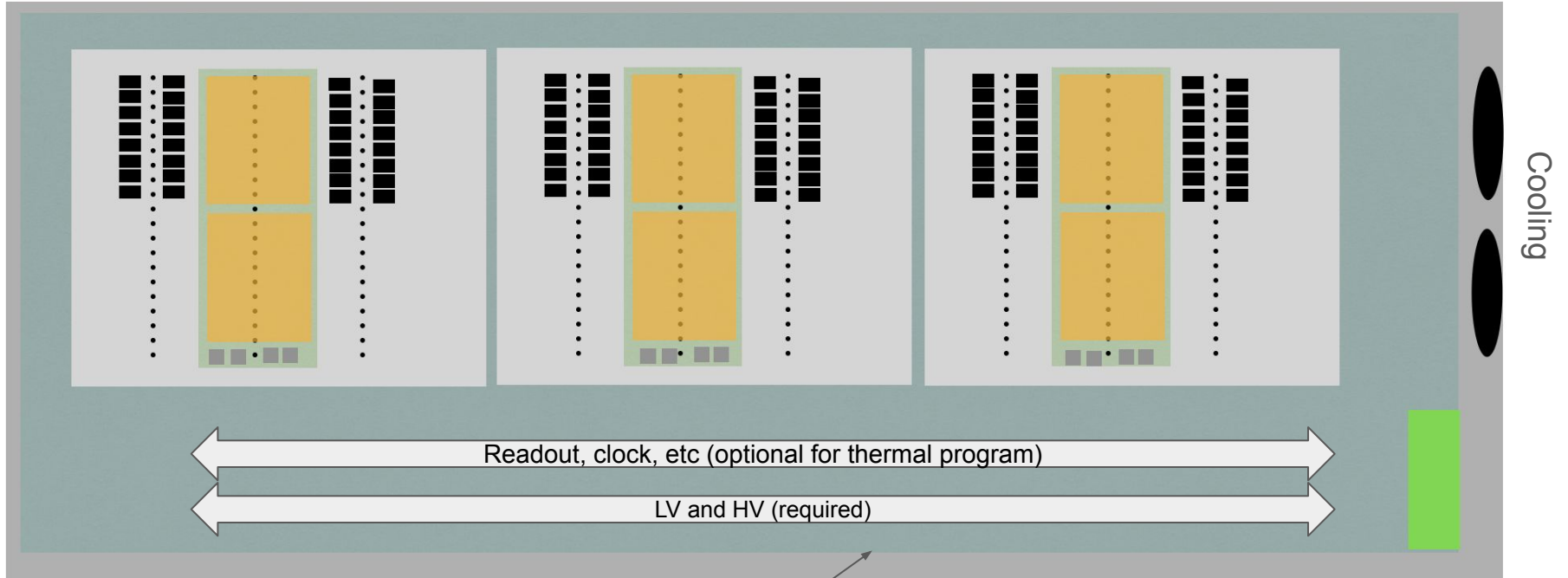
- In contact with **CNM** (Spain) about production of **glass patterning ASICs**
- They typically run fabrications in batches of 10 wafers of 100mm diameter
 - Current design assumes 2 ASICs per sensor, measuring 10 x 10mm²
 - **Do we have a better estimate for FCFD footprint?**
 - Approximate dies per wafer ~ 20 → 200 thermal ASICs minimum order
- Full process would take roughly between 5-8 weeks from the time the design is finished and approved until we have diced components in hand
- We could plan for a joint production with fTOF, however footprint and interconnect are likely different for bTOF. Main purpose of ASICs for bTOF is to demonstrate wire bonding connections between ASIC and sensor, however the fTOF will use a bump-bonding process (or similar, but not wire bonding)

Strip to ASIC interconnection

- Wire bonding planned to connect sensor and ASICs → relatively simple and well-controlled process with lots of experience from previous projects
- In this design, important to have bond pads on both ends of the strips, with wirebond-able sized pads (at least $\sim 50 \times 200 \mu\text{m}$)



Thermal module: rough sketch



- Besides demonstrating the assembly procedure, many studies important studies could be performed with these thermal prototypes:
 - **Thermal characterization** under two possible scenarios for ASIC power consumption
 - Target 1 mW/channel and worst case scenario ?
 - **Sensor characterization** when powered via hybrid flex
 - Current stability at operating bias voltage
 - Signal characteristics (amplitude, rise time, fall time) vs operating temperature
 - **Comparison of signal properties** for sensor segments with and without glue coverage
 - **Other ideas ... ?**
- Would also intend to perform characterizations (electrical, metrology, etc) throughout the assembly procedure, and use this information to define QC/QA procedures, required tooling, etc in preparation for the TDR

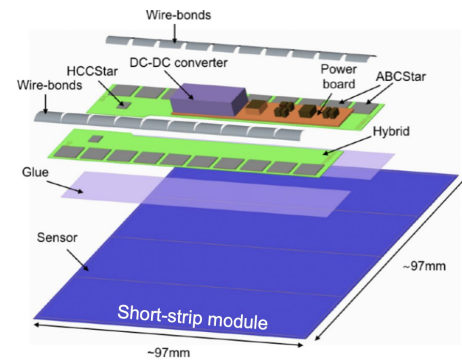
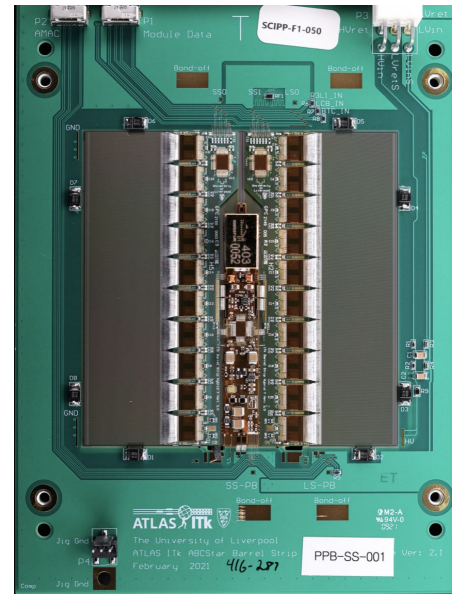
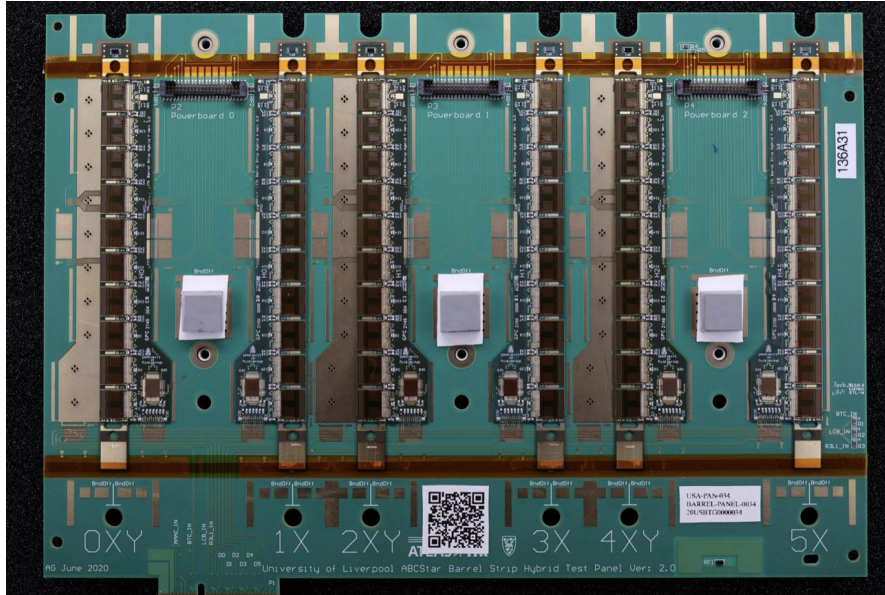
- Several sub-components still under R&D – would require close collaboration to achieve these (small) prototypes
- Without an electrical ASIC, we can focus on the mechanical (plus HV/LV) design and this would simplify design of the flex:
 - **Hybrid flex** (ORNL)
 - Can a “mechanical design” be produced in parallel to electrical design efforts?
 - Plans & responsible for attaching flex to support structure?
 - **Module support structure** (Purdue,NCKU)
 - Can design be adapted to provide cooling below sensor stack-up?
- Other *thermal* components could be designed by UCSC
 - **Readout hybrid or interposer** (UIC, UCSC)
 - **Thermal ASICs** (UCSC)

- UC Santa Cruz would like to start a thermal mechanical assembly program, and preliminary design of (thermal) components to support this program
- We are expecting to establish the assembly procedures, but the aim is for at more institutes to join these efforts towards the electrical program
- Beneficial (or necessary?) that institutes have existing infrastructure?
- Many institutes involved in ATLAS/CMS upgrades, and involvement in full-scale production would require those projects to ramp-down / conclude

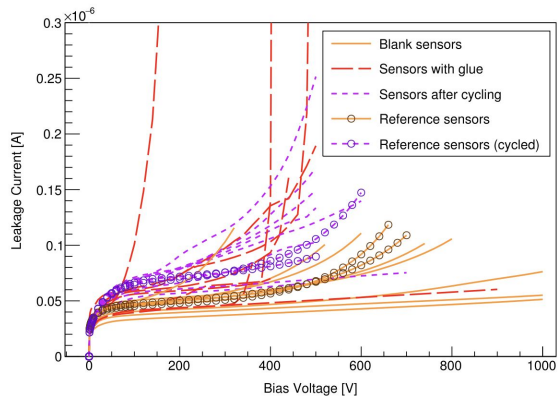
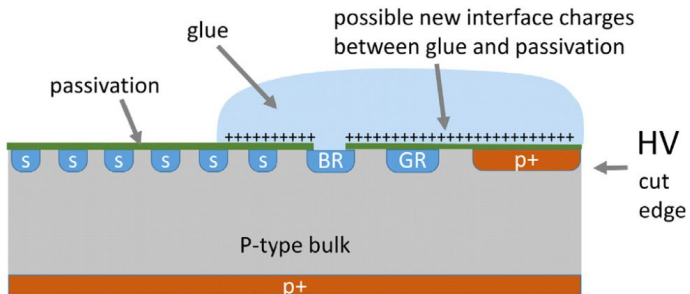


ATLAS ITk experience

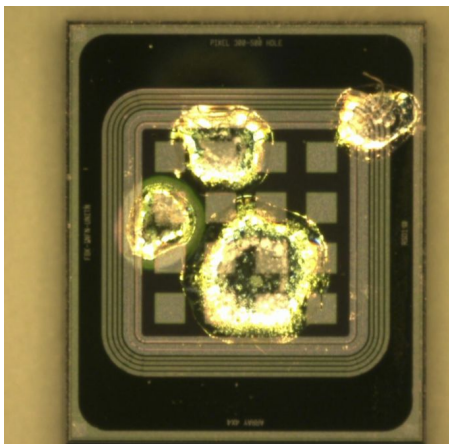
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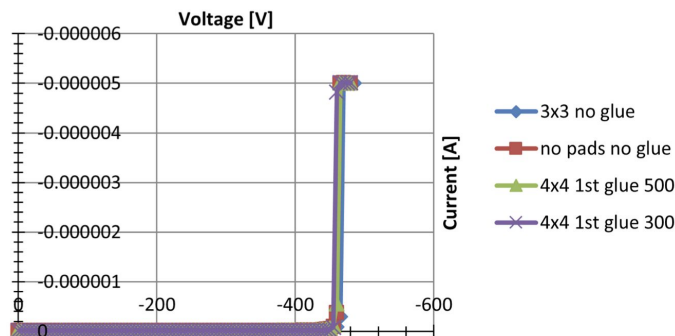
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- Throughout this program, we've encountered several challenges:
 - **Glue on guard ring, causing early sensor breakdown**
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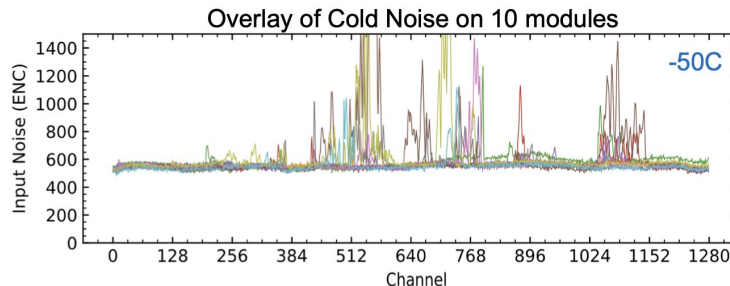


Current vs Voltage, Full Range



Started basic checks on FBK prototypes → **do not observe early breakdown**

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 - Many issues discovered relatively late due to time needed to commission these relatively complex test stations → **we should aim to test prototypes at the boundaries as early as possible to catch these types of issues**

- In preparation for CD 2/3 review at the end of this year, it's important to start to develop assembly procedures to demonstrate the preliminary design
- This serves multiple purposes:
 - Strengthen institutional collaboration and establishes parts flow
 - Demonstrates the feasibility of an assembly procedure using existing infrastructure
 - Provides a prototype module for thermal analysis
 - Provides input to define required tooling to meet required throughput
- Design of module support structure & hybrid flex would need to be adapted to proposed design, but would be simplified without an electrical ASIC
- A successful thermal mechanical program would position assembly teams to move quickly once an ASIC arrives