ePIC Forward TOF overview

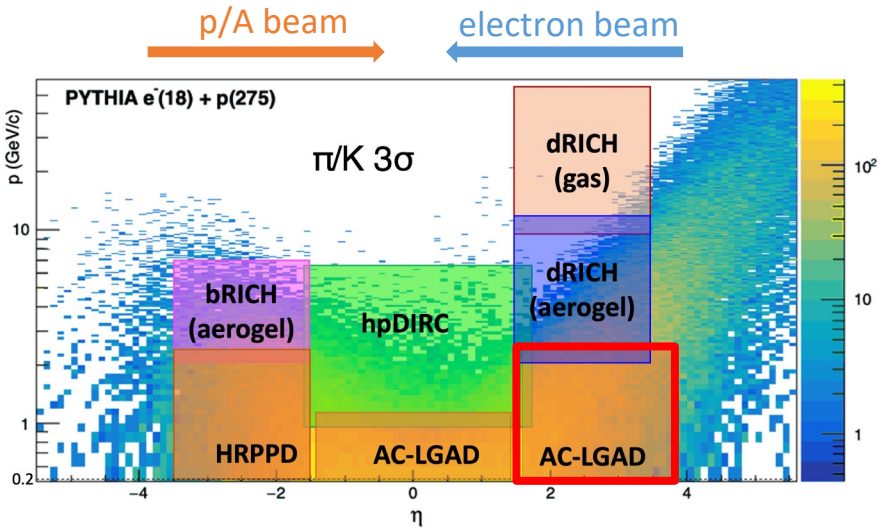
Wei Li (Rice University)

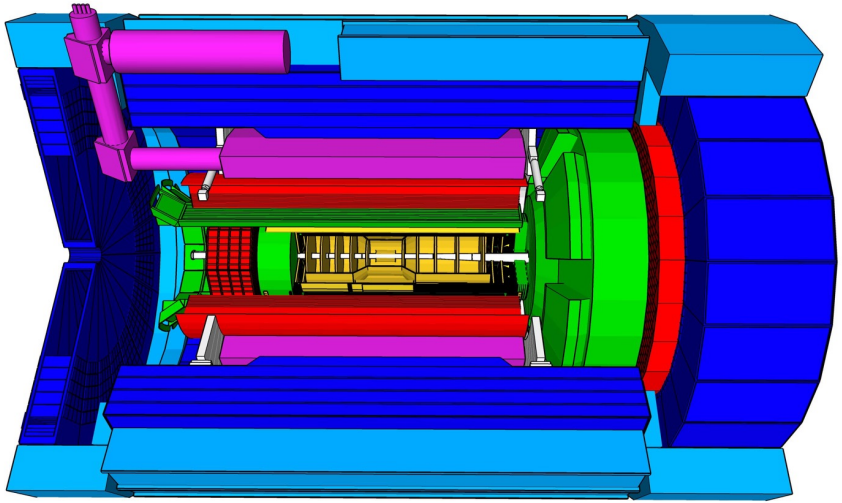
AC-LGADs Workfest@ePIC collaboration meeting
January 9-10, 2022

Electron-Ion Collider

BROOKHAVEN NATIONAL LABORATORY Jefferson Lab U.S. DEPARTMENT OF ENERGY | Office of Science

AC-LGADs TOF system for PID





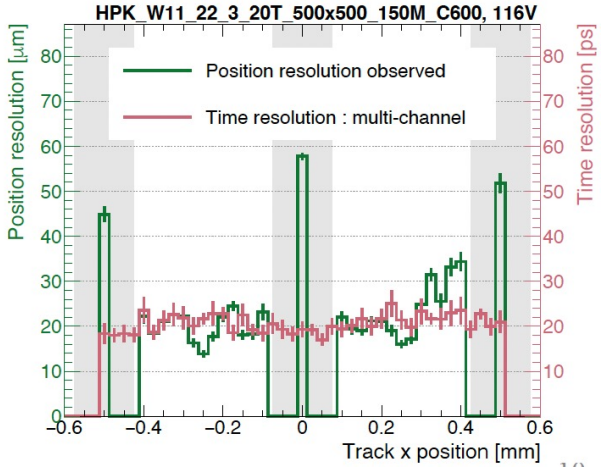
Latest envelope (Detector-20231031150001)

Detector	r (cm)	z (cm)	Rapidity coverage	Momentum range for 3σ π/K separation
Barrel TOF	56<r<63	-117.5<z<171.5	-1.42<η<1.77	0.2 < p_T < ~1.2 GeV
Forward TOF	8<r<60	180<z<195	1.86<η<3.85	0.2 < p < ~2.3 GeV

FTOF requirements and R&D progress

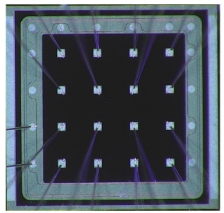
Current requirements (presented at FY23 EIC Project R&D - DAC Meeting)

	Area (m^2)	Channel size (mm^2)	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10	0.5*10	2.4M	30 → 35 ps	30 μm in $r \cdot \varphi$	0.01 X_0
Forward TOF	1.4	0.5*0.5	5.6M	25 ps	30 μm in x and y	0.08 → 0.025 X_0
B0 tracker	0.07	0.5*0.5	0.28M	30 ps	20 μm in x and y	0.01 → 0.05 X_0
RPs/OMD	0.14/0.08	0.5*0.5	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.



Max BV limited at ~11V/micron due to SEB

HPK Pixel Sensor (2x2 mm^2)



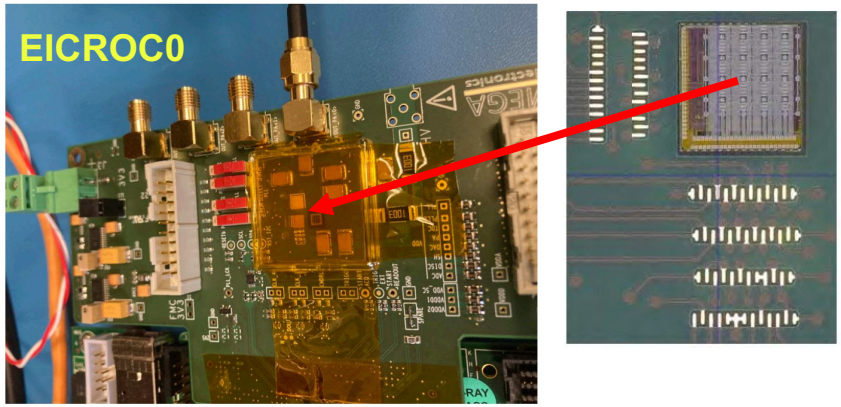
Promising to achieve the requirements with 20-micron thick, 0.5x0.5mm^2 pixel sensors

Next step: producing large sensors – **32x32**, **64x32**

FTOF ASICs - EICROC

ASIC requirements:

- Pixel size: 0.5x0.5 mm^2
- Low jitter: <20ps
- Low power consumption: 1mV/channel



EICROC0 (4x4): first version

↓

EICROC1 (8x32?): intermediate size

↓

EICROC2 (32x32): full size

↓

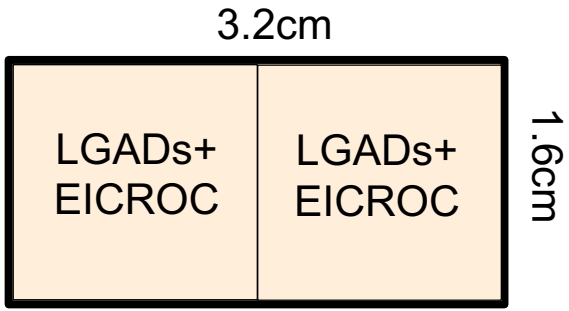
EICROC3 (32x32): final (if needed)

See details at Christophe's talk

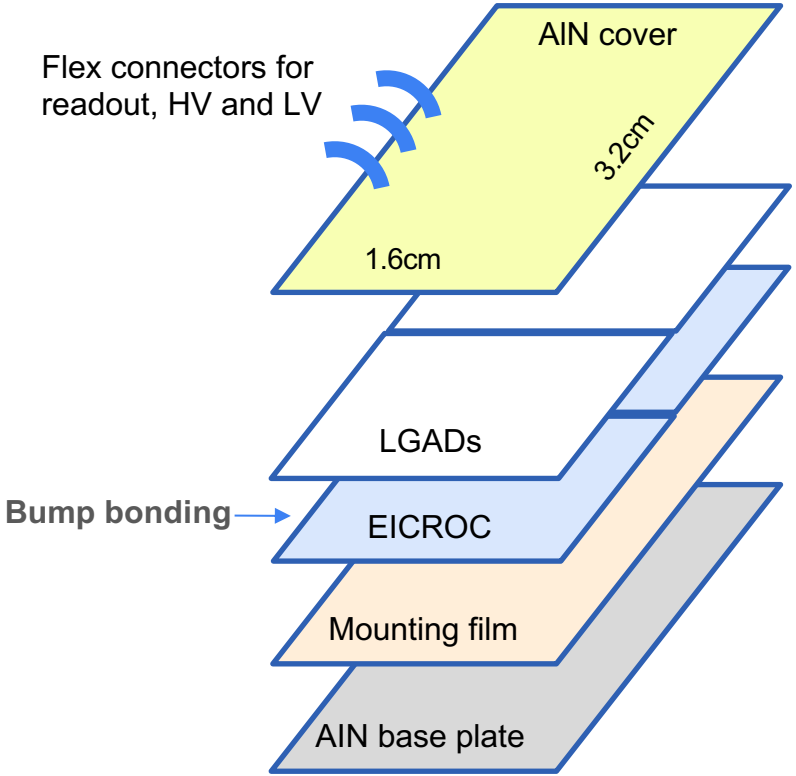
FTOF modules

Each FTOF module consists of

- Two 32x32 or one 64x32 sensors
- Two 32x32 ASIC chips (EICROC)

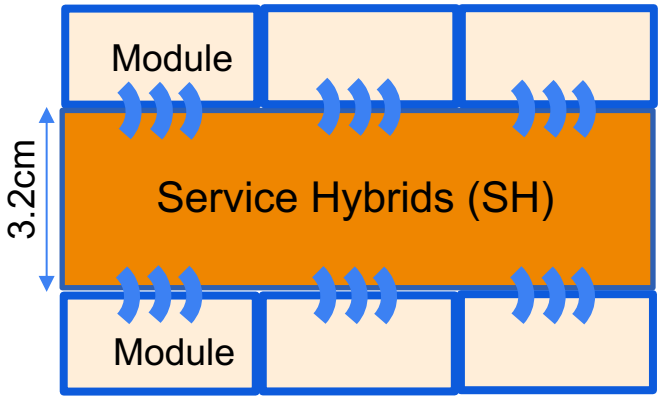


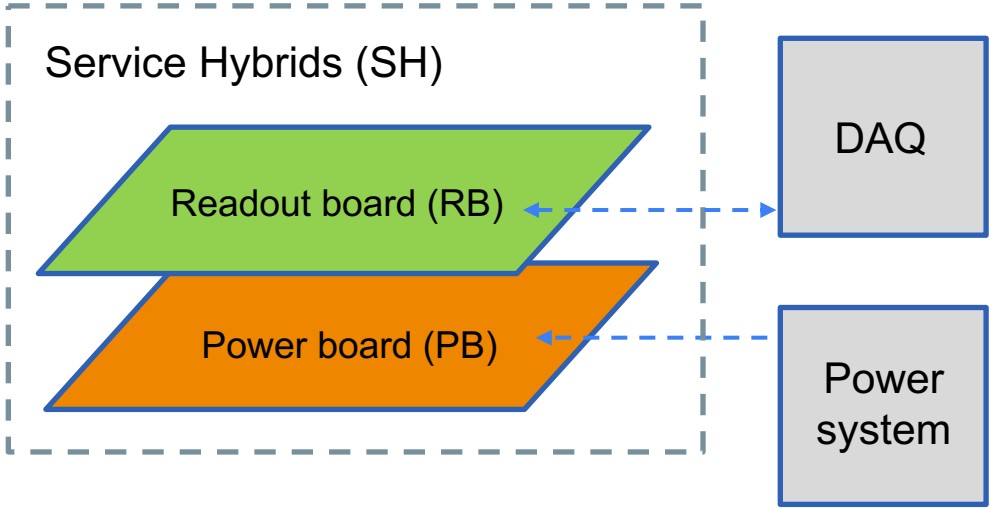
Expanded view of module illustration



FTOF service hybrids

- A readout board (data transmission) and a power board (LV/HV)
- Two types of SHs, serving 6 (12) or 8 (16) modules (EICROCs)
  - Not too many limited by pin connectivity, data rate to FPGA
  - Not too few so that the board is not too short (>~10cm)
  - Each SH serves even # of modules



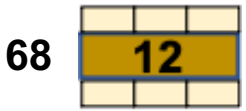


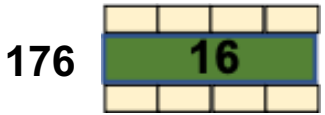
More details of design and prototyping in Wei's talk

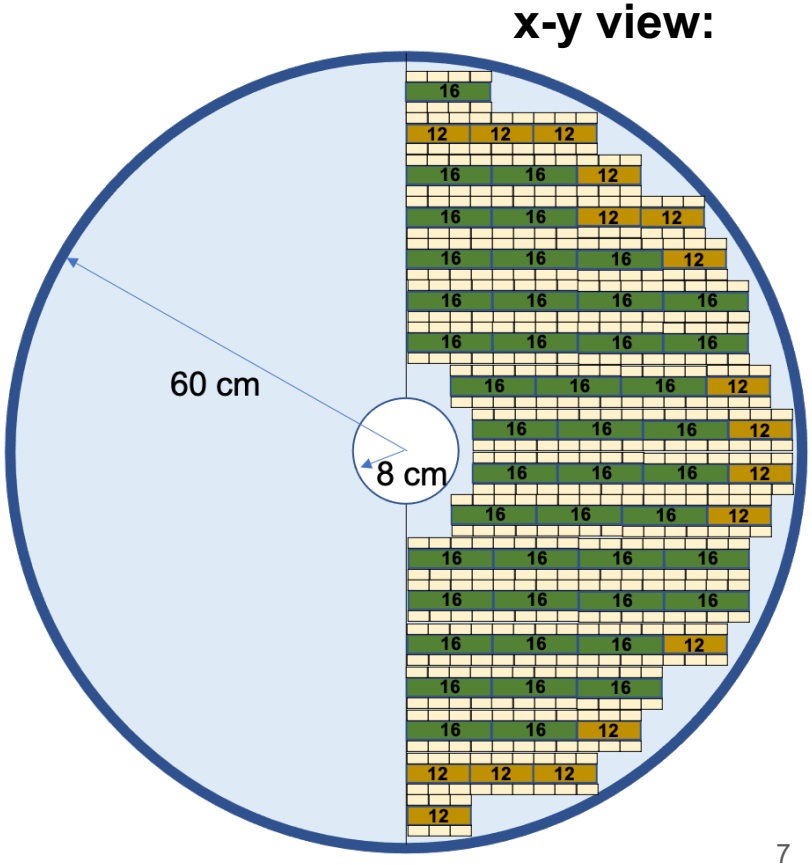
FTOF detector layout (v1)

FTOF disk will consist of two “DEE”s, made of carbon fibers and cooling pipes.

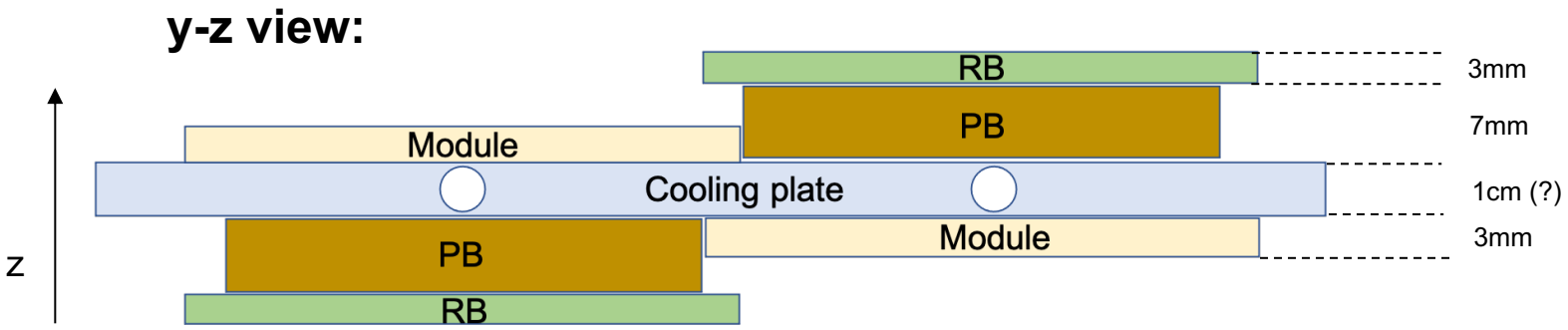
Each DEE is tiled by modules and SHs on both faces to maximize the coverage







FTOF detector layout (v1)



(illustration only, thickness not exactly to scale)

Material composition:

- RB: 1-2 mm Kapton + FPGAs
- PB: 1-2 mm Kapton + coils + bPol12
- Cooling: a few mm to 1cm? (Andy/Yi)
- Module: 1mm Si + 1mm AlN

Channel counts and power budget

	Counts
Modules	1816
Sensors/ASICs	3632
Data fiber pairs	244
LV cable pairs	244
HV cable pairs	244

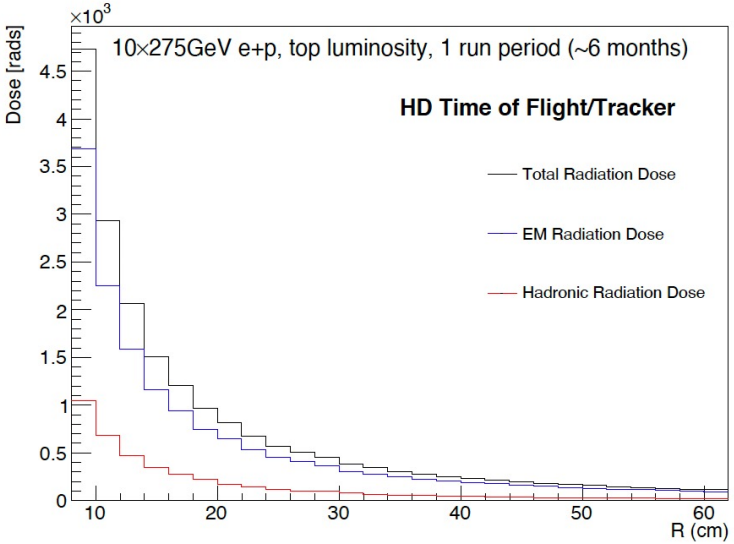
	Power
Sensors	0.3kW
EPTROC	3.6kW
DC-DC	2.5kW
FPGAs	1kW
Total	7.4kW

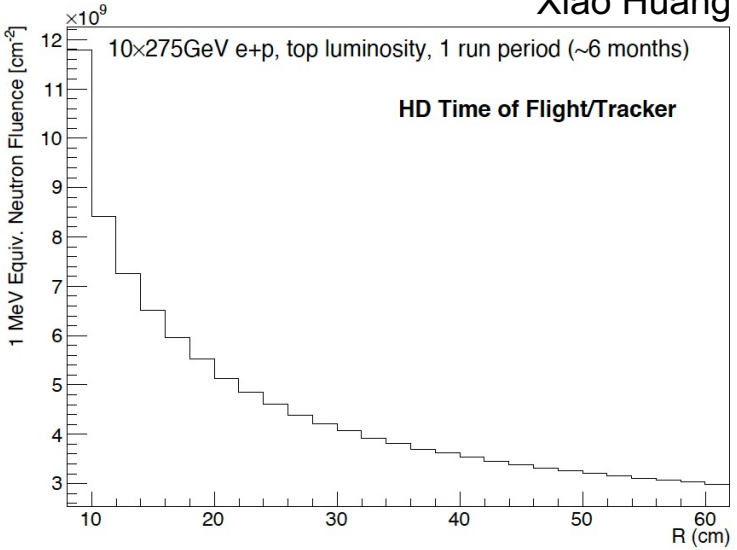
Assuming a single value of HV for each SH

Channels and power budget reduced from v0 mainly because of reduced envelope

FTOF radiation dose

Xiao Huang





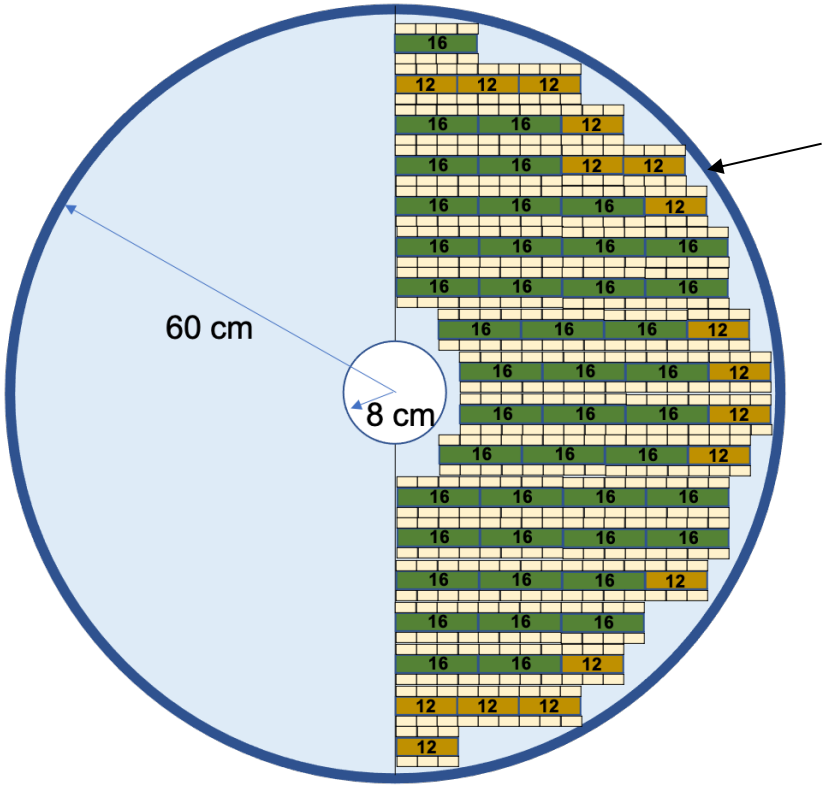
Equivalent numbers for CMS ETL at HL-LHC is up to ~10^6x higher

- R-dependent HV map is necessary to maintain unform gains toward the end of lifetime
- Each SH is designed to provide up to 4 different HVs (thus 4 HV cables)

Necessity of multiple HV values per SH at ePIC to be determined by irradiation tests

- If needed, in which region? Possibly only needed for a small inner region, which can be implemented for a small set of SHs.

FTOF mechanics, cooling and power system



Cooling manifolds and LV/HV patch panels mounted on the rim of the DEEs to take advantage of space in the z direction and minimize impact to the active detector area

Light-weight structure made of Carbon-Fiber foam with embedded cooling tube being developed under eRD112 and PED. See more details in Andy's talk

Organization and work packages for FTOF

Organize the work in terms of work packages, each led by a coordinator. Will work together with coordinators on refining the schedule and cost estimate.

Work Package	**Coordinator(s)**	**Institutions (currently identified)**
Sensor		ORNL, SCNU
Sensor-ASIC integration		ORNL, (SCNU)
Frontend ASIC		(IJCLab/Omega), BNL, ORNL
Service Hybrid and Module PCB		Rice, BNL
Module Mechanical Structure		Purdue, NCKU
Module Assembly		LANL, ORNL, (RIKEN)

See https://indico.bnl.gov/event/20826/ for the first discussion

We highly welcome more institutes/colleagues to join the efforts and take leading roles!

Backups

Power budget (v0)

0.5x0.5 mm^2 option

0.5x0.5	Forward	Backward
Sensors	0.6kW	0.35kW
EPTROC	8.5kW	4.8kW
DC-DC	3.5kW	2kW
lpGBT, VTRx+, SCA	0.5kW	0.3kW
Power cables	0.5kW	0.3kW
Total	13.6kW	7.75kW

0.8x0.8 mm^2 option

0.8x0.8	Forward	Backward
Sensors	0.2kW	0.13kW
EPTROC	3.2kW (6.4kW)	1.8kW (3.6kW)
DC-DC	1.3kW	0.75kW
lpGBT, VTRx+, SCA	0.2kW	0.12kW
Power cables	0.2kW	0.12kW
Total	6.1kW	2.9kW

Electron-Ion Collider

Brookhaven National Laboratory