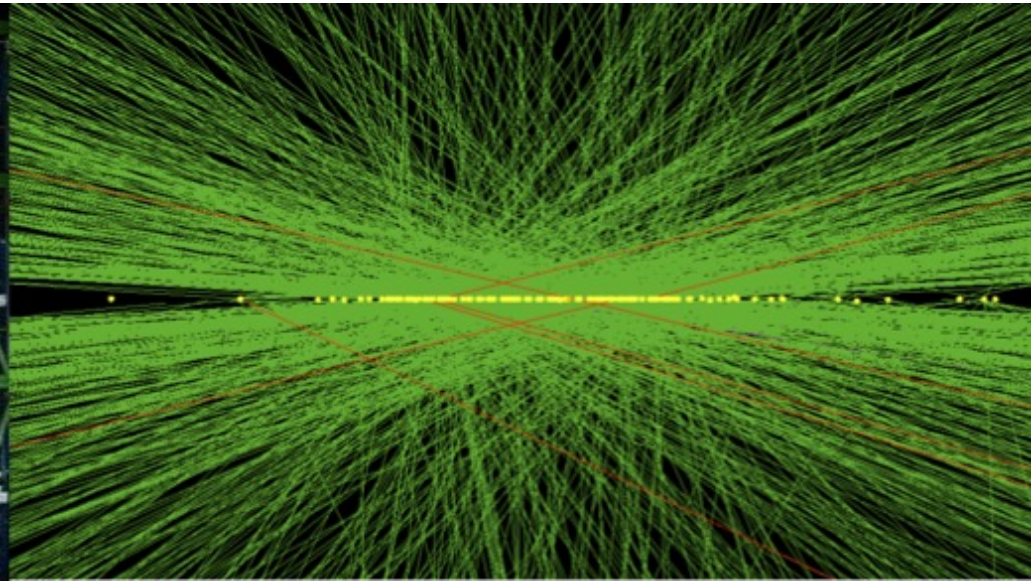
ETROC ASIC experiences

Ted Liu

Fermilab

AC-LGAD workshop, ANL

Jan 9, 2024

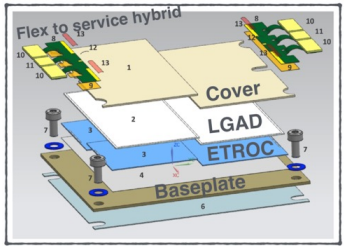


Outline

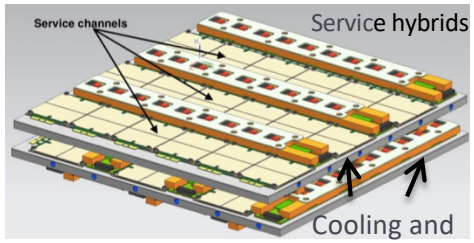
- Overview
- Technical Design
- Brief Summary of Testing Results
- Some Comments on ETROC Development Experiences

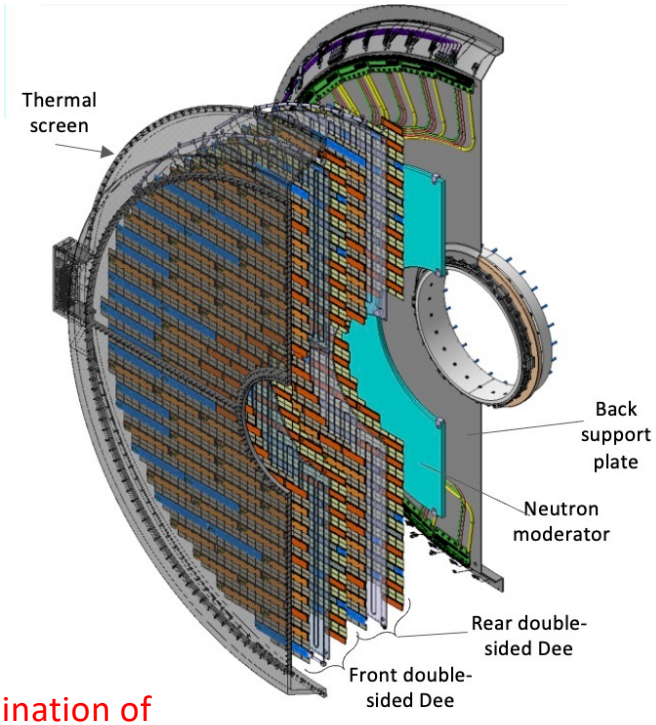
CMS ETL precision timing *challenges*

Low gain is the key ingredient to excellent temporal resolution



Module





ETL: Precision determination of the arrival time of small water drop ripples

- Low Gain Avalanche Detectors (LGADs)
  - Basic unit:
    - 2x2 cm^2 LGAD bump-bonded to ETROC ASIC mounted on two sides of cooling plates
  - Two layers/disks per endcap (~2 hits per track)
  - $1.6 < |\eta| < 3.0$, surface ~14 m^2; ~9 M channels
  - Nominal fluence: ***1.7×10^{15} n_{eq}/cm^2*** (@ 3000 fb^{-1})
- LGAD gain modest: 10-30
  - LGAD Landau contribution: ~ 30ps
  - ***Front-end contribution should be kept < 40ps***
  - < 50ps per hit, or 35ps per track (with 2 hits)
- ***Extract precision timing from***

  Small LGAD signal (range: 10 -20 fC)
  - ***With low power: < 4mW/channel on average***

Challenges:

Low power and fast/precision timing,
Precision clock distribution,
Minimizing readout digital activities

Design considerations for precision timing detector

- System power and cooling constraint and how it influences ASIC design
- Design methodology to optimize front-end from system point of view
- Single layer detector vs multi-layer (ETL design: 1 layer →2 layer)
- TDC design choice: very low power required → new design
- Precision clock distribution considerations: from system to detector, to chip, to pixel and to each TDC delay unit (using H-tree approach)
- Design to enhance physics reach:
  - such as detection/trigger for long live particles, with wide TDC window
- Design for testability, monitoring and calibration considerations:
  - Internal pattern generator within each pixel
  - Internal automatic threshold calibration within each pixel
  - waveform sampler
  - FPGA emulator
- …

Proper System Design is the Key to the success of any challenging ASIC project

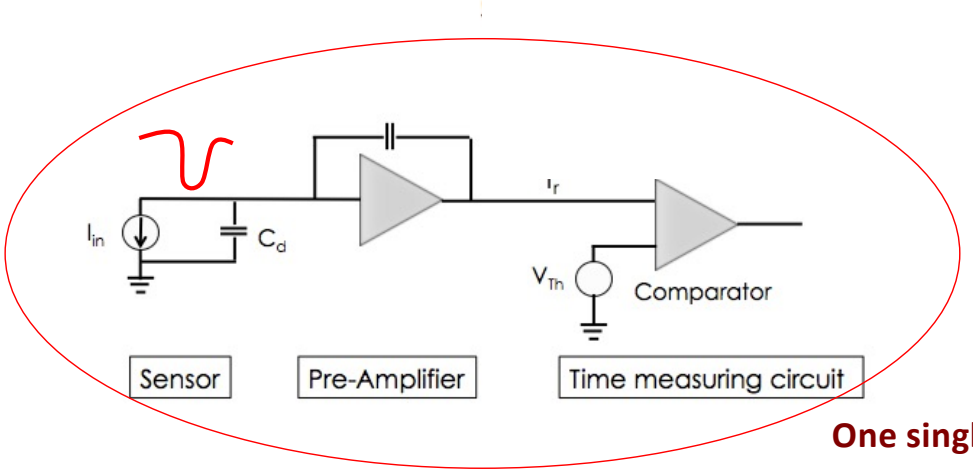
A good design is a compromise between system design and ASIC design

Our approach: "ASIC == A System design Including a Chip"

One system: sensor and ASIC

A slide from Nicolo Cartiglia

- Sensors produce a current pulse
- The read-out measures the time of arrival



One single system

Sensors and read-out are two parts of a single object, sometimes even on the same substrate

Sensors and electronics succeed (or eventually fail) together

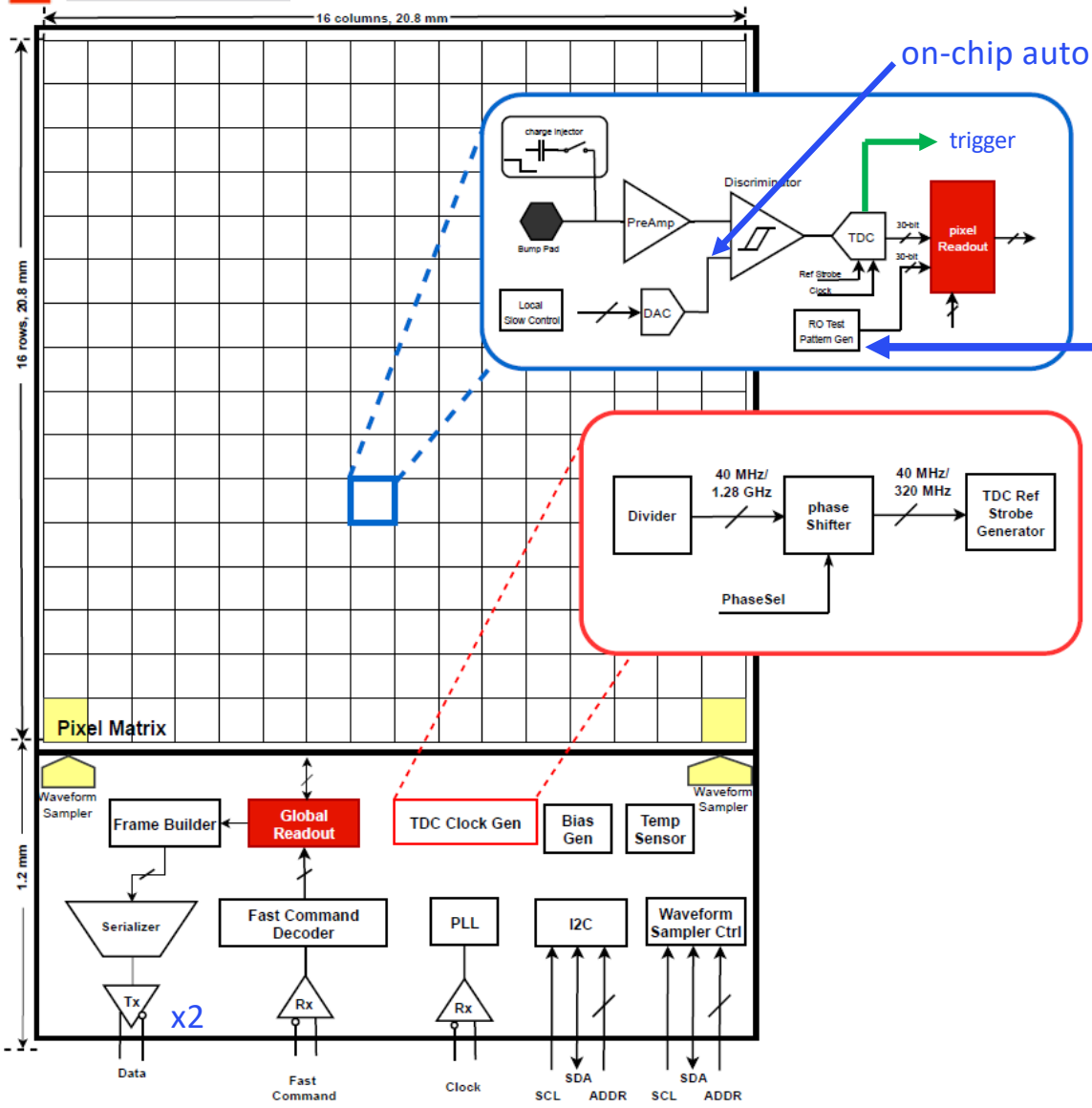
In “timing circuits” things can go wrong very rapidly (quote stolen from a chip designer)

==> This is not a simple evolution of what we know how to do.

From the very beginning, the ETROC front-end design team and the sensor expert have worked very closely together, and the front-end was optimized using LGAD simulation files provided by Nicolo.

ETROC Design

ETROC is designed to process
LGAD signals with time resolution
~50ps per hit, ~35 ps per track with 2 hits.



on-chip auto threshold calibration

ASIC/FEE contribution should be kept < 40ps
Discriminator threshold: ~ 5fC

Self-test capability (for ***design verification*** & chip and system level testing with backend)

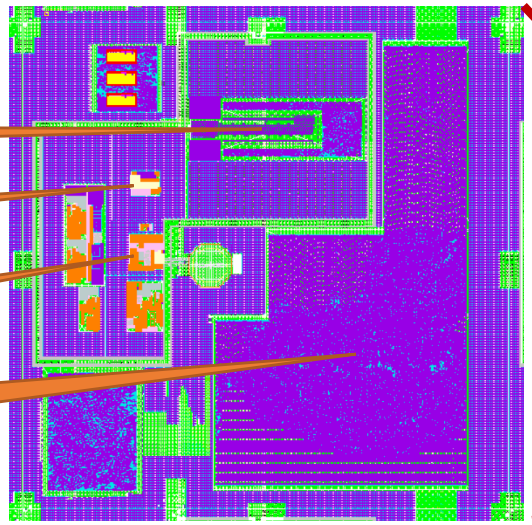
- Measuring arrival time of LGAD signal
  - Front-end: PA + Discriminator + TDC
  - L1 latency circular buffer
  - L1A-driven readout with zero suppression
  - A coarse map of ***delayed*** hits for L1 trigger
- Interface of ETROC2
  - 40 MHz reference clock
  - I2C-based slow control
  - 320 Mbps fast control
  - Serial data link 320/640/1280 Mbps
- Waveform Sampling of preamp output (only 1 pixel)
  - For test & monitoring purpose

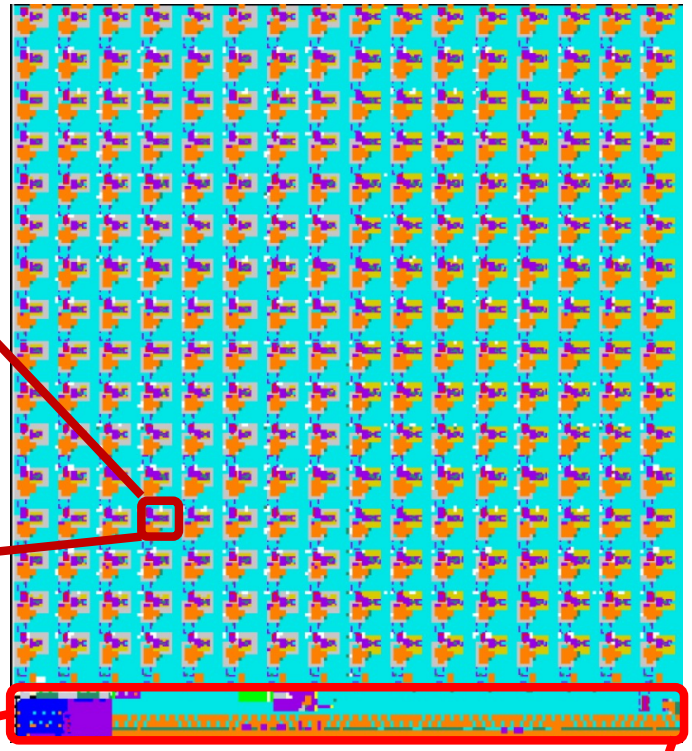
2.5 V for efuse (will require 2.5V once)

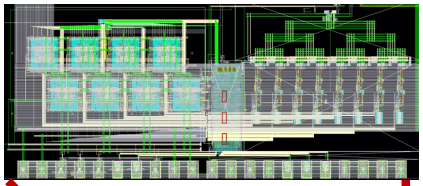
ETROC2 is designed in such a way as if it is the final design, with full functionalities

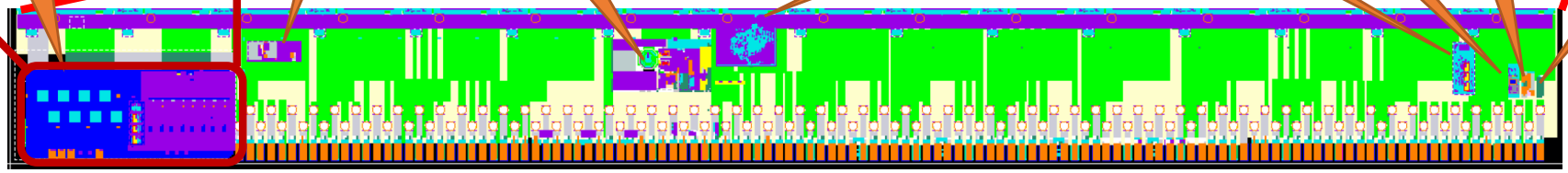
(with extra flexibilities for performance study purpose)

ETROC2 layout (submitted on Oct 21, 2022)









ETROC2 key features: from testing/user point of view

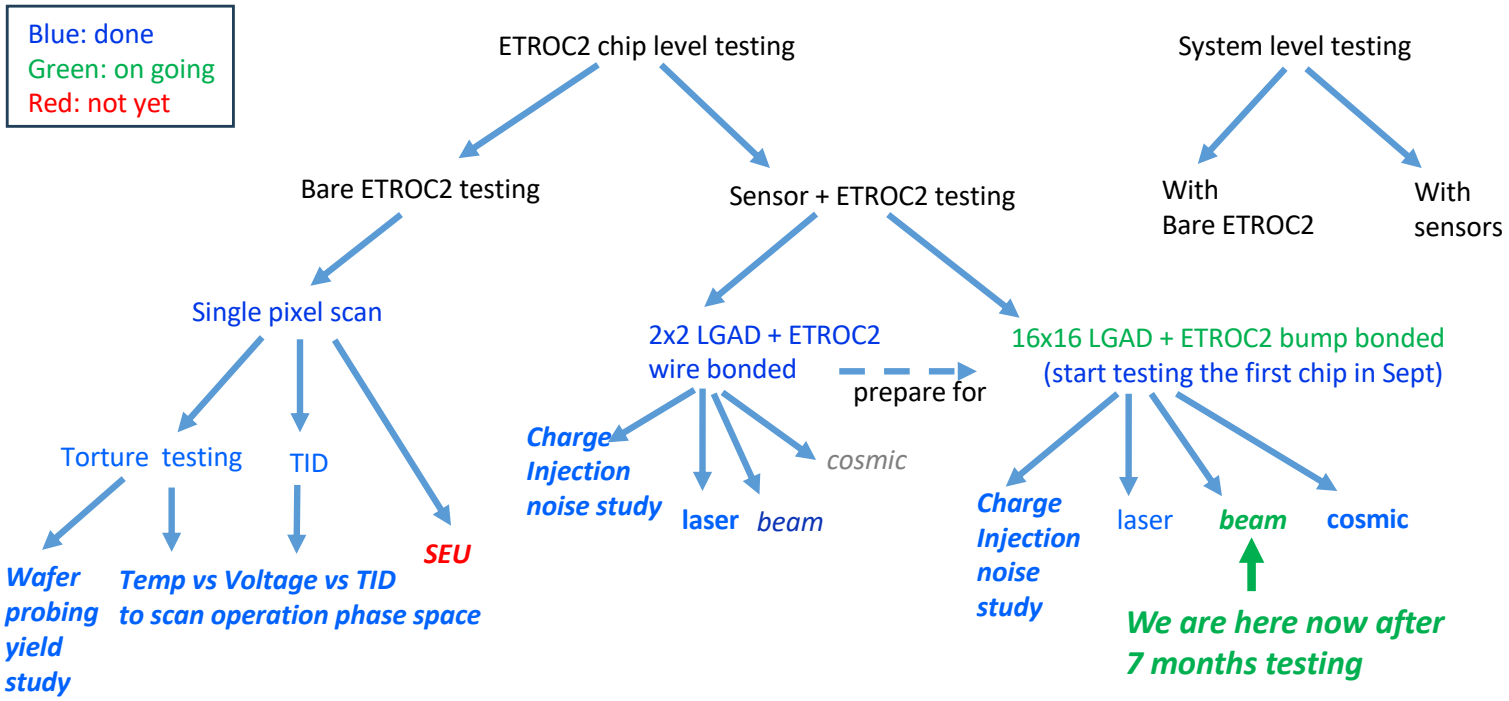
First round of testing done, chip functional well

seven months into testing so far, a lot has been done

- **Self-test pattern generator**
  - Can be used to test the digital data flow and link interfaces. Users can dial the occupancy of pixels and change patterns
    - been used extensively to simulate and verify the readout design of ETROC2, with emulator as well
    - for testing at chip level (as *build in self-testing capability*), board level, and system level (with DAQ backend)
- ***Charge injection***
  - *full path: charge injection to preamp to discriminator to TDC to circular buffer to event buffer to global digital readout*
- ***DAQ readout***
  - User adjustable TOA measurement window (up to 12.5ns, 11.4ns effective)
  - User adjustable windows for TOA, TOT and CAL to filter/suppress hits before readout
  - Each pixel can be enabled or disabled for DAQ readout/trigger
  - The relative phases adjustable between the TDC clock, pixel readout clock and global readout clock
  - …
- ***Auto-threshold scan within each pixel***
  - Automatically determine the threshold and noise level, and set the threshold with user-adjustable offset
- ***Trigger path (used beam testing as self-triggering)***
  - Can be used for monitoring purpose initially, a coarse map of user defined hits continuously sent out every BC
  - Can be used for self triggering for beam test if so desired, user can define the window for TOA, TOT and CAL for triggered hit
  - Use flashing bits in empty BCID (beam gap), defined via I2C. Can be used as cross check and monitoring purpose.
- ***Waveform Sampler***
  - record waveform of one pixel up to 16 bunch crossing (400 ns), start and stop controlled via fast command, readout via I2C
  - power-down when not used, intend to use for monitoring purpose during detector operation
- ***Power consumption ~1W per chip, confirmed with ETROC2 chips***

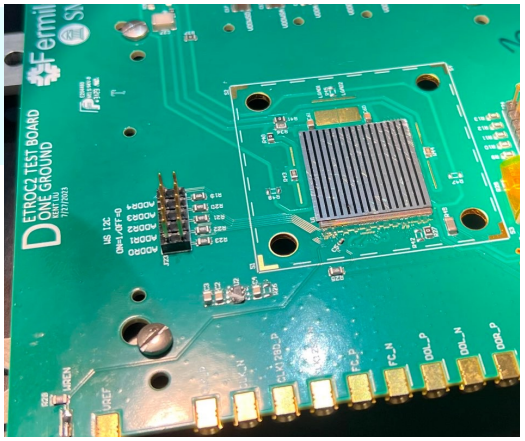
ETROC2 chip level testing road map

ETROC2 chips received in late April 2023

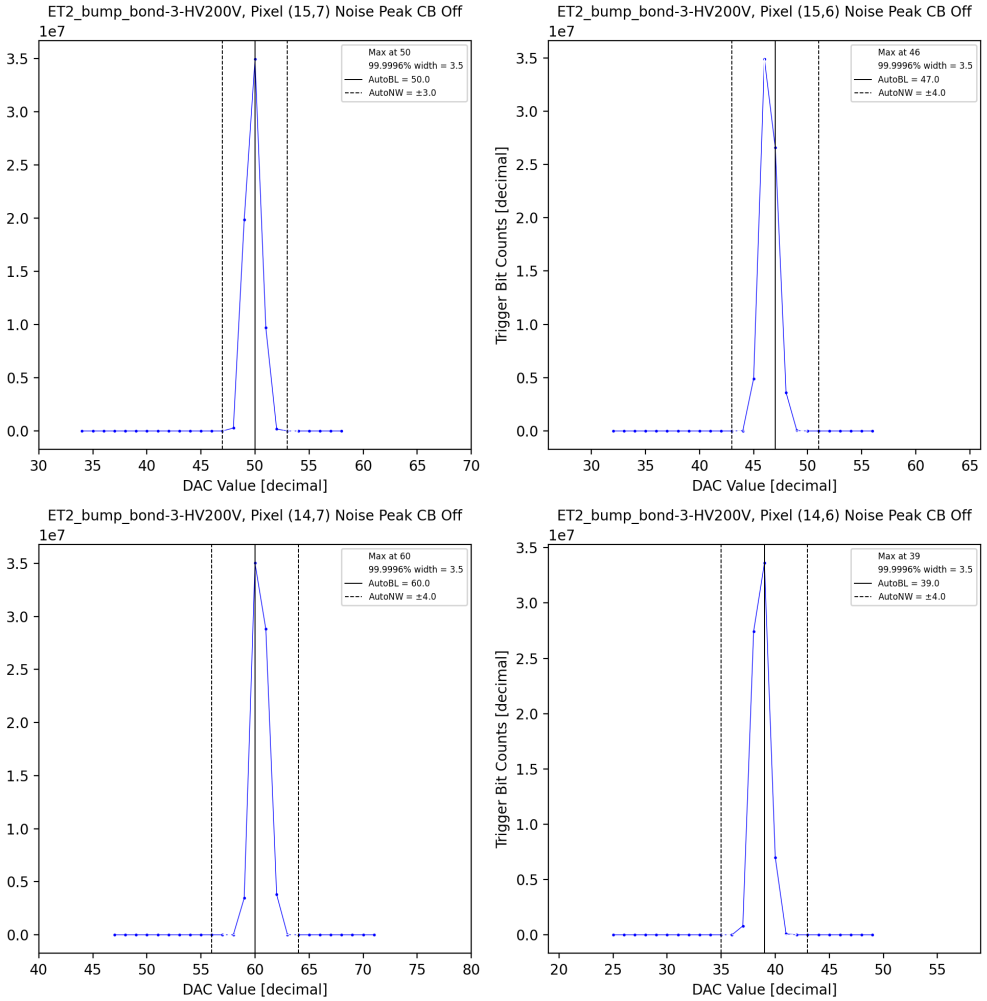


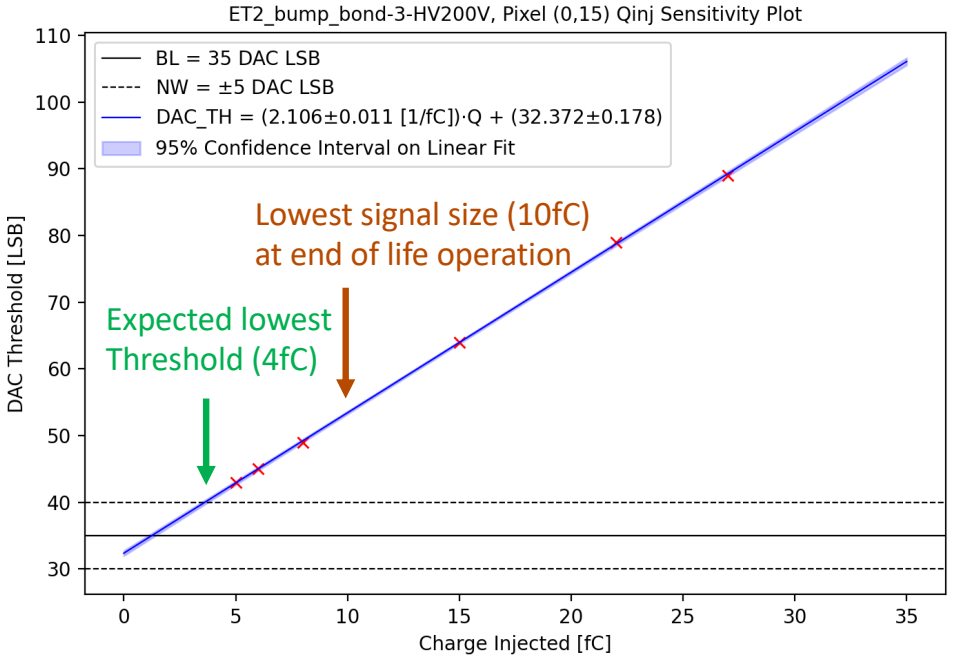
First beam test at CERN in Sept 2023: commissioning run successful
Second beam test at DESY (Dec 2023): two weeks beam test successful, analysis on going;
More beam tests reserved at DESY in 2024, requesting beam time at CERN as well
SEU testing scheduled for end of Jan, April and June

Bump bonded ETROC2



Noise level meeting our requirements





The minimal signal at the end of life operation is >= 10 fC.

From a noise perspective, this performance provides sufficient margin.

Measured (bump bonded) ETROC2 performance with charge injection

ETL spec is ~ 50 ps per hit:

LGAD contribution: ~30ps

ASIC contribution:

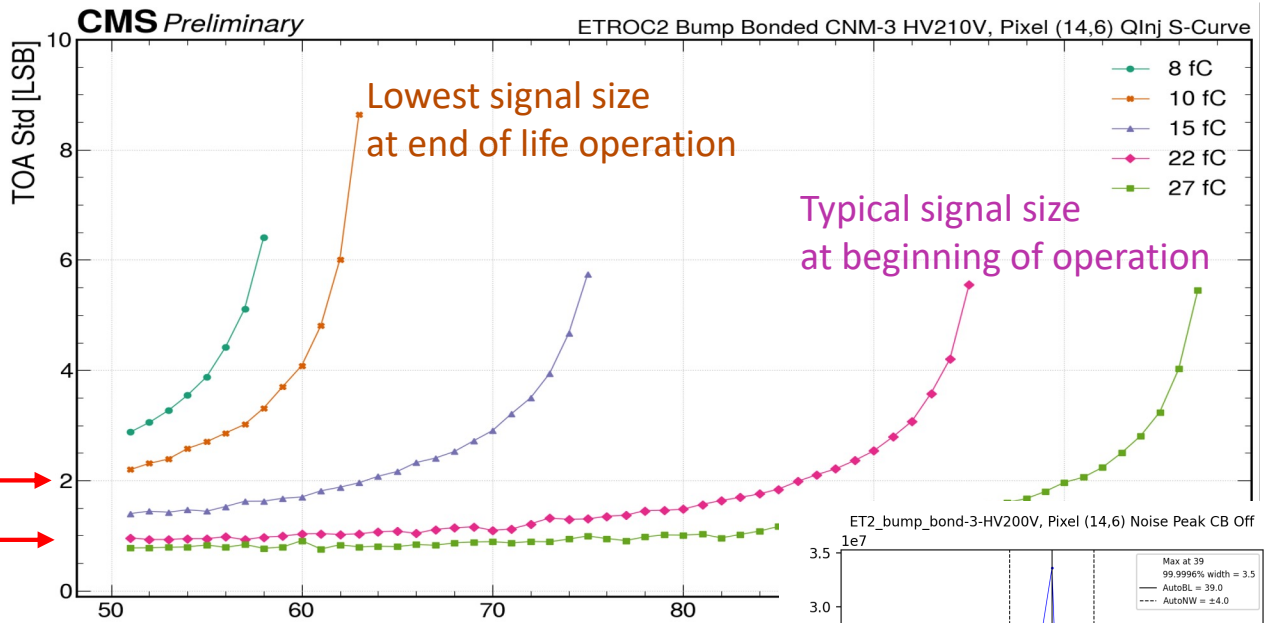
Expected performance:

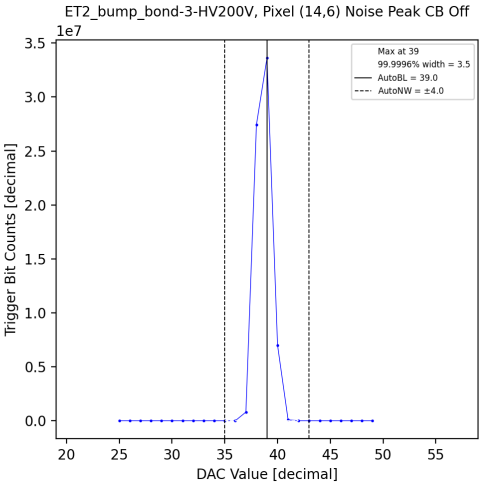
LGAD+ preamp/discriminator + TDC bin	34 / 40 ps
Time-walk correction residual	< 10 ps
Internal clock distribution	< 10 ps
System clock distribution	< 15 ps
Per hit total time resolution	39 / 45 ps
Per track (2 hits) total time resolution	28 / 32 ps

Initial operation: 39 ps per hit

End of life operation: 45ps per hit

With safety margin for ~50ps spec

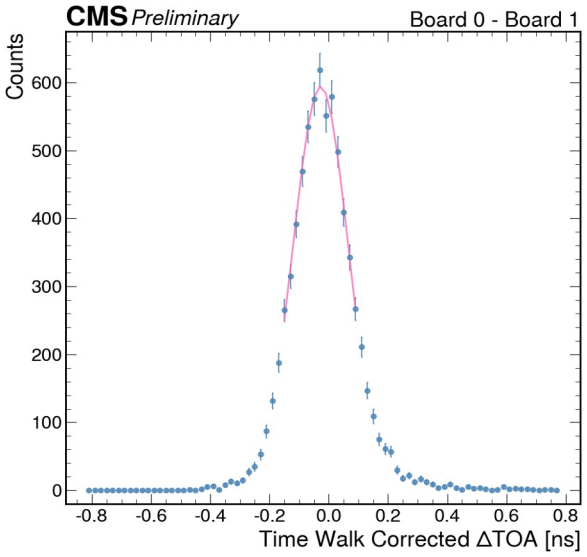


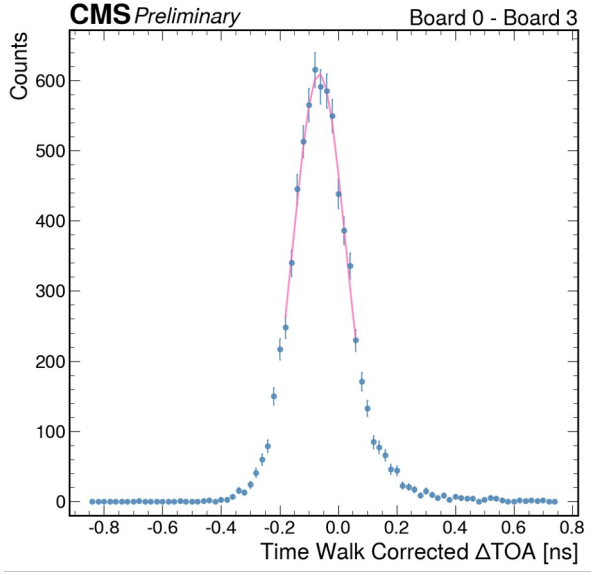


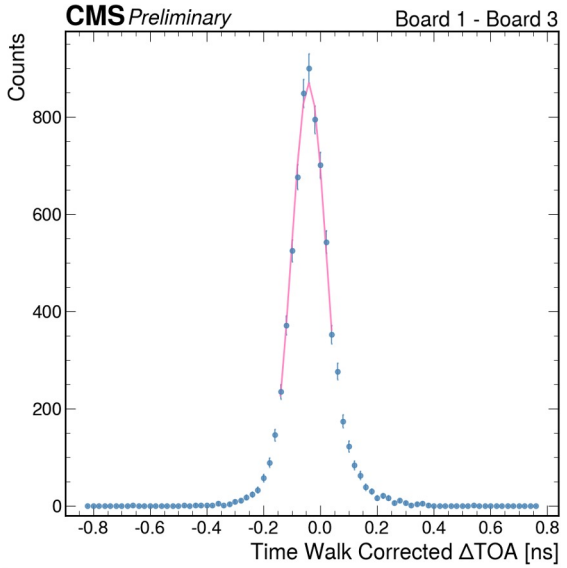
CAL ~207

TOA bin=15ps

Preliminary result from beam data







The very first CERN beam test (Sept 2023) was just for testing the telescope operation hardware, firmware and software (online & offline), to better prepare for DESY beam test in Dec 2023. not meant for performance study.

Nevertheless, we performed some data analysis to check the data integrity, even though the setup was not optimized.

The usual analysis procedure:

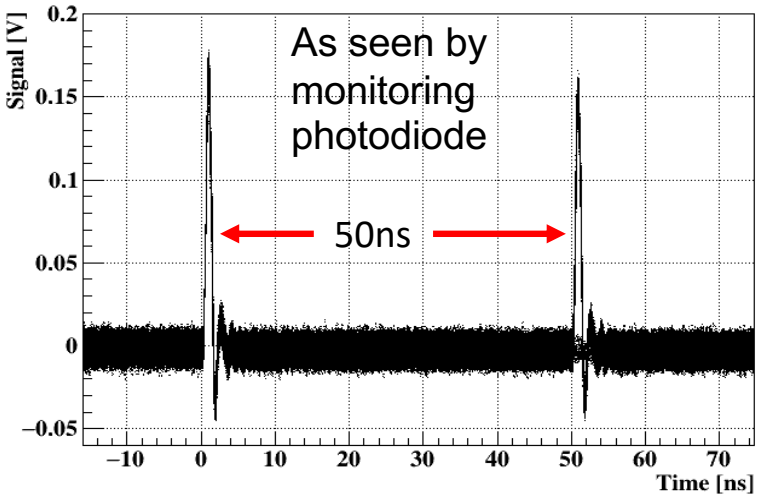
1. Convert TOA and TOT in [ns] from TOA code and TOT code
2. Construct the pairwise differences $T_{ij} = TOA_i - TOA_j$
3. Perform time walk corrections
4. Extract widths σ_{ij}
5. Time resolution $\sigma_i = 1/\sqrt{2} \times \sqrt{(\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2)}$

⬇

The derived time resolution of DUT (Board 3): 39 ps with discriminator threshold at ~5fC

First look at bump bonded ETROC2 performance with a double pulse IR laser at CERN-SSD

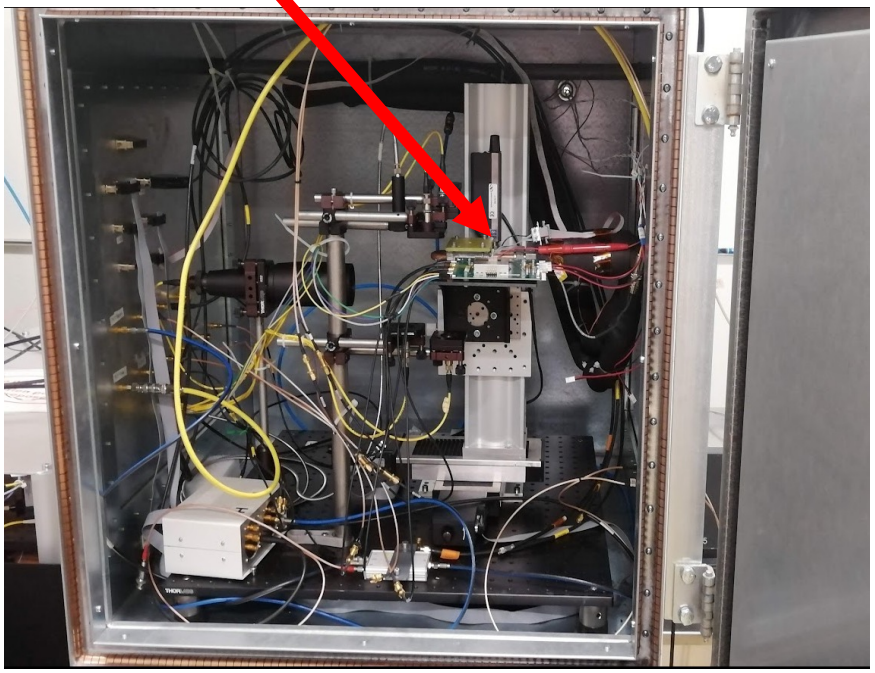
$$\sigma_{ToA}^2 = \sigma_{laser}^2 + \sigma_{Clock}^2 + \sigma_{sensor}^2 + \sigma_{ETROC2}^2$$



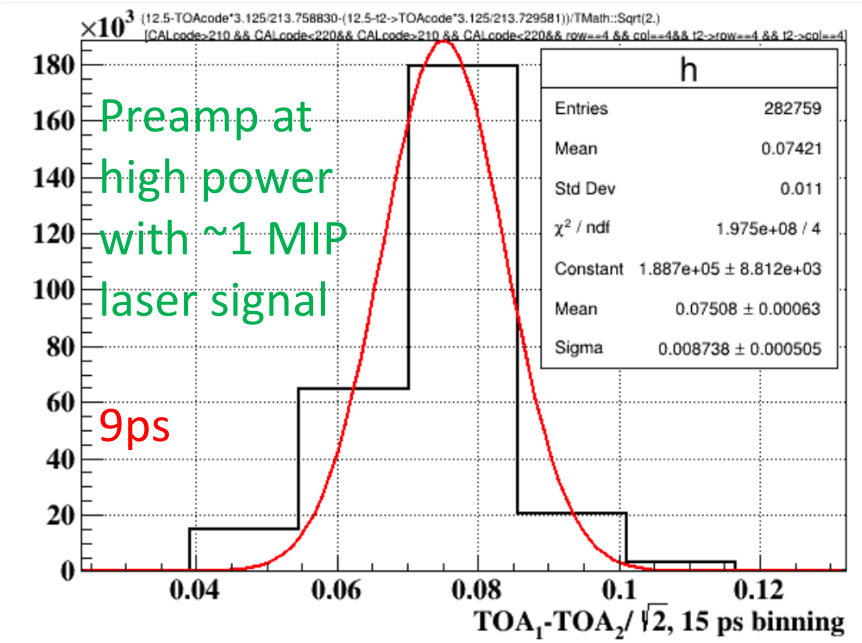
Jitter is calculated as:

$$\frac{\sigma_{(TOA_1 - TOA_2)}}{\sqrt{2}}$$

ETROC2 bump bonded with 16x16 sensor



Two pulse "timing" configuration



ETROC Overall Status

Preamp + discriminator + TDC:
Very first version works well enough, went into ETROC2 without any modification

- ETROC0 (single channel, preamp + discriminator)
  - Beam testing: ~30ps achieved in beam
  - TID test to 100Mrads: works
- ETROC1 (4x4), with ETROC0 preamp/discriminator + new TDC
  - New TDC: excellent performance (<~6ps resolution) with robust operation
  - New 4x4 H-tree: works well, designed to be scalable to 16x16
  - ETROC1 and LGAD sensor bump-bonded
    - ***achieved ~ 40ps per hit in beam with threshold at ~8fC***
- ETROC2 (16x16)L: ***full size and full functionality***, submitted Oct 2022
  - ***All ETROC2 analog blocks have been silicon proven in prototype chips, re-used in ETROC2 without modification***
  - ***All digital designs/interface emulated in FPGA, tested with down stream all the way to back end***
  - ***ETROC2 is working well after seven months intense testing***
    - ***Bump bonded ETROC2 noise level is excellent, initial cosmic/laser/beam testing with promising results***
      - ***Initial beam test: observed time resolution at 39 ps with threshold at ~5fC, within specifications***
    - ***Voltage (1.0 – 1.3 V) vs temperature (-30C to 30C) vs TID (tested up to 200 MRad) scan: all works***
    - ***Wafer probing test shows high yield***
    - ***Tested successfully with module, readout board and power board prototypes***
    - ***SEU testing to be done, first test scheduled end of Jan 2024***
- ETROC3 (16x16): intended as final version, submission in 2024
- ETROC3 production: 2025

Dedicated Technical Reviews in the past:
Three “God Parents” technical reviews (2018-2021)
ETROC2 features review (Oct 2021)
ETROC2 pre-submission review (July 20th, 2022)
ETROC2 final submission review (Oct 7th, 2022)
ETROC2 final submission to IMEC (Oct 21, 2022)

Some Comments on ETROC Development Experience

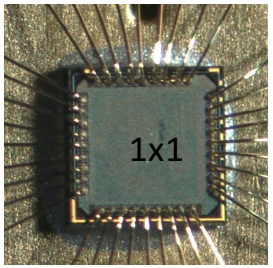
- Design spec development strategy: from system to chip
  - ASIC: A System design Including a Chip
- Development strategy: divide and conquer 1x1 → 4x4 → 16x16
  - Skipped 8x8 step, went straight to full size and full functionality ETROC2
  - Learned a great deal from ETROC1 (4x4), esp the need to minimize digital activities
- Design choice:
  - preamp/discriminator: text book design, optimized for ETL LGAD at end of life
  - TDC: new design from scratch, for simplicity and low power
  - Readout: new design with new readout architecture
  - Other design blocks: borrow existing blocks from other projects as much as we could
- Clock distributions: H-tree approach with shielding structures
- Analog on top vs digital on top
- Verification strategy
  - All analog blocks silicon proven before ETROC2
  - All digital blocks emulated in FGGA and tested with downstream
- Submission strategy:
  - With wafers on hold, to allow revisions to fix minor issues (free of charge)
  - With corner wafer lot
- Beam test strategy: use the simplest ETROC telescope
- System development strategy before ETROC2
  - Use ETROC2 emulator to help the system development
- … many more

ETROC prototyping: what has been done

Sept 2018 | Dec 2018 | May 2019 | Aug 2019 | March 2020 | May 2020 | July 2021 | Sept 2021 ...

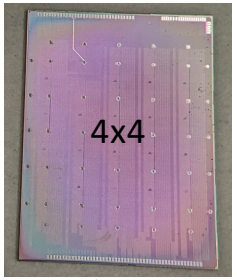
Project started

ETROC0 submitted



Preamp + discriminator

ETROC1 submitted



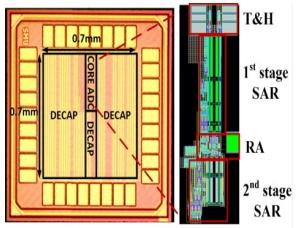
Preamp + discriminator + TDC
4x4 H-tree clock distribution

Covid

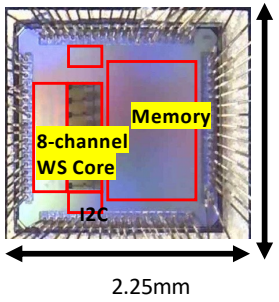
ETROC2: 8x8 → 16x16

Decision to go for full size full functionality ETROC2, Delay submission and add few test chips …

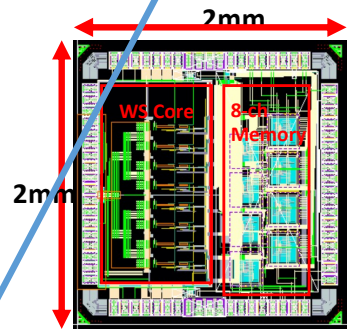
Single channel ADC submitted



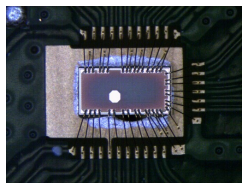
8-channel ADC Waveform Sampler (WS1) submitted



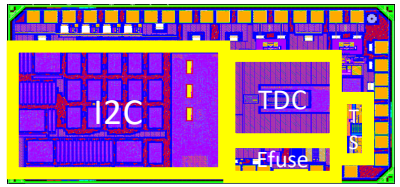
Rad-hard version of Waveform Sampler (WS2) submitted



ETROC-PLL mini ASIC submitted



I2C Test chip submitted



Total of 7 small chips, all successful

All analog blocks have been silicon proven in test chips
ETROC2 FPGA emulator: has verified digital readout and system interfaces

ETROC2 was submitted (Oct 21, 2022), testing started in later April 2023

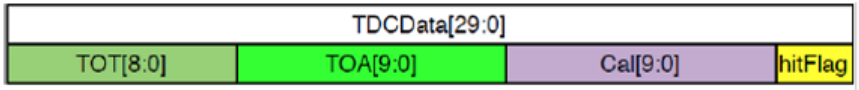
Design team: FNAL/SMU/LBNL/UCSB
Testing team: FNAL/SMU/UIC/UCSB/Lisbon/IFAE with students from KSU/KU

ETROC1 TDC Design

- TDC requirements
  - TOA bin < ~30ps, TOT bin < ~100ps ***(achieved: 18 ps TOA bin, 36ps TOT bin)***
  - Lower power highly desirable
    - ***ETROC TDC design goal: < 0.2mW per pixel (achieved 0.1mW)***
- ETROC TDC design optimized for low power
  - A simple delay line without the use for DLL's to control individual delay cells, with a cyclic structure to reduce the number of delay cells, to measure TOA & TOT at the same time
- ***In-situ delay cell self-calibration technique***
  - For each hit, will use two consecutive rising clock edges to record two time stamps, with a time difference of the known 320 MHz clock period: 3.125ns
    - TOA bin size = 3.125ns / CAL_code
    - CAL_code is the difference between the two time stamps
  - Important to reach the required precision using a tapped delay line with uncontrolled delay cells (thus lower power)

For TDC details: see TDC paper
https://ieeexplore.ieee.org/document/9446843

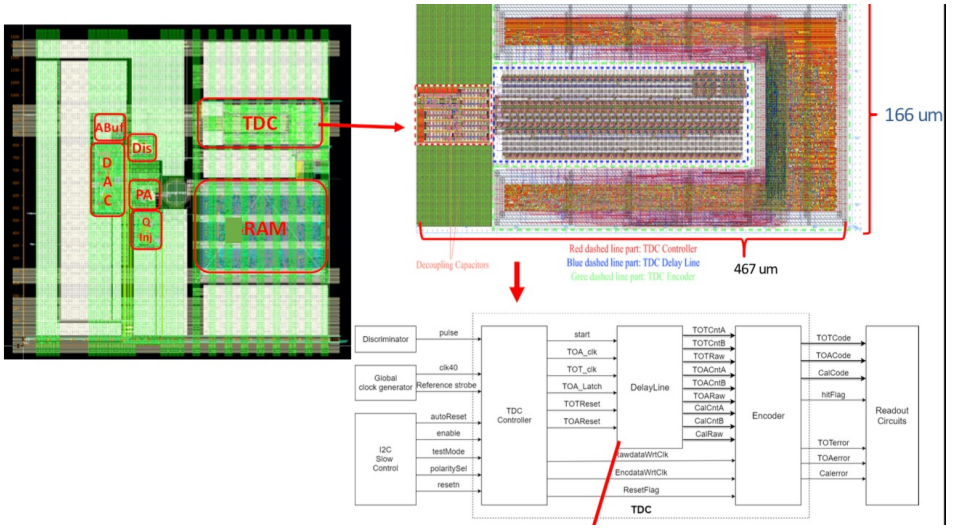
ETROC TDC

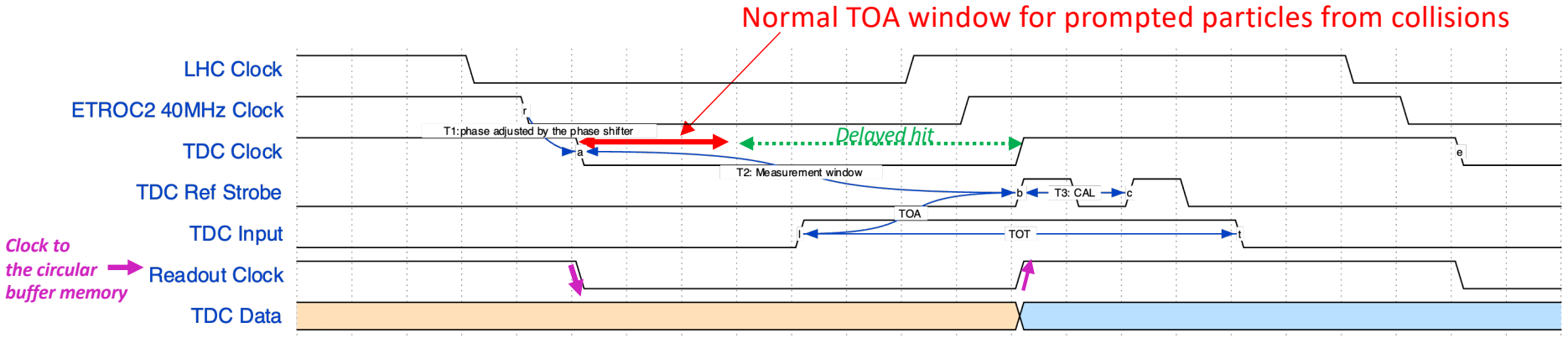


hitFlag: discriminator is fired or not

- bin= T3/Cal_code
- TOA=12.5 - bin*TOA_code

T3 is programable with 3.125 ns by default.



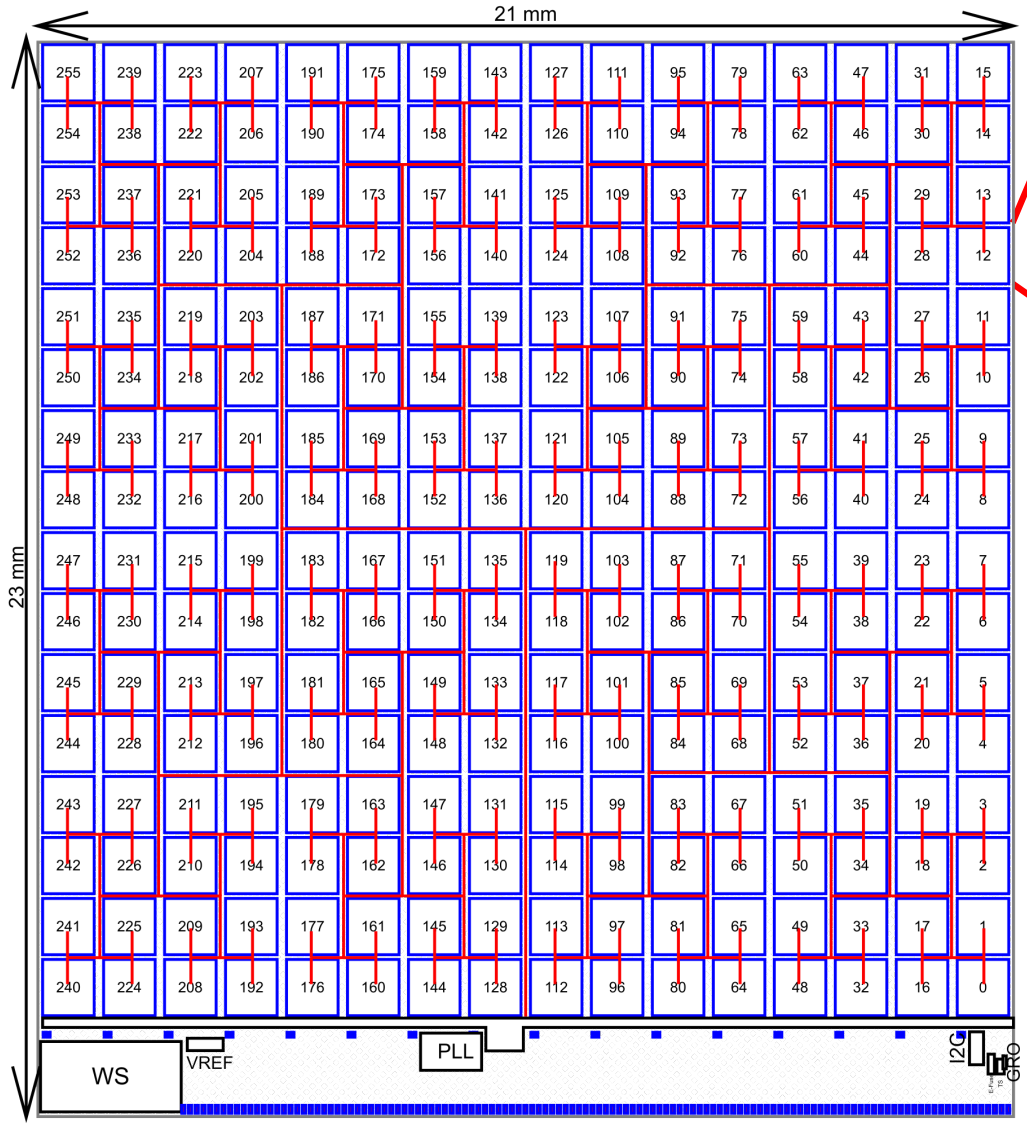


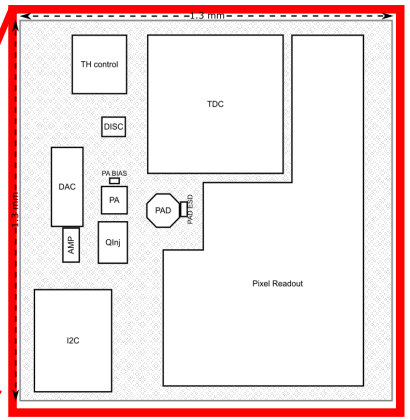
1984 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 68, NO. 8, AUGUST 2021

A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade

https://ieeexplore.ieee.org/document/9446843

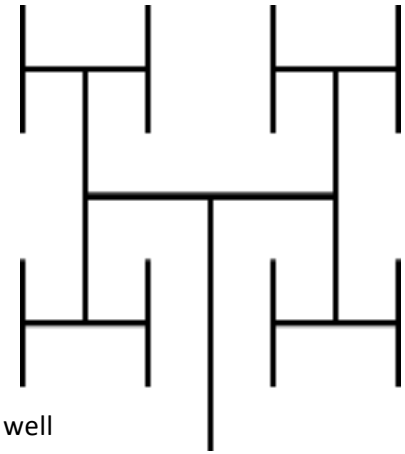
ETROC2 design strategy: most building blocks have been silicon proven





Front-end:
Charge injection/DAC
Preamp,
Discriminator
TDC

- PLL
  - PLL is based on lpGBT and validated with PLL test chip (+SEU)
- I2C
  - I2C design validated with I2C test chip, including SEU
  - In-pixel I2C register expanded and verified
- TS (Temp Sensor)
  - TS validated with I2C test chip
- Efuse
  - Efuse validated with I2C test chip
- VREF
  - VREF validated with I2C test chip
- GRO
  - Reusing the GRO in ETROC1
- Tx and Rx
  - reusing Tx in ETROC1
  - Reusing Rx in ETROC1(from lpGBT)
- WS (Waveform Sampler)
  - Rad-hard version tested and works well
- In-pixel threshold calibration
  - tested with ETROC0 via FPGA emulator

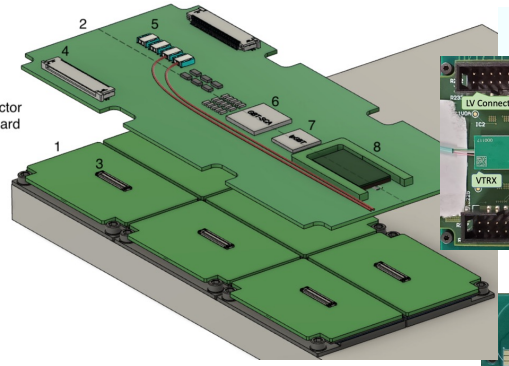


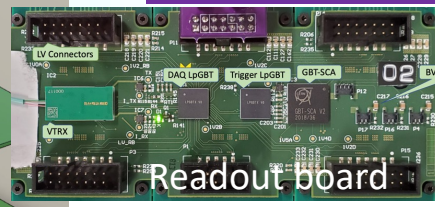
All critical analog building blocks have been silicon proven and all went into ETROC2 without modification and the digital building blocks have been emulated in FPGA and tested with the downstream readout board with backend.

ETROC system interfaces

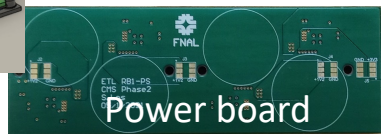
Charge #4, 5

1: Flipped module
2: Readout board
3: Board-to-board connector
4: Connector to powerboard
5: BV connector
6: GBT-SCA
7: lpGBT
8: VTRx+



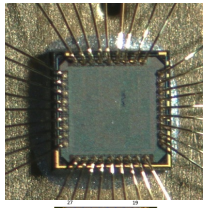


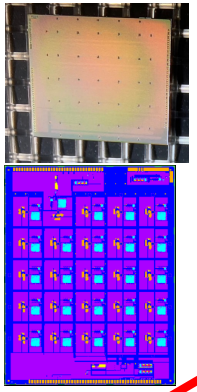
Readout board

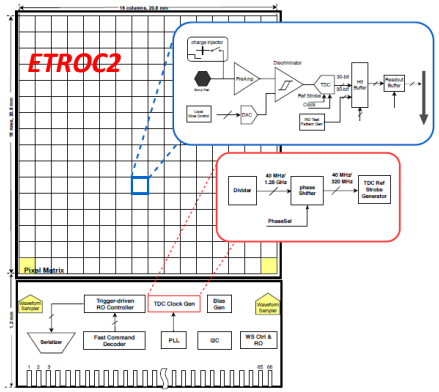


Power board

Our system development strategy:
use ETROC2 emulator to speed up system development


ETROC0


ETROC1



ETROC3

Sensor design

Bump-bonding R&D

Module design

Readout board design

Power board design

ETROC2 emulator

All designs have to be mature enough in order to finalize ETROC2 design

All prototypes have to be mature enough in order to test ETROC2 at system level in time to move to ETROC3

Backend firmware/software

Detector Cooling

Production QC needs …

Initial system level testing has been successful with the module and readout and power board prototypes together with the back-end electronics

ETROC2 Engineering Run experience

20 wafers split in 2 lots

6 corner wafers (3 FFF + 3 SSS)

ESD defects observed by TSMC

2 diced for testing
works well with high yield

14 typical wafers

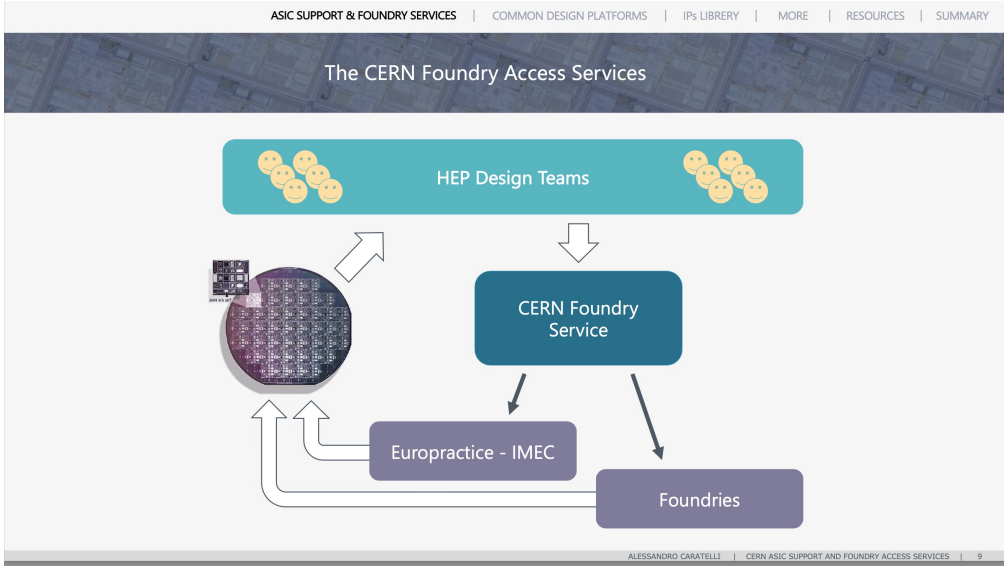
8 wafers released

2 diced for Testing
works well with lower yield

6 wafers on hold at TSMC

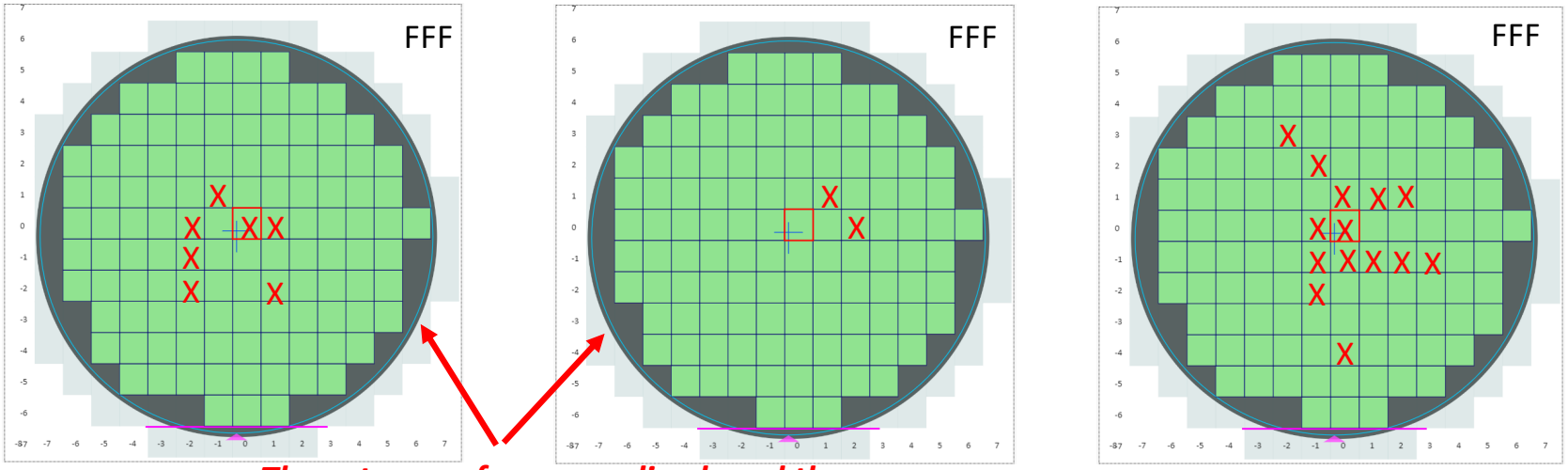
2 wafers released in July (with high yield) (H-tree shielding grounded at metal 3) processed at PacTeck for bump bonding, testing on going.

4 wafers to be released in the near future (fix known minor issues for ETROC2)



We have been working closely with CERN ASIC Support and Foundry Service, with IMEC and TSMC

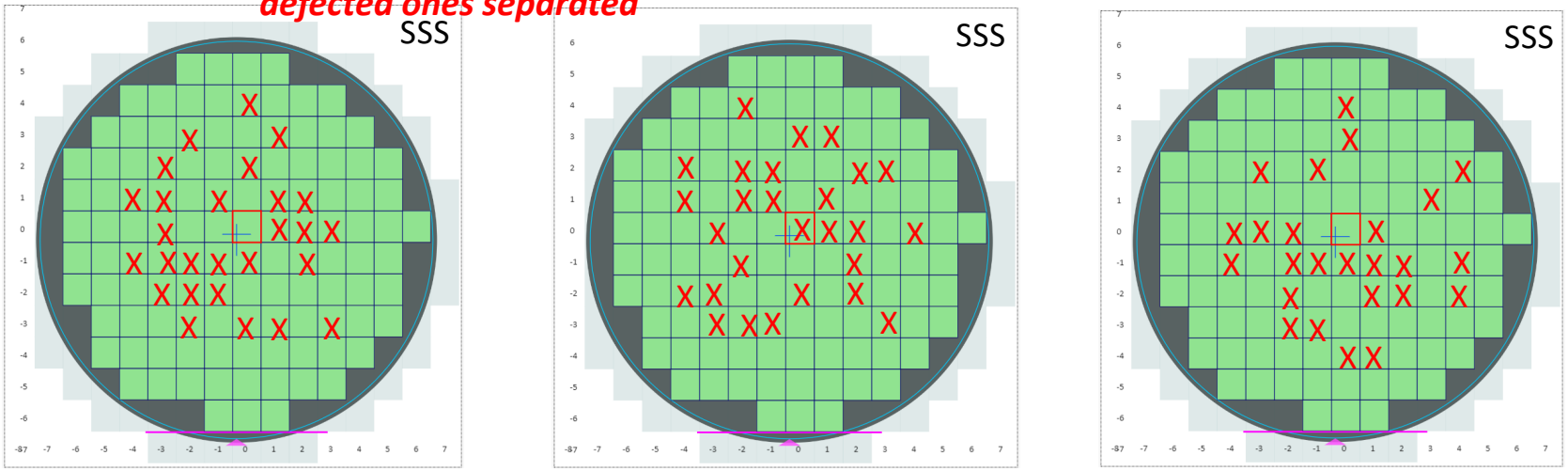
Defect map measured by TSMC from the ETROC2 corner lot: 6 wafers, with #1/2/3 in FFF corner and #4/5/6 in SSS corner



#1 #2 #3

These two wafers were diced, and the defected ones separated

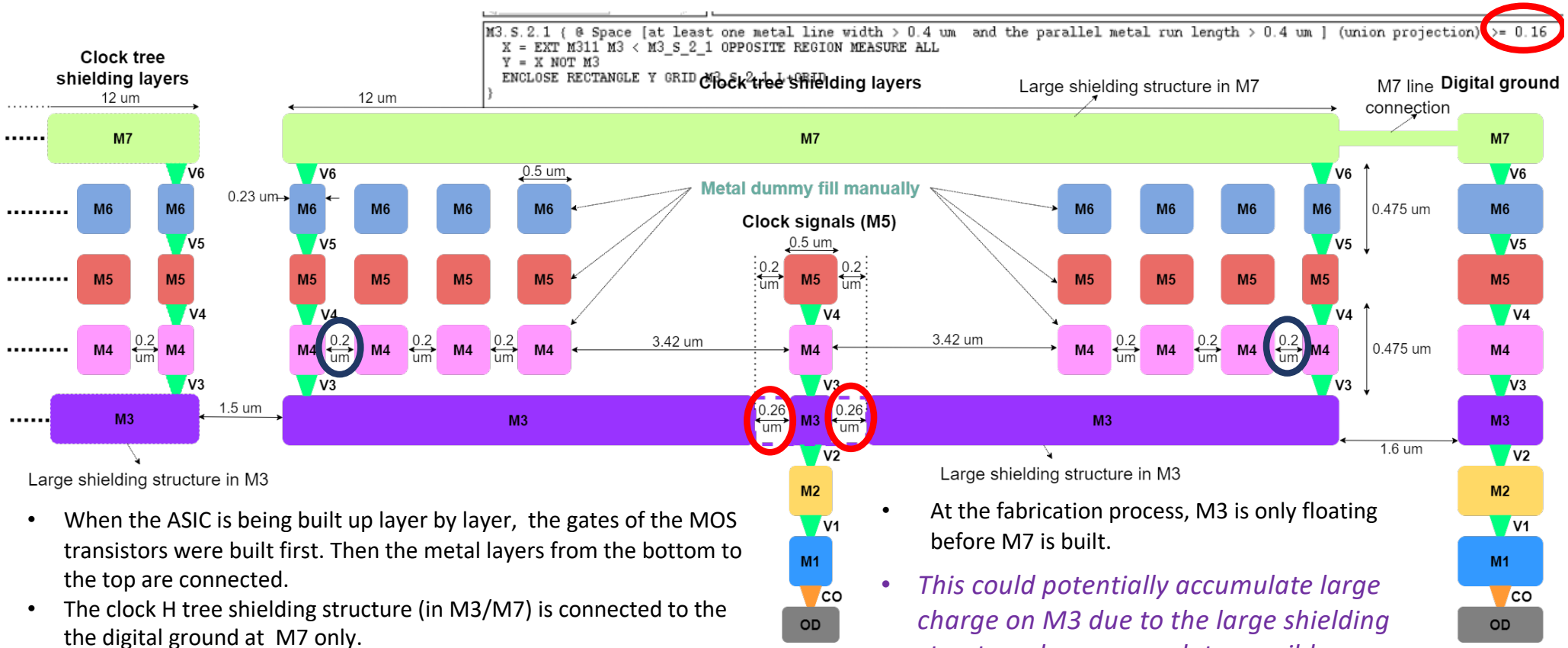
Defect ratio: 1.7% – 24.5%



#4 #5 #6

[Slide from TSMC] Feb 22, 2023

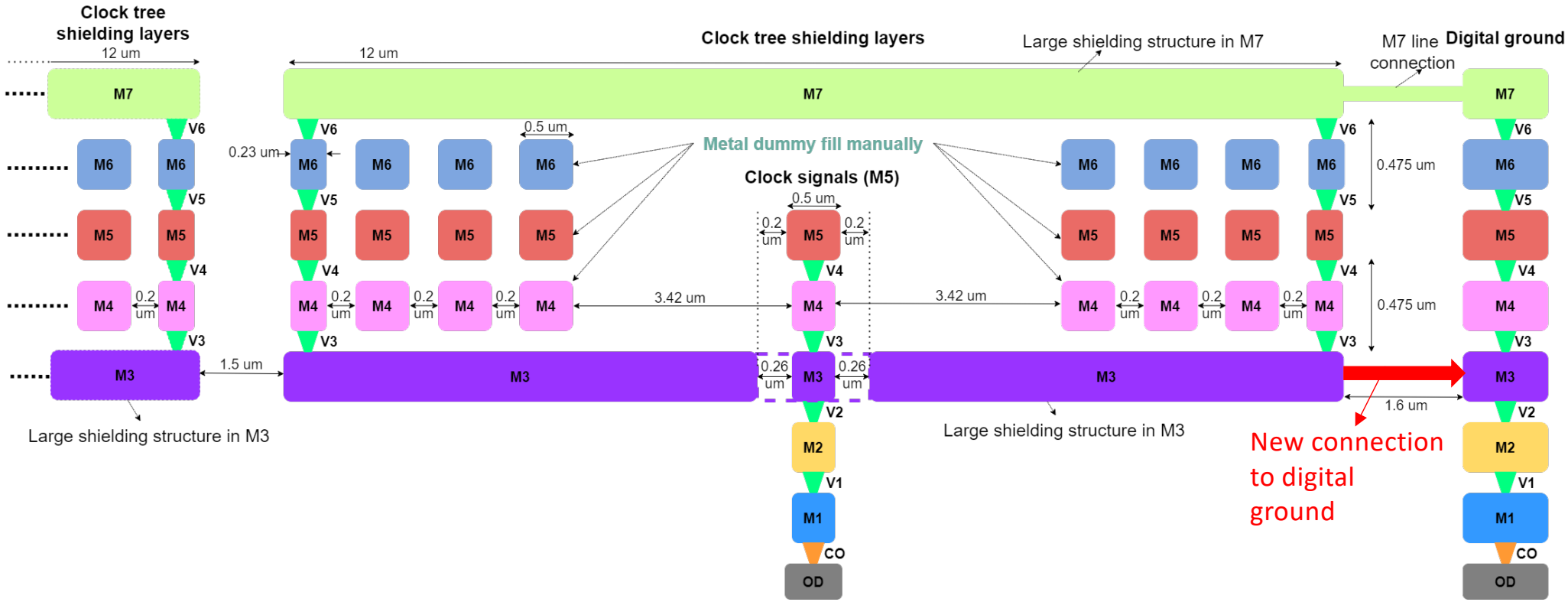
Clock tree layout cross section view



- When the ASIC is being built up layer by layer, the gates of the MOS transistors were built first. Then the metal layers from the bottom to the top are connected.
- The clock H tree shielding structure (in M3/M7) is connected to the the digital ground at M7 only.
- The relatively large shielding in M3 layer would be floating before M7 is built in the fabrication process.
- The minimum space requirement of the wide metal is 0.16 um. To play safe, we use 0.26 um space between M3 of clock signals and M3 shielding.

- At the fabrication process, M3 is only floating before M7 is built.
- *This could potentially accumulate large charge on M3 due to the large shielding structure, large enough to possibly cause damage during the fabrication process.*
- *There is no warning on this potential issue by the design tools/rules.*

Very simple solution at metal 3: grounding

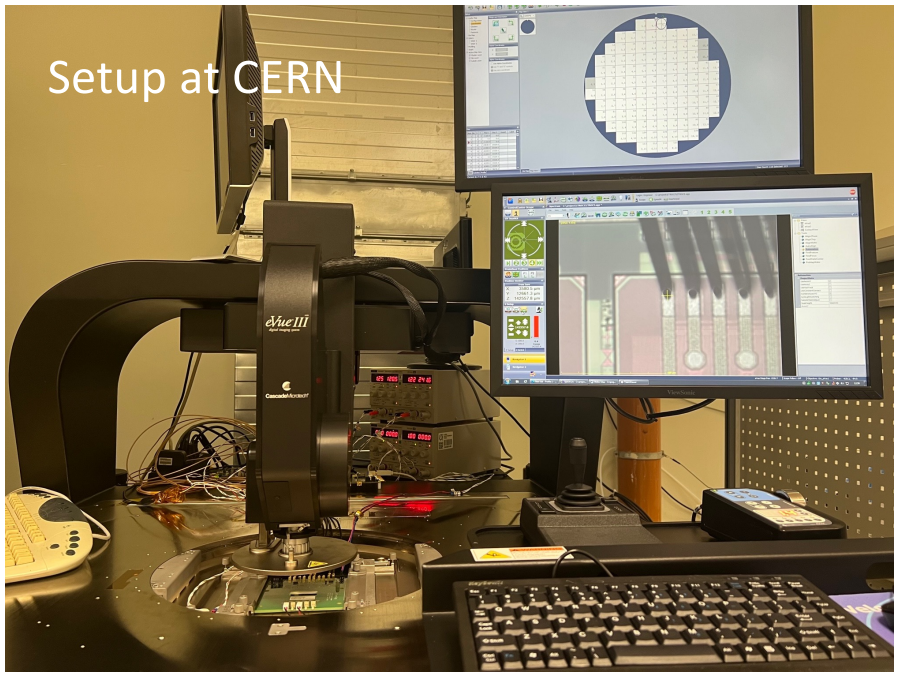


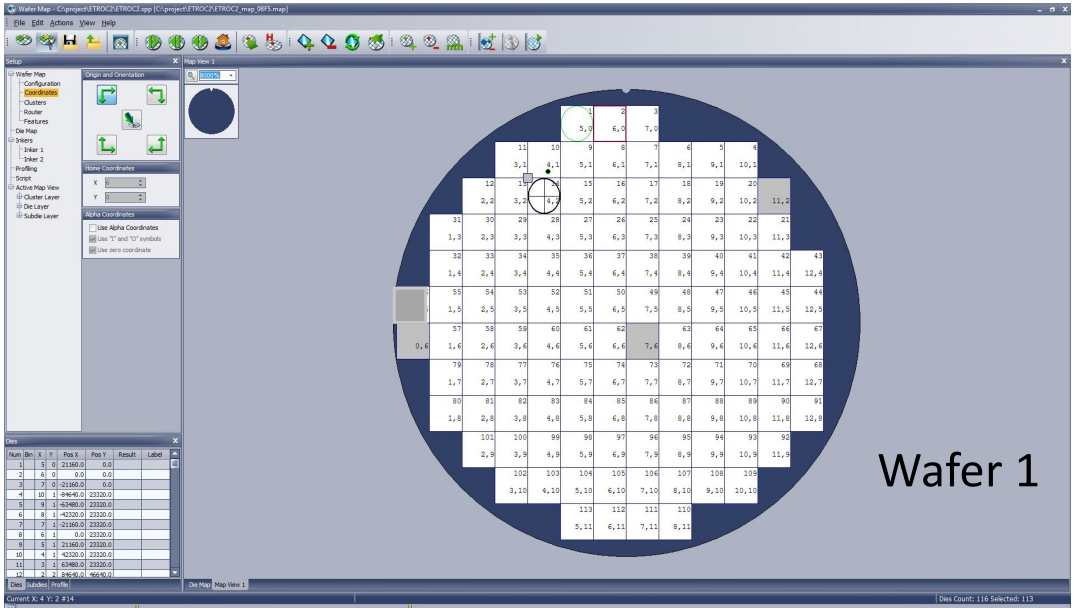
- *The solution is connecting the shielding structures to the digital ground at M3*
- *As such, during production, the M3 always has a discharge path*

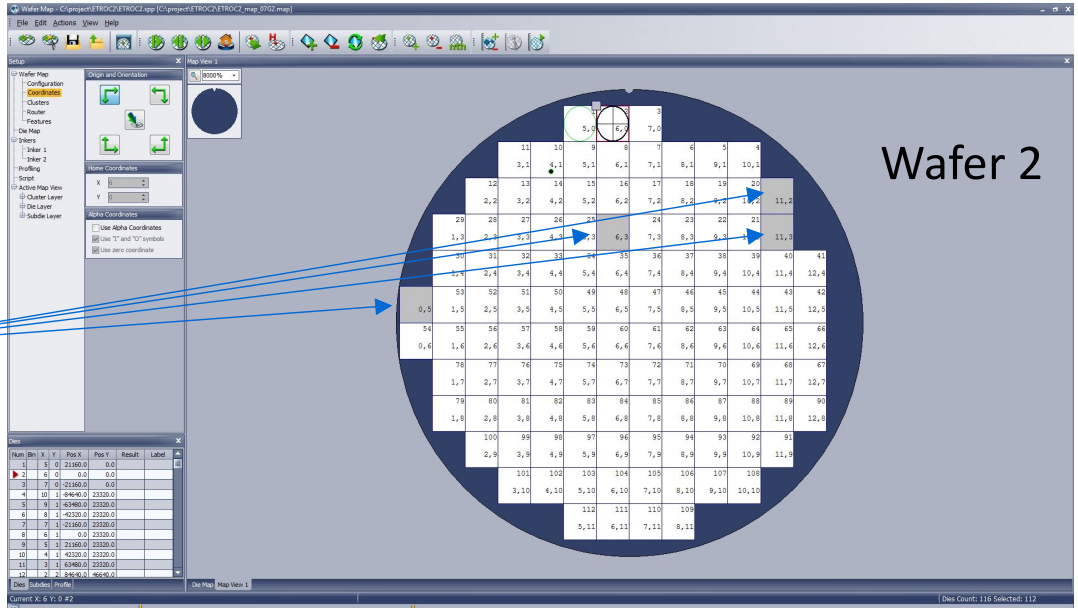
- *This simple change was made and applied to 2 wafer (out of 6) wafers on hold at TSMC*
- *The two new wafers arrived CERN in early Aug 2023, and have been wafer probe tested right away*

The ESD problem is fixed this way

Wafer probe testing for the new ETROC2 wafers







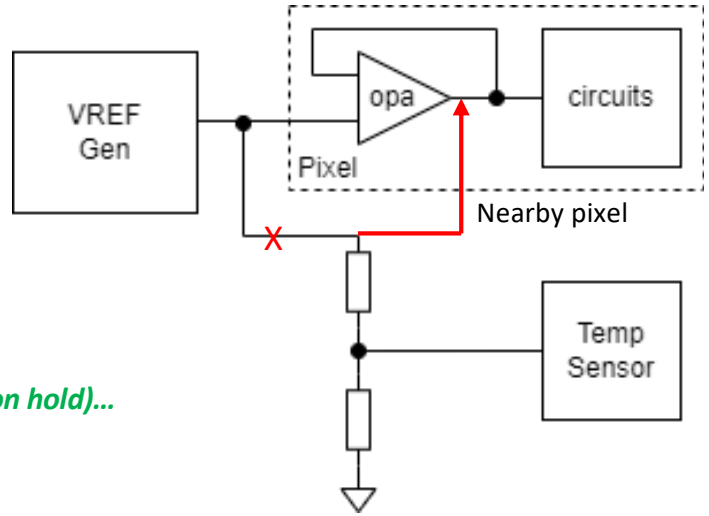
Two new ETROC2 wafers from TSMC arrived CERN in Aug 2023

probe testing shows ***only 4 bad dies (out of 116 dies) per wafer in each case***

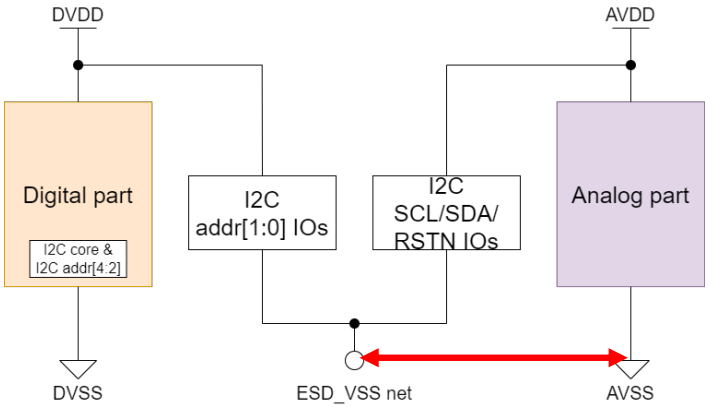
Production QC procedure developed and established for wafer probe testing.

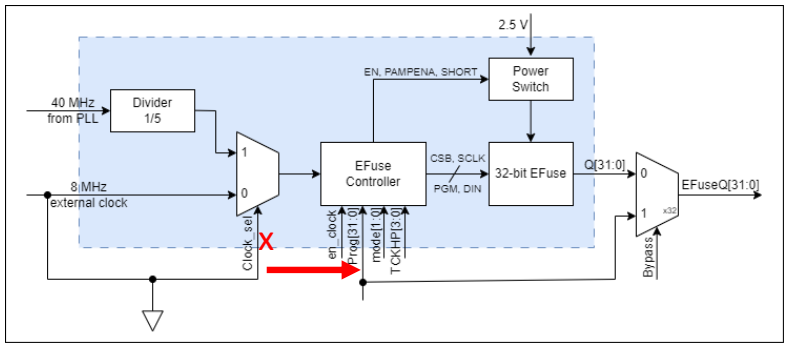
ETROC2 known issues: three minor modifications at metal layers

1) Disconnecting the VREF of TS (Temp Sensor).
2) Connecting floating ground net in WS.
3) Change the clock selection for Efuse.



The above three are the known minor issues identified during ETROC2 testing so far. ***These modifications have been implemented, submission on going this week (for next 2 wafers on hold)…***





These mods need to be fully tested to guide ETROC3

Summary: ETROC2 towards ETROC3

- ***The ETROC2 design is full size, full functionality***
  - ***Fully functional with time resolution of ~10ps*** using charge/laser injection
  - ***Has passed 200 MRad TID test*** (spec is 100 MRad), works with voltage (1.3V to 1.0V) vs temperature (-30C to +30C) for analog and digital power supplies, before and after TID.
  - ***The performance of the bump bonded ETROC2 is as expected***
  - *ETROC2 has been tested successfully with the module and readout and power board prototypes together with the back-end electronics, with charge injection and laser (by system designers)*
  - ***All known issues are minor and can be fixed with wafers on hold***

- ***Towards ETROC3:***
  - ***Chips level: more testing on going (laser/beam followed by SEU)***
    - ***DESY beam during Dec 4-23, 2023, with more planned later***
    - ***SEU study/testing scheduled in Jan and April/June 2024, in collaboration with KU Leuven***
  - ***System level: more system level testing on going (laser/source/beam)***

ETROC Team (current, as of Dec 2023)

- ETROC2/3 testing (chip and wafer level): mostly from ETROC0/1 team + new people
  - FNAL:
    - Physicists: Murtaza Safdari (postdoc), Ted Liu
    - Engineers: Datao Gong, Jinyuan Wu, Jamieson Olsen, Sergey Los
  - UIC:
    - Jongho Lee, (Zhenyu Ye, now LBNL), Grigory Nigmatkulov, Enea Prifti, Austin Baty, Olga Evdokimov, Zhengwei Xue
  - UCSB engineer:
    - Xing Huang
  - SMU Engineers:
    - Kent Liu, Kevin Wang
  - SMU EE PhD students (thesis work on ETROC waveform sampler):
    - Xianshan Wen, Tao Fu, supervised by Prof. Ping Gui
  - Kansas: Zachary Buchanan Flowers, Chris Rogan
  - Lisbon:
    - Cristovao Silva, Jonathan Hollar and Michele Gallinaro
  - IFAE (Spain):
    - Ivan Vila Alvarez, Jordi Duarte, Marcos Garcia, Andres Molina, Efren Navarrete, Javier Guarch
  - INFN Torino: Roberta Arcidiacono, Leonardo Lanteri

- ETROC3 design team: ETROC0/1/2 design team + new people
  - FNAL engineers: Datao Gong, (Quan Sun), Giuseppe Di Guglielmo (for verification)
  - UCSB engineer: Xing Huang
  - SMU EE PhD students: Xianshan Wen, Tao Fu, supervised by Prof. Ping Gui
  - LBNL: Dario Gnani and Tarun Prakash (digital implementation and verification)
  - KU Leuven: Jeffrey Prinzie's group (focus on SEU related)
  - Physicists to help with design verifications (using cocotb approach)

More groups/people have joined the ETROC project past year