EICROC
status and plans

ePiC meeting Argonne

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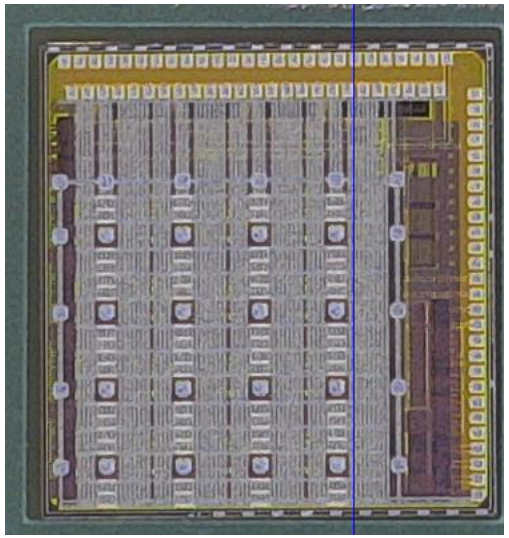
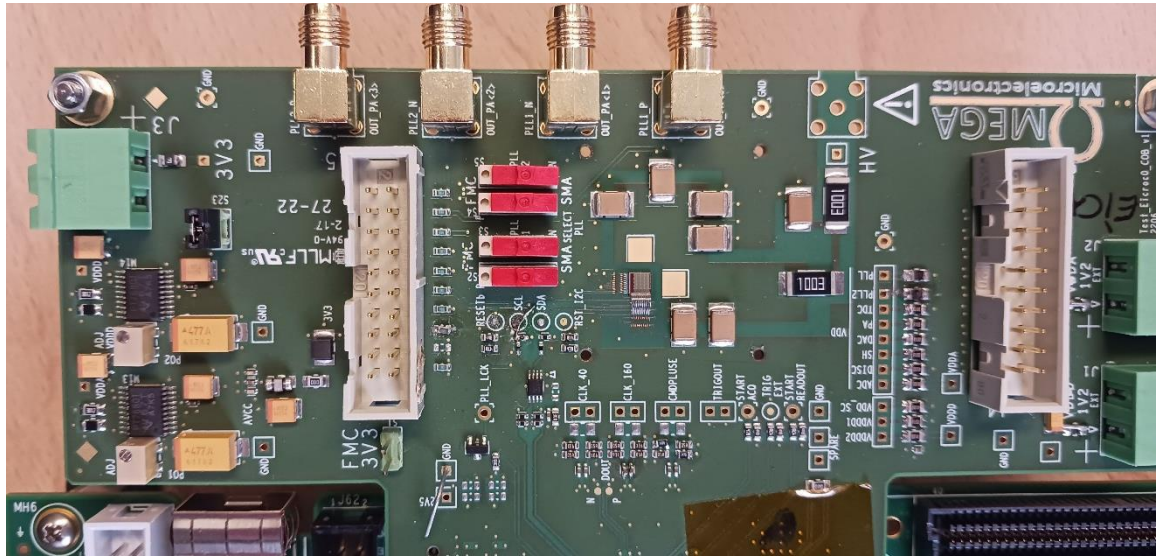
9 jan 2024

Organization for Micro-Electronics desiGn and Applications

EICROC0 overview

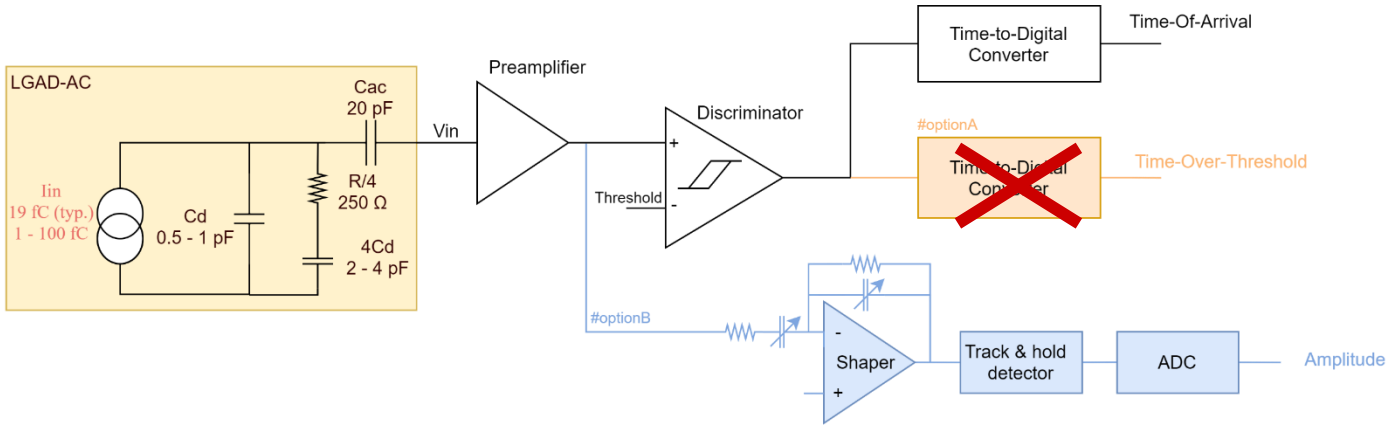
- EICROC0 is a 16-channel testchip for AC-LGADs at EIC
  - Based on ALTIROC (ATLAS HGTD) front-end and HGCROC (CMS HGCAL) ADC/TDC
  - Reads 500x500 um pixels for sensor evaluation
  - Readout designed for testbeam (not EIC)
  - Fabricated in march 2022, received beg july 2022
  - now under test at IJCLAB and OMEGA.

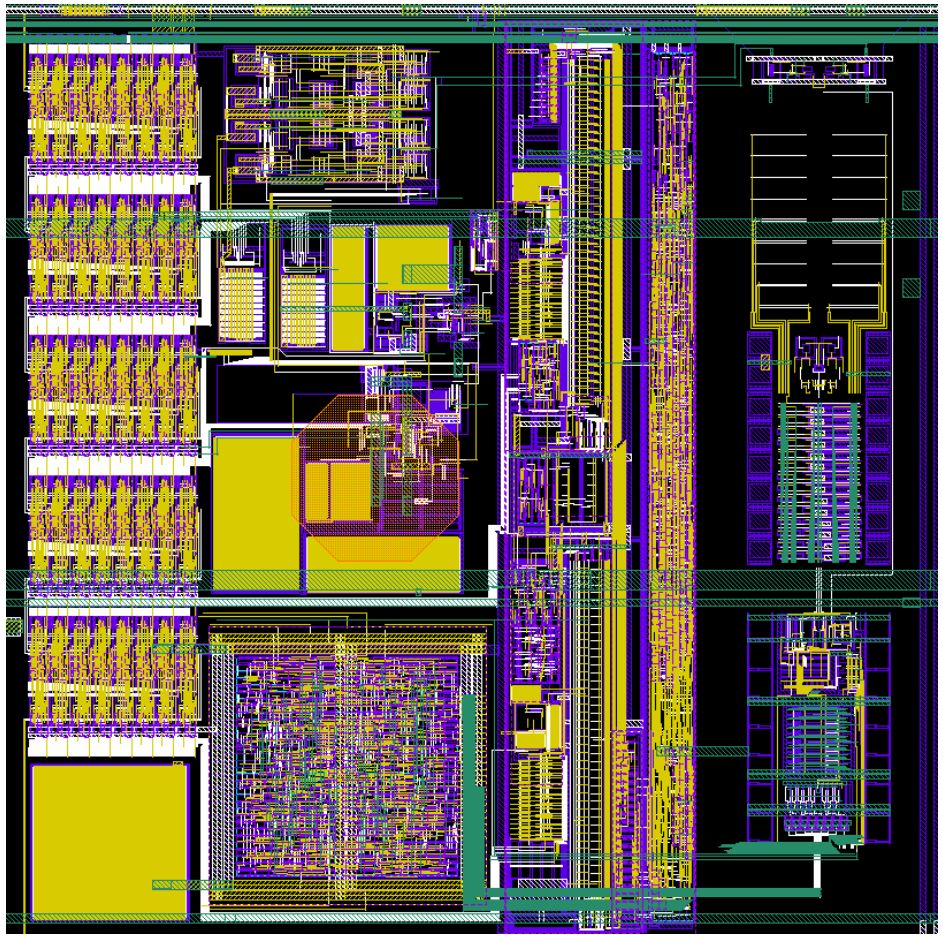




EICROC0 : one pixel overview

- One pixel design
  - Preamp, discri taken from ATLAS ALTIROC
  - I2C slow control taken from CMS HGCROC
  - TOA TDC adapted by IRFU Saclay
  - ADC adapted to 8bits by AGH Krakow
  - Digital readout : FIFO depth 8 (200 ns)
- 5 slow control bytes/pixel
  - 6 bits local threshold
  - 6 bits ADC pedestal
  - 16 TDC calibration bits
  - Various on/off and probes





Slow control | PA +discri | TOA TDC | 8b 40M ADC

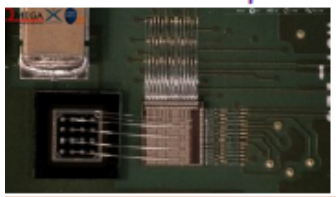
Status of EICROC0 Test Bench at IJCLab

RC2 | RC3

Preliminary studies [board w/ EICROC0, no AC-LGAD]

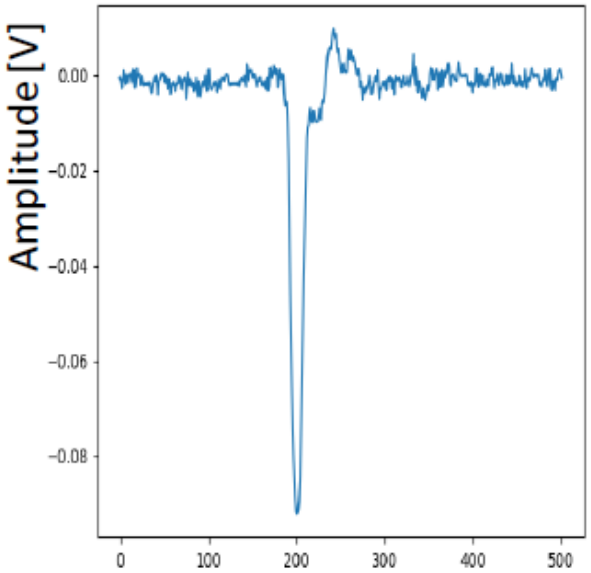
- TZ Pre Amplifier output signals
  - SNR > 70 for 12.5 fC input ; SNR > 6 for 1 fC input)
  - Jitter evaluation: < 20 ps (≥ 6 fC) ; 8 ps (25 fC)
- TDC performance (alone):
  - quantification step (~25 ps) in fair agreement with design
  - observation of a large noise coupled to 160 MHz clock
  - Time of Arrival resolution estimated to 14 ps (25 fC)
- ADC performance (alone) functional, 8-fold noise structure observed
- Evaluation of cross-talk between channels underway
- Further nvestigation of noise / clock couplings (**TDC and ADC**)

Short term plan: to evaluate performances of the existing board w/ **EICROC0 + AC-LGAD** (4 x 4)



Wire-bonding by Brookhaven National Laboratory

Typical **PA output signal** (12.5 fC input)

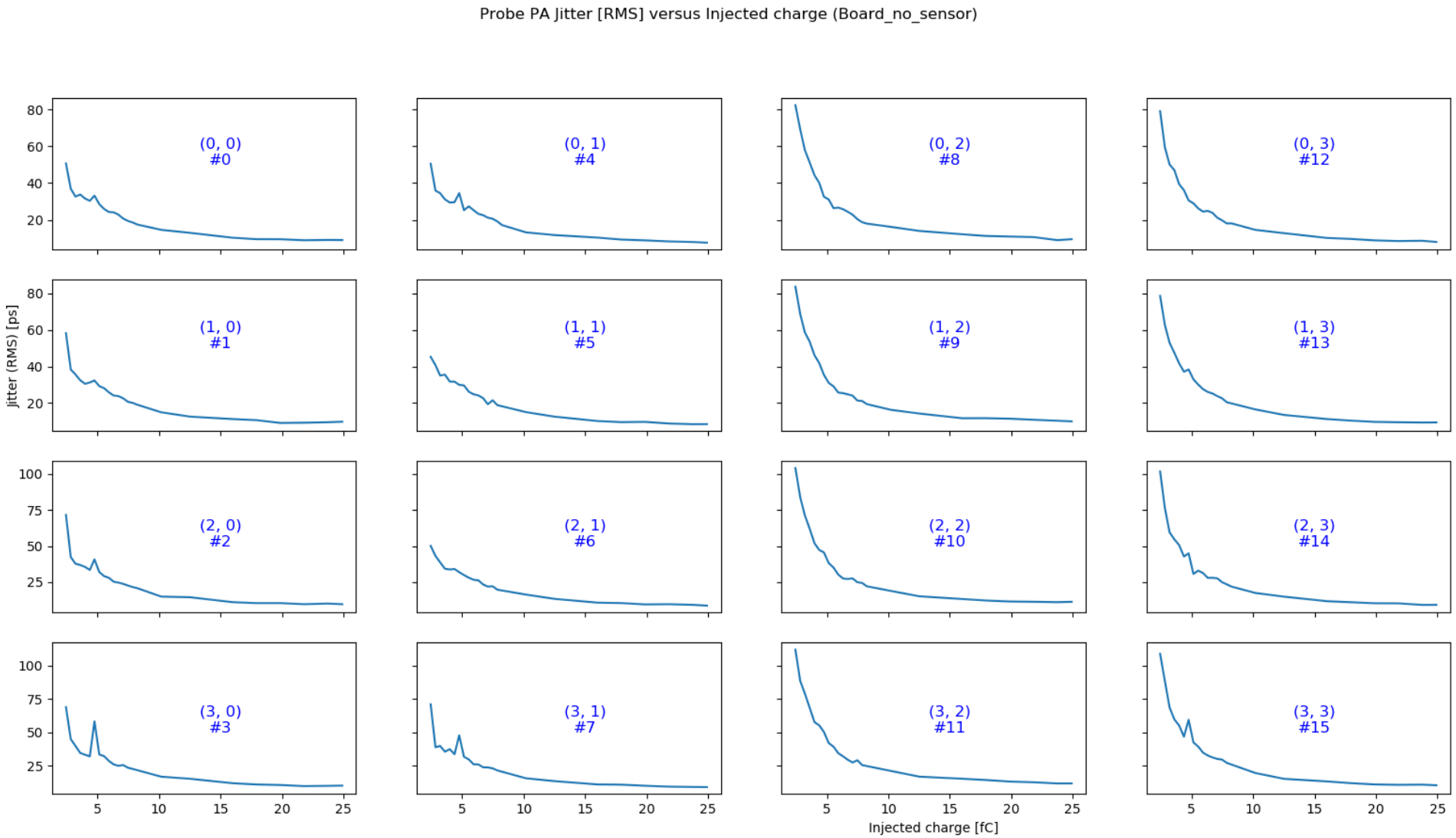


|Max. Amplitude| 95.5 mV

RMS 0.6 ns

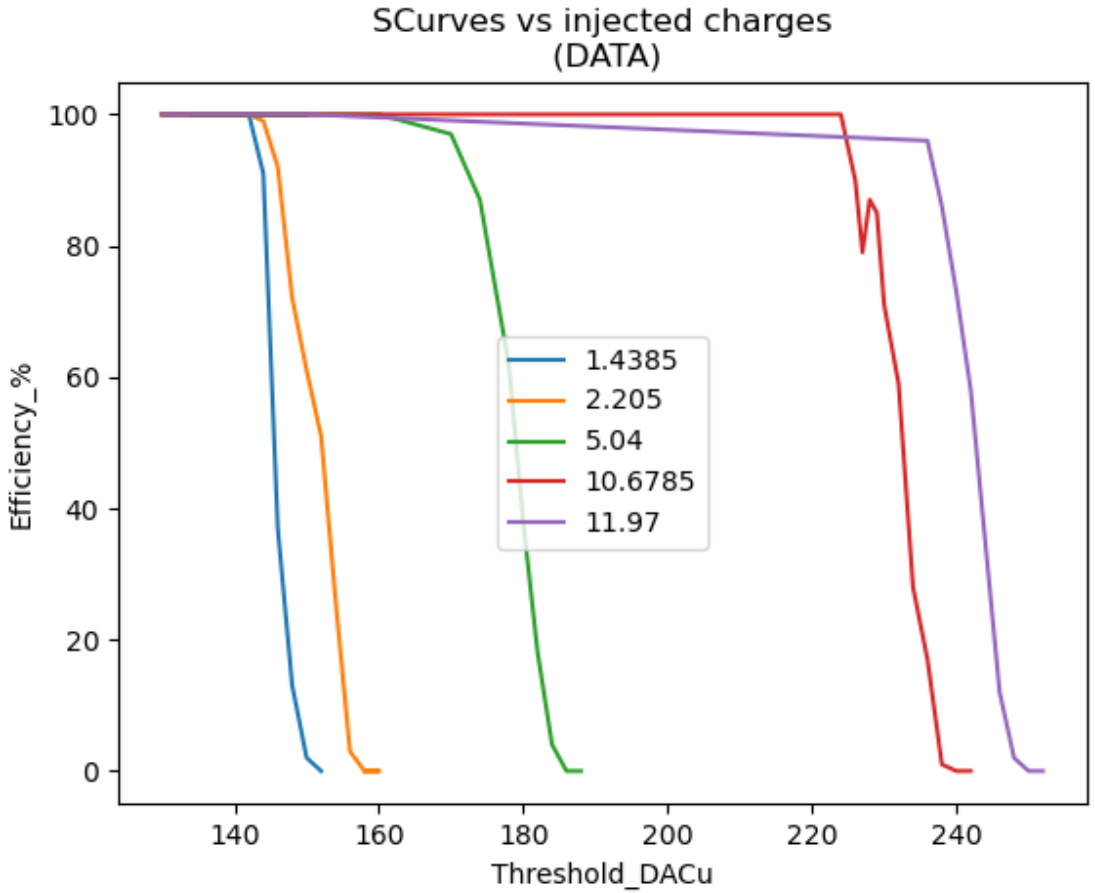
Rise (Fall) Time **0.7 ns**
computed between
10% and 90% of |Max. Ampl.|

Jitter on analog probe_pa output (clocks off) [Dominique]



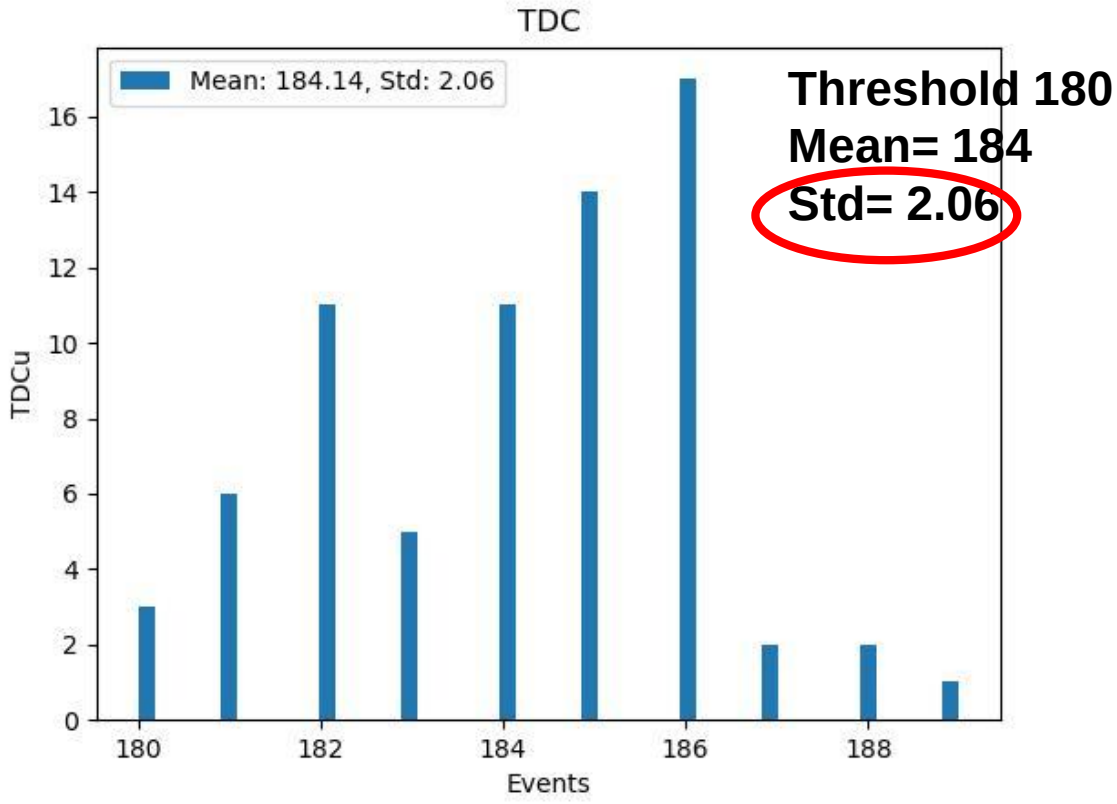
Trigger efficiency [Selma, Adrien]

- Measurements with DAQ (clocks on)
- Minimum threshold ~ 2 fC
- Noise from s-curve ~0.2 fC
- Better from what is observed with analog probe (~10fC clock noise)
  - Probe picks up clock noise

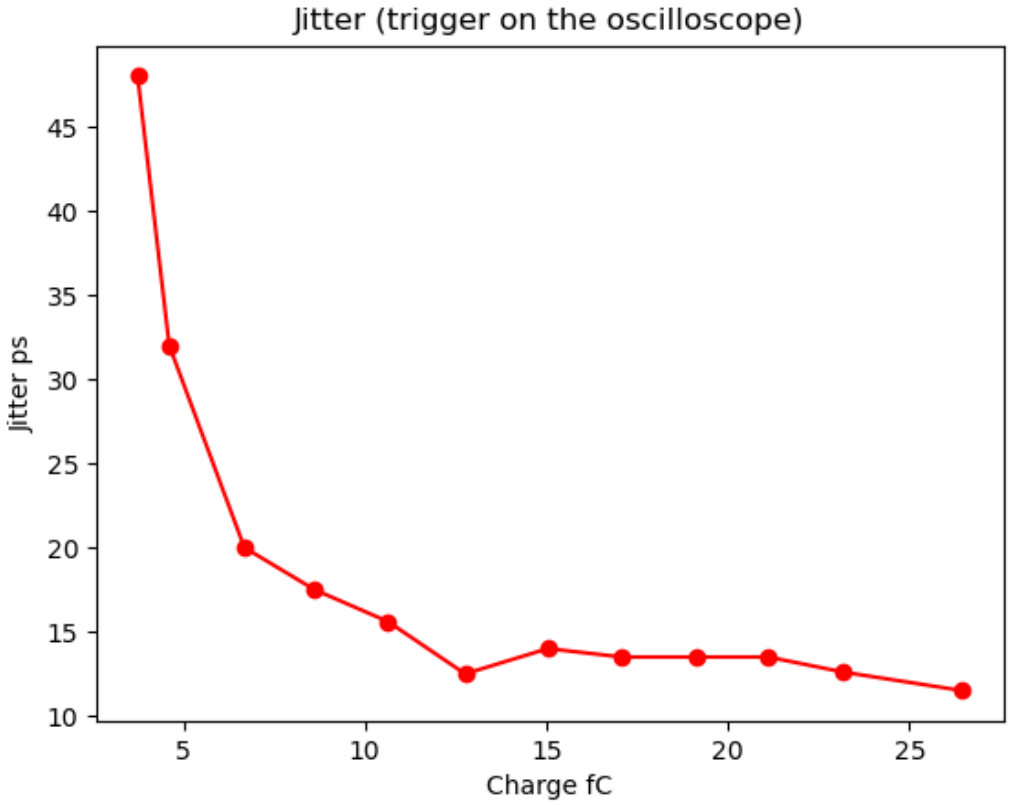


Jitter measurement [Selma, Adrien]

- Scope measurement from discriminator output : 15 ps @ 10 fC
- TDC measurements ~50 ps
  - Still large correlated noise under investigation



Threshold 180
Mean= 184
Std= 2.06



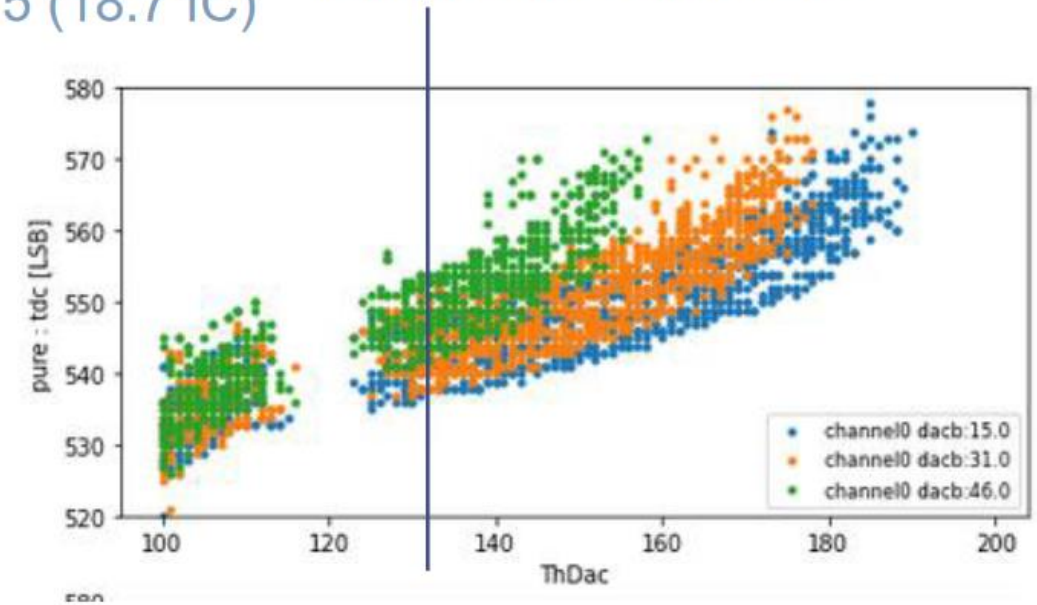
More TDC measurements [Florent]

- Threshold ~2 fC
- Noise ~3 TDCU = 75 ps

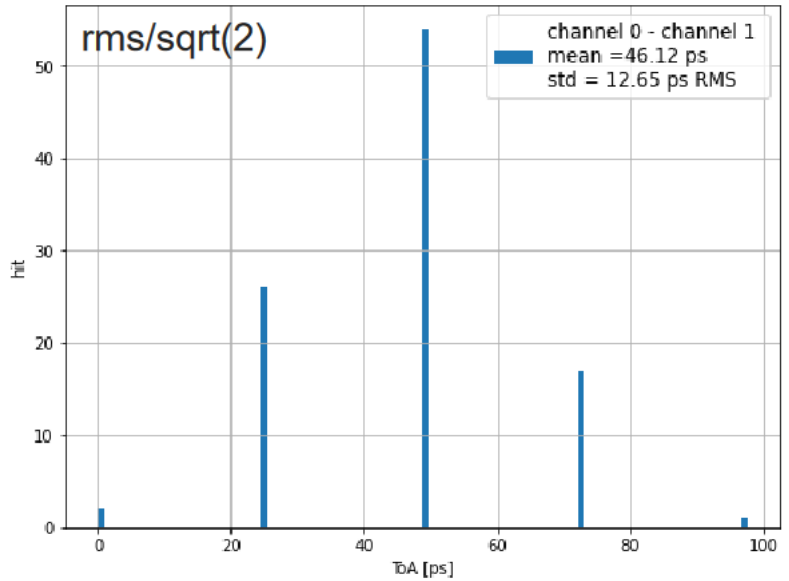
dacb_pulser :

- 46 (6.2 fC)
- 31 (12.5 fC)
- 15 (18.7 fC)

Estimated noise floor : 2 fC ?



ThDac : 130 :

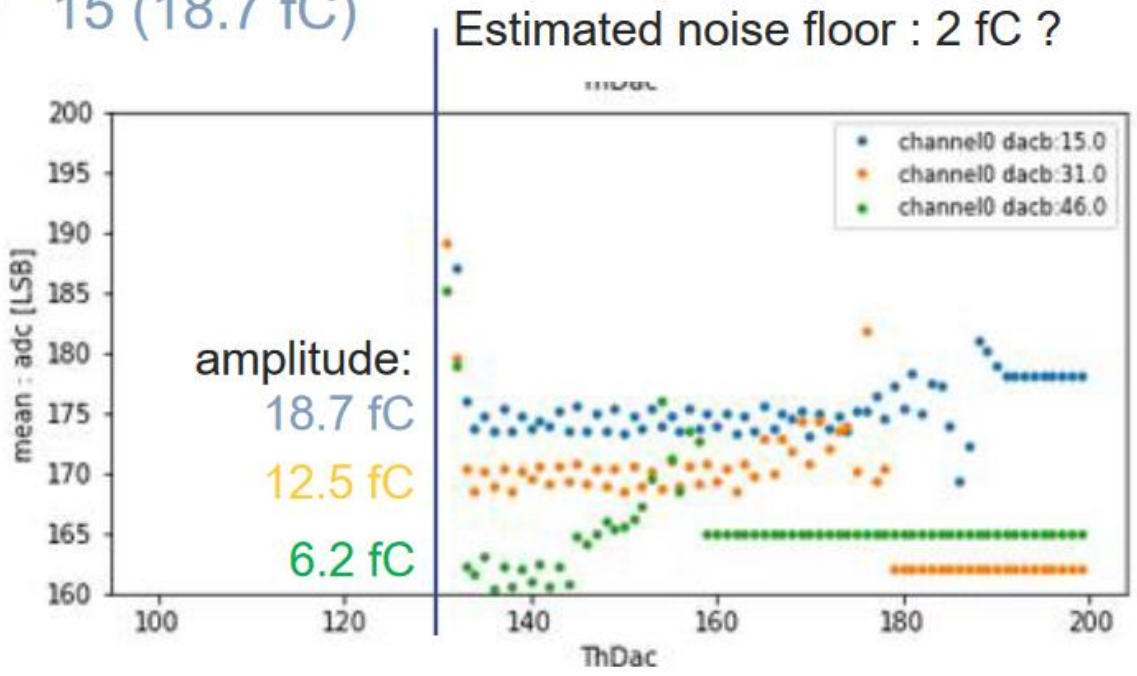


Distribution of the time difference

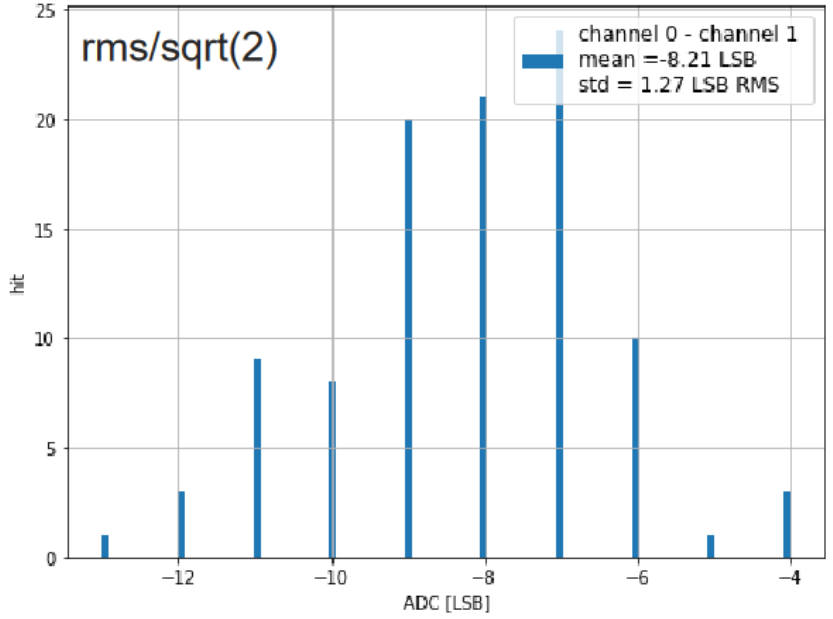
Preliminary ADC measurements [Florent, Laurent]

- ~large ADC noise (~10 UADC) under investigation
- Mostly coherent

dacb_pulser :
- 46 (6.2 fC)
- 31 (12.5 fC)
- 15 (18.7 fC)



ThDac : 150 :



Distribution

Noise near 1.2 LSB RMS

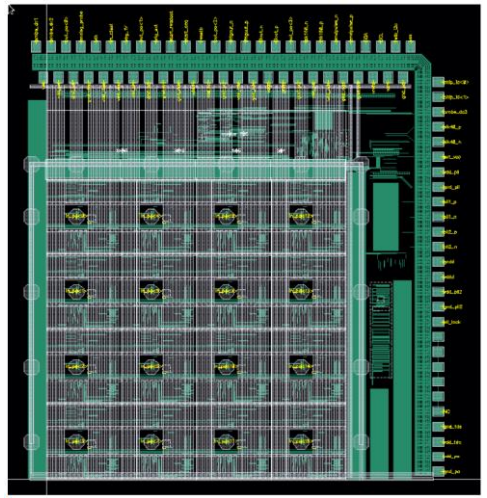
ise is removed

Evolution of EICROC

- EICROC0 is a testbeam prototype => sensor characterization
  - Triggered readout
  - all data shipped out : 16 ch * 8 samples ADC + TDC
  - Present power ~2 mW/ch + 4*20 mW « analog probe preamp »
  - ADC power + shaper/driver to be reduced from ~1 mW to 100 µW/ch => EICROC0A

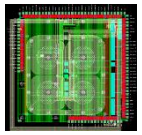
- EICROC1 will address larger dimensions 4x16 or 8x16 or 4x32
  - Address floor planning and power distribution
  - Selective readout : hit + 9 neighbouring channels

- EICROC2 final size : 32x32



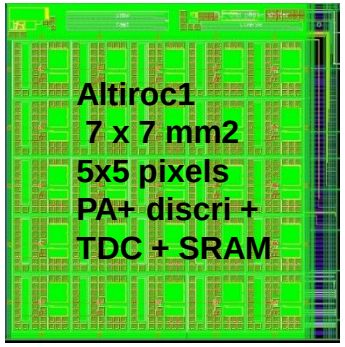
ATLAS LGAD readout : evolution of ALTIROC

2016

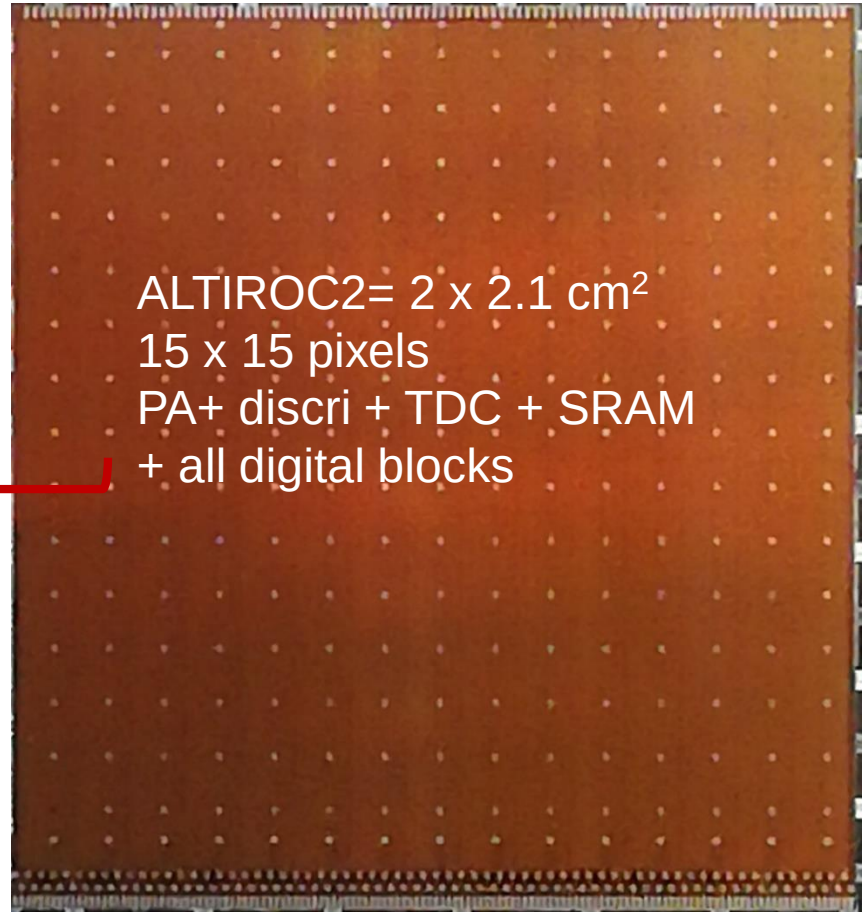


Altiroc0
2 x 2 mm2
2 x 2 pixels
PA + discri

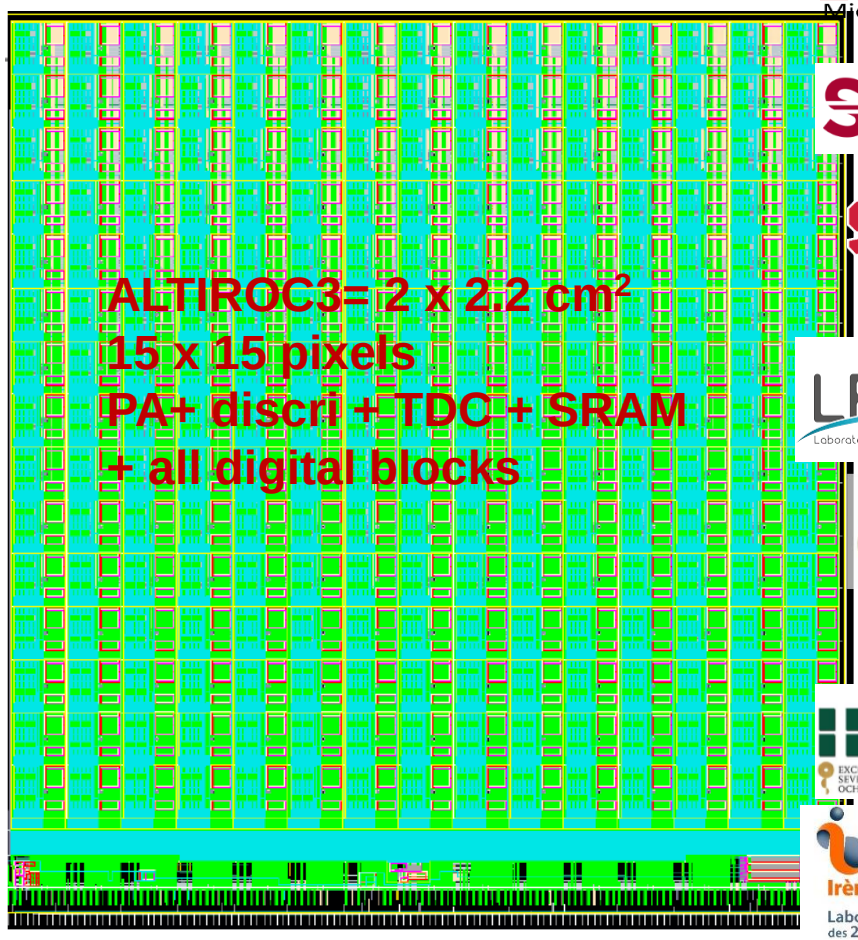
2018



2019



2021



Altiroc0 and 1:
No digital,
To validate the FE part at system level (= ASIC bump-bonded onto a sensor)

ALTIROC2:
First full size chip with 15 x 15 channels – 2 x 2 cm2
To demonstrate the functionality/performance of the ASIC (time resolution + luminosity counting) alone and bump-bonded onto a sensor
But NOT to be fully radiation hard (against SEE)

ALTIROC3:
Last full chip prototype before pre-production
Same as Altiroc2 but fully triplicated

Comparison EICROC / HGCROC

EICROC

- « 2D chip » 16 -> 1024 channels
- Input capacitance : Cd = 1-5 pF
- Dynamic range : 1 fC – 50 fC
- ToA and ADC
- Target power : 1 mW/ch
- Area 10 mm² (300 mm² final)

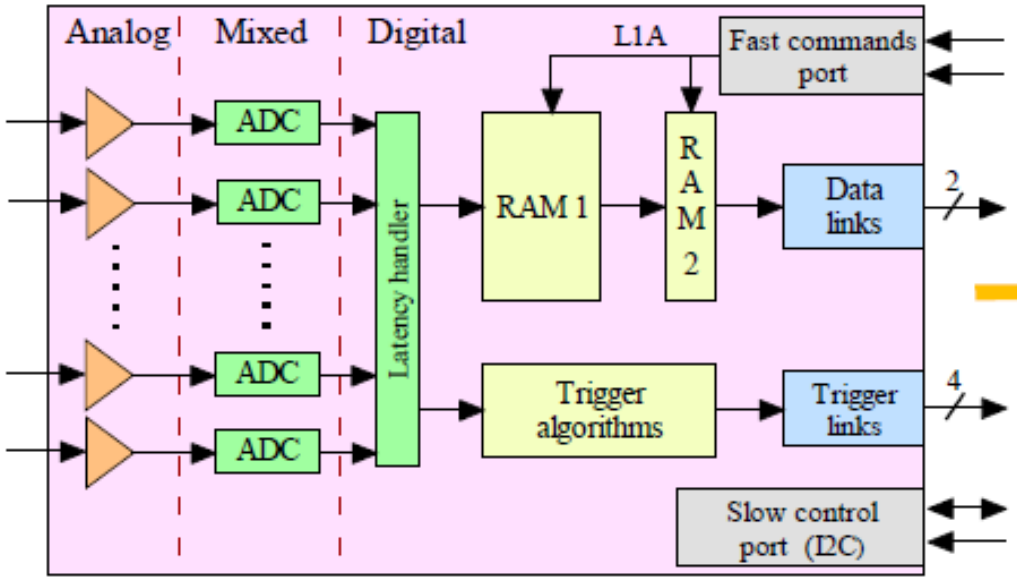
HGCROC

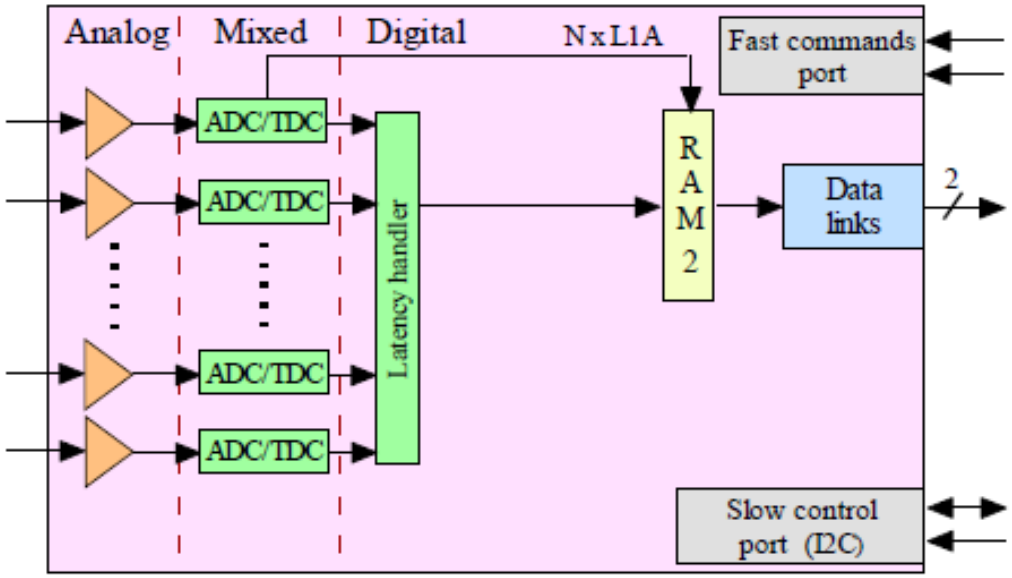
- « 1D chip » 72 (64) channels
- Input capacitance : Cd = 5-50 pF
- Dynamic range : 1 fC – 10 pC
- ToA and ToT
- Target power : 5-10 mW/ch (now 15)
- Area 100 mm²

- SiPM version H2GCROC
- Cd = 100 – 2.5 nF
- Studies for 10 nF groupings
- Can be used by EIC calo

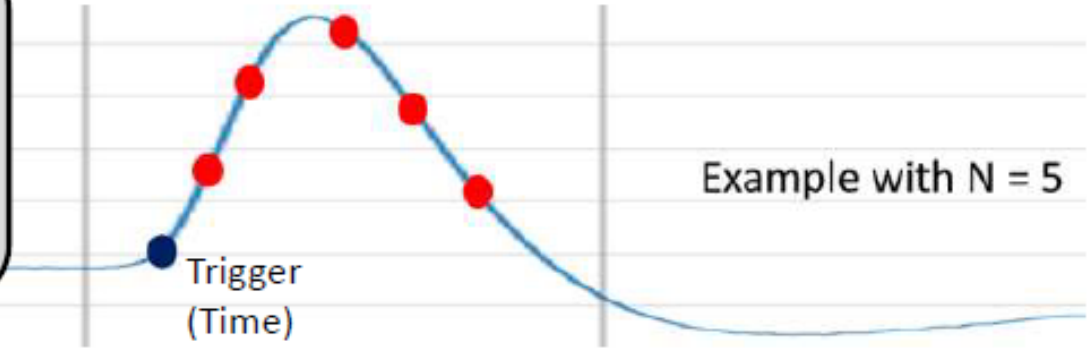
Evolution for EIC readout [Frédéric]

- Data streaming : auto-trigger and zero-suppress, 200 MHz clock
- Already done in HKROC (see backup)





- Each event passing the threshold is readout
- Auto-trigger with N "samples" (1 to 7)
- Can be exercised with present HGCROC (multiple L1A-triggers)



Evolution of H2GCROC : CALOROC1 (2024)

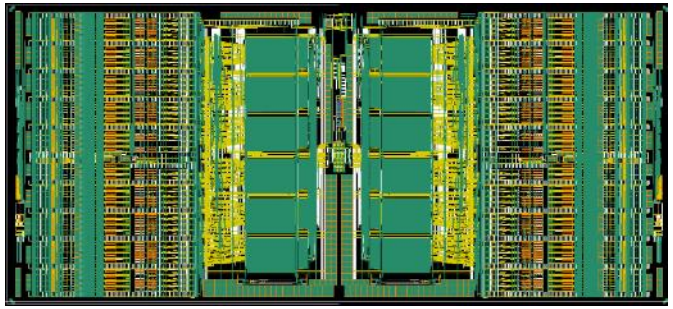
- SiPM readout calorimetry : CMS H2GCROC with EIC readout (200 MHz clock and fast commands)
  - SiPM from 500 pF to 2.5 nF (or 10 nF)
  - ~5-10 mW/channel

- 2 versions : conservative and exploratory
  - Conservative : uses H2GCROC (ADC, TOT) as it is and replaces the backend
  - Exploratory : new analog part (dynamic gain switching).
  - Pin to pin compatible
  - Backend « à la HKROC » : auto-triggered, zero-suppressed
  - 40 MHz internal clocking (ADC, TDCs)

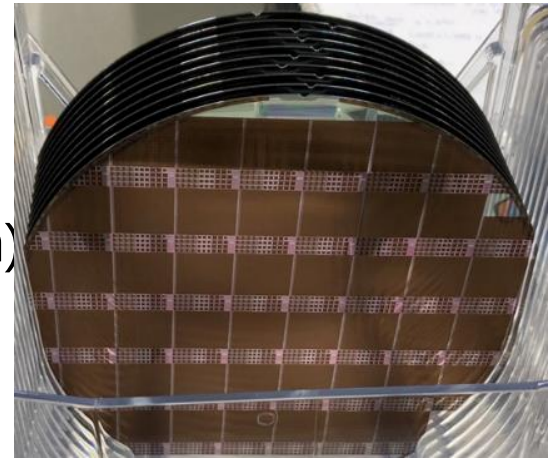
- Channel number tbd : 32 (HKROC) or 64 (HGCROC)
  - Cost issue and pin/pin compatibility with prototypes

- « Si » version considered for HRPPD and/or strips

HKROC

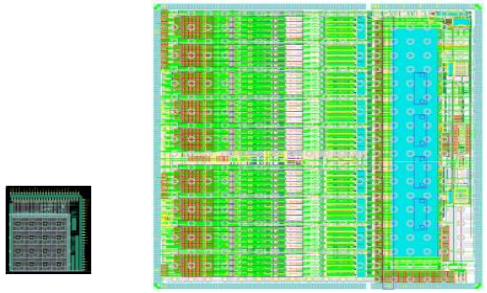


Plans for 2024

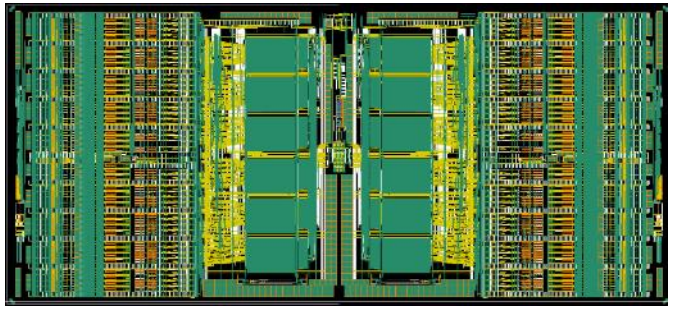


- CALOROC = H2GCROC (SiPM) for EIC
  - Analog part = H2GCROC, backend EIC specific
  - Need to choose HGCROC pin-pin compatibility (64 ch) or HKROC size (32ch)
  - 2 versions : conservative (ADC/ToT), improved (multi-gain)
  - Cost in MPW : 2 * (50 or 100 mm²) * 2 k€ > Engineering run = 250 k€
  - Mid/fall 2024 tbd

HKROC

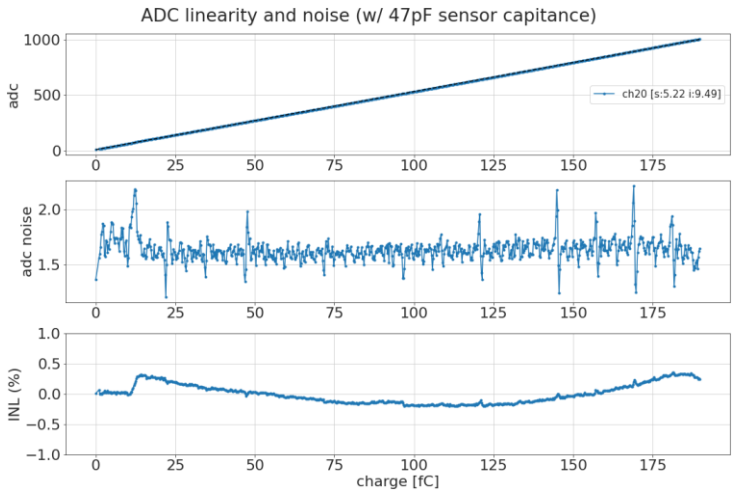


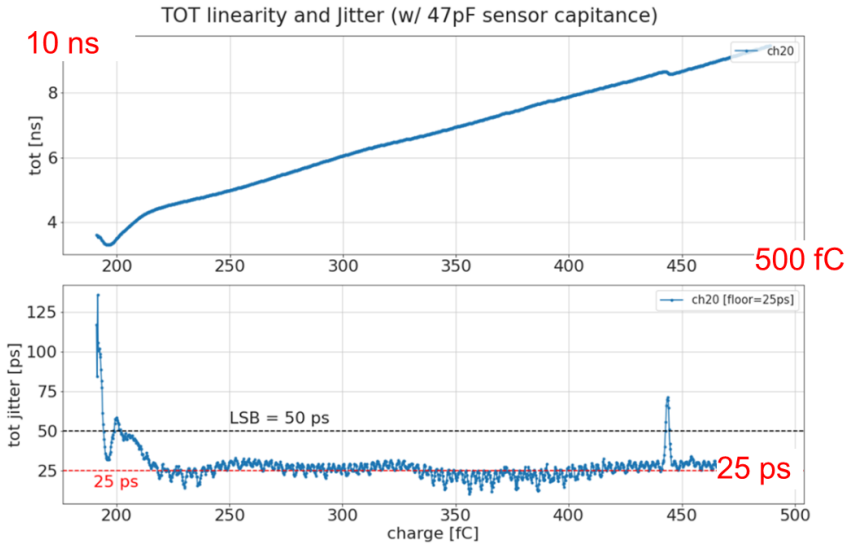
- EICROC
  - Possibly EICROC0A with improved digital noise and low power ADC
  - EICROC1 (4 or 8)*16 channels with possible column « flavours »
  - Probably not yet with EIC readout
  - Area : 20 - 35 mm²
  - Mid/fall 2024 especially if Engineering Run chosen

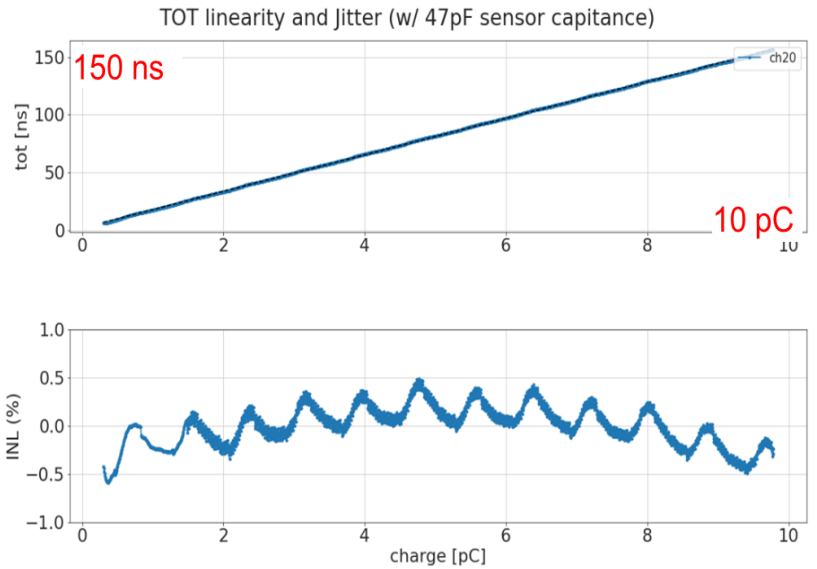


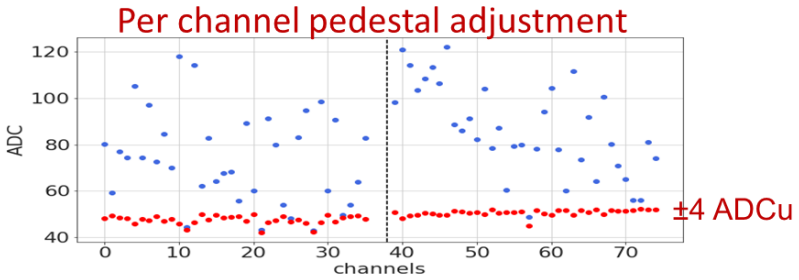
backup

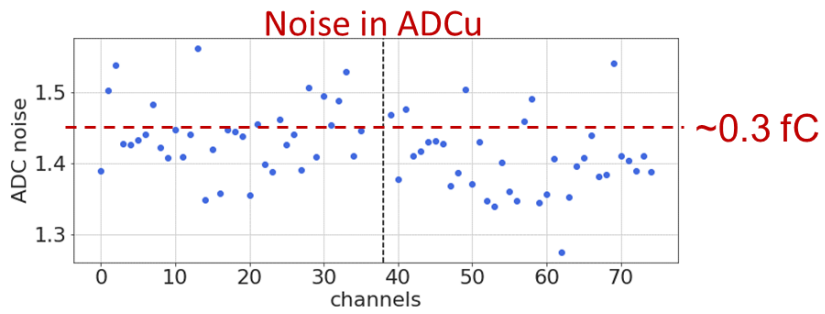
HGCROC3 performance

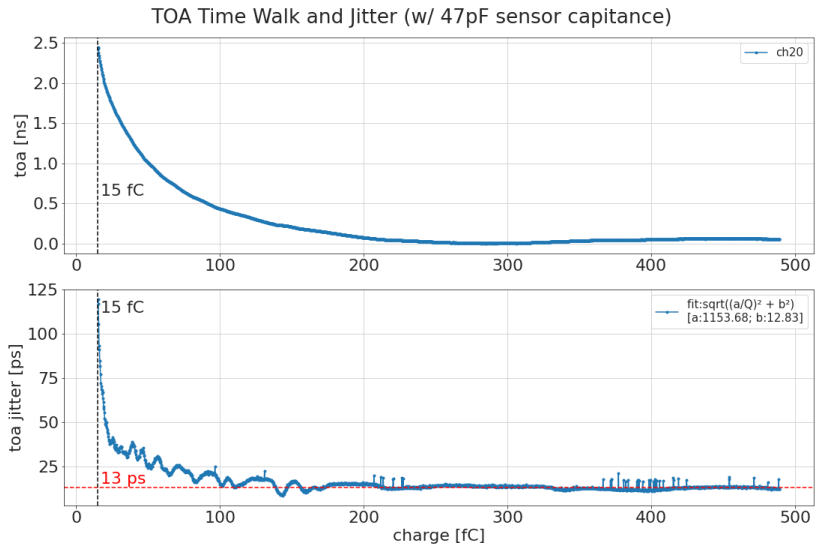






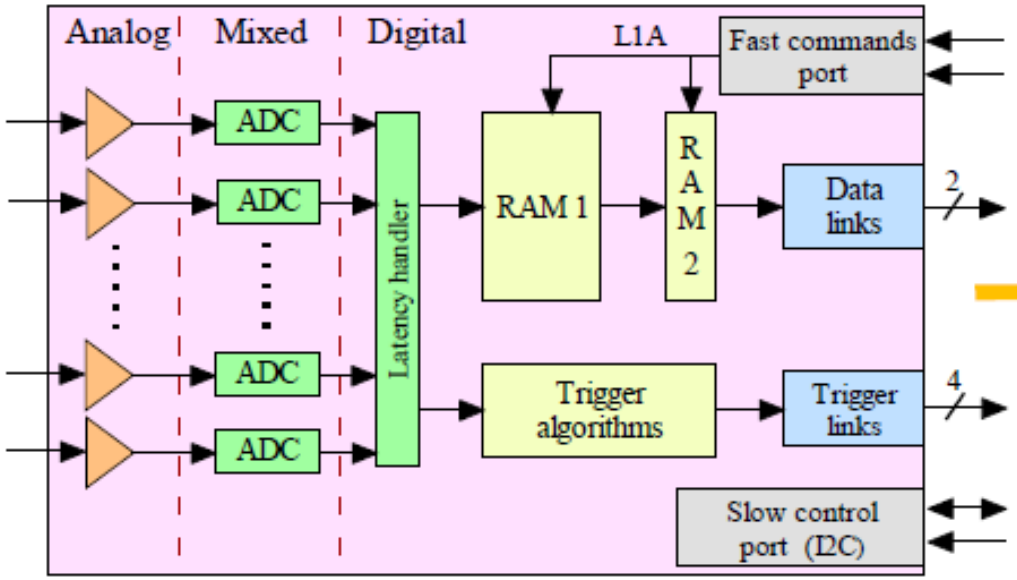


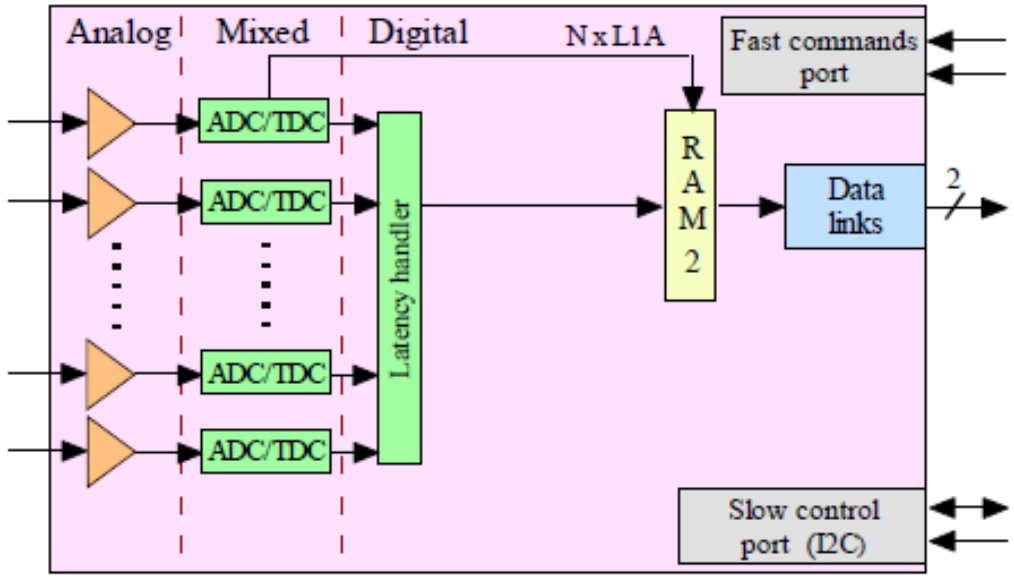




Evolution for EIC readout [F. Dulucq]

- Data streaming : auto-trigger and zero-suppress





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- Can be exercised with present HGCROC (multiple L1A-triggers)