OAK RIDGE National Laboratory

# Kapton Flex Hybrid R&D Update

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U.S. DEPARTMENT OF ENERGY

# Barrel TOF Flex PCB

- Connect 64 ASICs (+X) along stave to RDO at end of stave
  - Low voltage, bias (HV), ground
  - Differential e-links, **clocks**, slowcontrol/$I^2C$?
  - Individual ASIC output data rate is only ~Mbit/s (based on Tonko's initial estimates)
- Low mass: 1% $X/X_0$ total barrel material budget
- Needs to fit barrel TOF geometry
  - ~1.3m length
- Kapton flex PCB:
  - Custom geometry "sandwich" of thin kapton and conductor layers
  - Used in other tracking detectors already

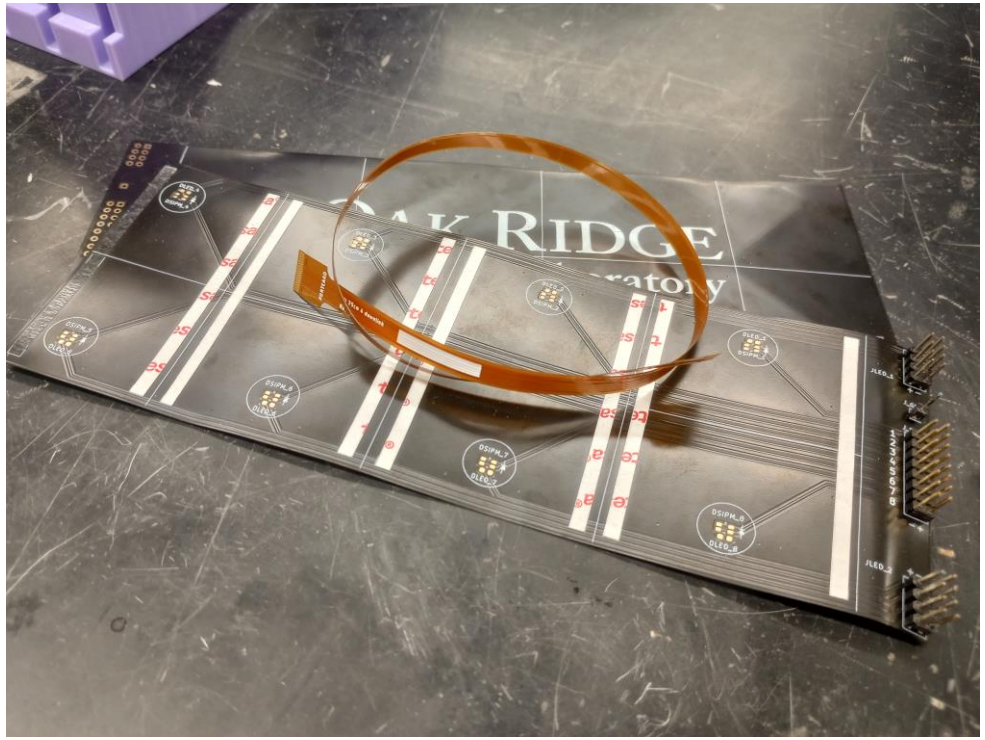
| | | | | | | |
|---|---|---|---|---|---|---|
| PID-TOF | 3M-50M | 240-500 | 6Gb/sec | 12 | EICROC / AC-LGAD | Channel / Fiber counts depend on sensor geometry. Considering pitches of: .5mm x 1cm, .5mm x .3cm, .5mm x .5mm |

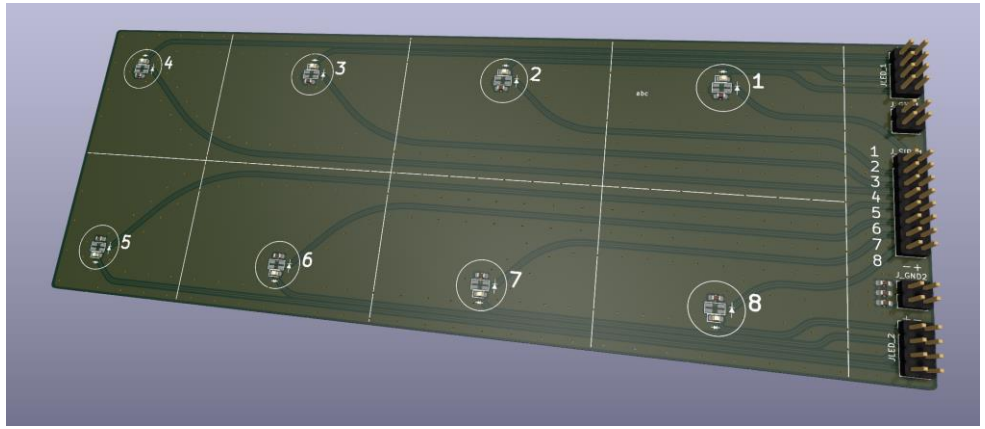
# Update

- Found capable engineering support at University of Debrecen
  - Payment figured out
  - Looking into connectors etc, but also working on LFHCAL prototype electronics…
- In the meantime: produced flex PCBs with different vendors by ourselves
  - Evaluated LV, HV characteristics (very simple…)
- Alice Bean (Kansas U.) was on sabbatical in ORNL RNP group
  - Experience with long flex lines for ATLAS pixel upgrades
  - Got a some prototypes and direct contact to their

# LFHCAL Flex PCB

- ePIC LFHCAL uses Kapton flex to gather SiPM signals per layer
  - Different geometry then TOF flex, but same technology and similar conductor layout
- Designed two revisions ourselves
  - Worked well in testbeams
- Different vendor than previous prototypes
  - Fast production,  good quality, more detailed layup options etc.
- Learned a lot about vendors, process and capabilities





# Towards a Flex Prototype for the TDR

- TDR should be 70-90% design maturity.
  - We won't have a 70-90% mature ASIC.
  - The ASIC (largely) defines the actual requirements of the flex: number of conductors, e-link speed, power requirements…
- All we can really do is demonstrate we master the technology to 70-90% design maturity
  - Reading out a similar ASIC over a "long" flex with a prototype TOF RDO would be reasonable
- Tonko plans to design an TOF RDO prototype with custom connectivity: Can add whatever we need to demonstrate flex prototype

# Towards a Flex Prototype for the TDR – Open Questions

- Which ASIC?
  - EICROC0 seems premature, EICROC0a likely available in time, EICROC1 definitely unavailable
  - Current FCFD is analog only
  - How about ETROC? Mature, digital I/O, "real chip", have expertise within ePIC TOF
- With or without sensor?
  - Needs some clarity on interconnects, but ORNL has some eRD109 funding on that…
- Connectors:
  - E-links and LV, GNDs no real problem, especially for prototype.
  - HV connectors not so easy… no single COTS connector will do HV and LV in one enclosure

# Backup

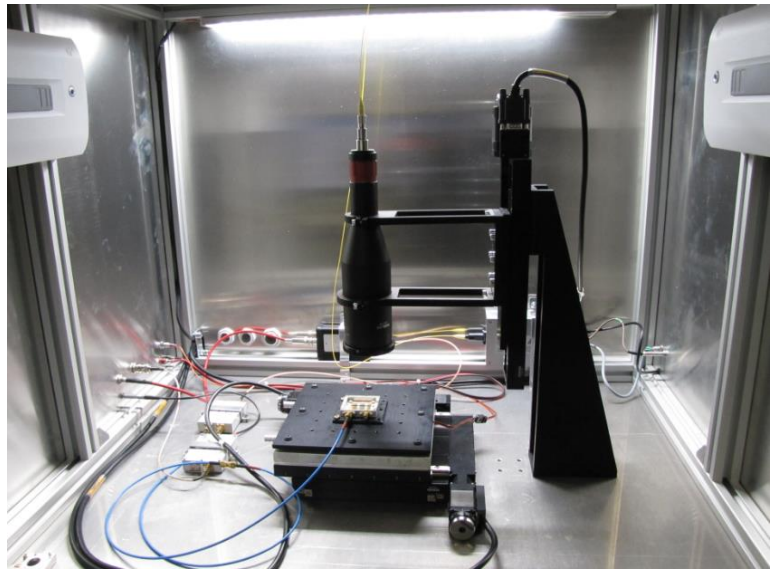
# SET FC150 precision bonder

ORNL will purchase a FC150 flip-chip bonder in FY'24 from lab funds

- Up to 150mm substrate and chip handling
- +- 1µm post-bonding accuracy
- +- 1µRad parallelism with active levelling
- Pressure up to 200 kg
- Temperature up to 400C (~1C/s)
- Can be operated in fully automated mode
- Liquid dispenser integrated in the machine for glue, underfill distribution

# Other ORNL News

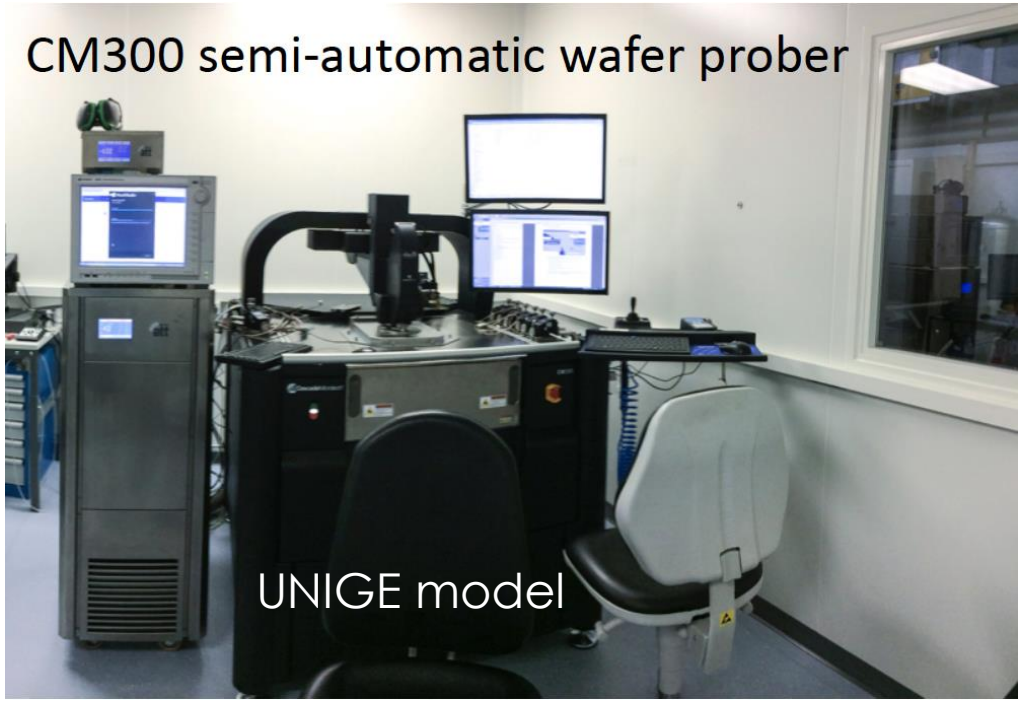
- TCT Setup finally arrived…
  - 1064nm, 550nm lasers
- New wire bonder available (*)

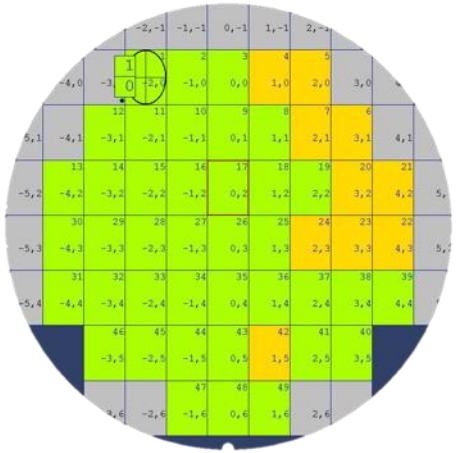


# FormFactor CM300xi probe station

We acquired a 300mm semi-automatic prober that is now installed at ORNL:

- Accommodate 5-300mm sample size
- Light tight and airtight thermal chamber
  - -60C to 125C testing range
- Probes :
  - 8 x DC probe for parametric measurement
  - 2 x RF probes
  - 1 x XYZ robotic probe with optical probing
  - Probe card holder for open, closed top probe cards
- 4 x Cameras :
  - Top view up to 1000x
  - Bottom-up view (probe alignment)
  - Side view (wafer surface alignment)
  - Auxiliary view (closed top probe card alignment)
- Fully automated alignment of wafers and dices
- Fully programmable for unattended testing



Same machine installed at University of Geneva, CERN building 14, Fermilab

# Budget Request FY'24

| Inst. | Resource | FTE (%) | Budget (k$) |
|---|---|---|---|
| | **Barrel Low-Mass Service Hybrid R&D** | | |
| ORNL | Electrical Engineering + Technician | 10 | 10 |
| ORNL | Staff Scientist | 10 | 0 (in-kind) |
| ORNL | Materials and Supplies | - | 10 |
| ORNL | Production and Bonding | - | 10 |
| ORNL | Low cost interconnect | - | 15 |
| **Total** | | | **45** |

Table 15: eRD109 Budget request for the continuation of the ORNL flexible Kapton PCB R&D in FY24, starting from December 1st 2023. All entries in thousands of dollars.

# Budget Request FY'23

| Inst. | Personnel | | Budget (k$) |
|---|---|---|---|
| | **Readout and Timing Distribution R&D** | | |
| BNL | Electrical Engineer | | 38 |
| BNL | Staff Scientist | 2x0.2 FTE | 0 (in-kind) |
| BNL | Xilinx Dev. Kit | | 4 |
| BNL | Timing Chips + Boards | | 15 |
| BNL | Travel Support | | 5 |
| | **Barrel Service Hybrid R&D** | | |
| ORNL | Electrical Engineer | | 32 |
| ORNL | Staff Scientist | 0.1 FTE | 0 (in-kind) |
| ORNL | Materials and Supplies | | 8 |
| ORNL | Xilinx Dev. Kit | | 4 |
| | **Endcap Service Hybrid R&D** | | |
| Rice | Electrical Engineer | 0.15 FTE | 18 |
| Rice | Faculty | 0.1 FTE | 0 (in-kind) |
| **Total** | | | **116** |

Table 22: Budget request for the TOF system readout electronics R&D in FY23. All entries in thousands of dollars.

# Test Structure and Measurements

- Design test prototype: As long as possible
  - Differential link loops at various lengths, geometries (?)
  - LV/HV conductors
- RF testing:
  - Confirm simulations: bandwidths, insertion losses, crosstalk
  - Test link speed/BER with FPGA/established line driver, edge jitter
  - Eventually integration into timing distribution test bench at ORNL
- DC testing:
  - Acceptable voltages, currents, resistances
- Mechanical:
  - Thermal cycling
  - Handling, bending, folding

# Simulation and Design

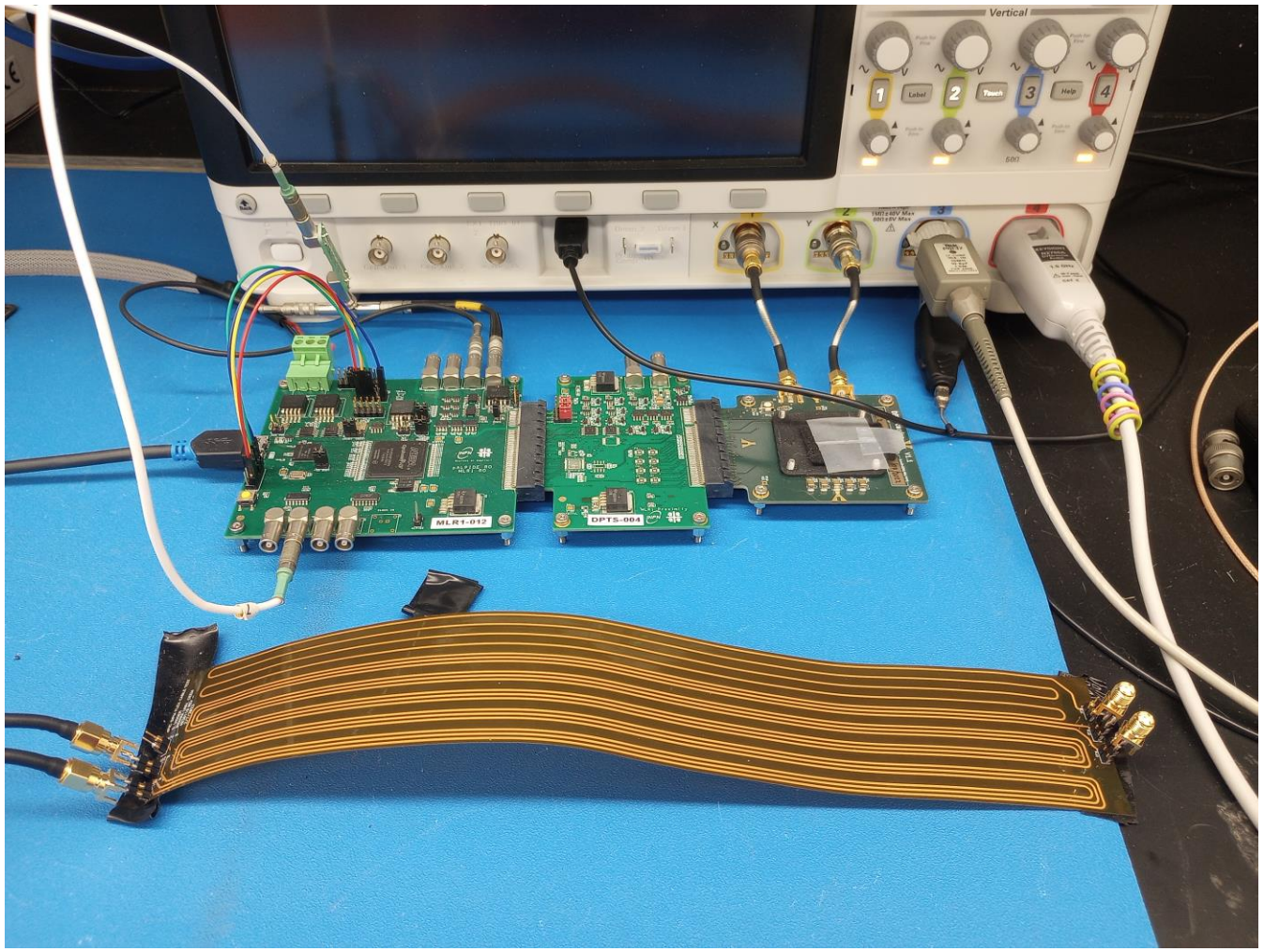
- LV/HV
  - Required material budget for current requirements
  - How much DC-DC converters for given ASIC?
  - Serial powering?
  - Design requirements for HV conductors
- Differential links:
  - Insertion losses, analog bandwidth for different lengths
  - **Crosstalk on clock line(s)!**
  - Ultimately informs output drive strength
- Common flex foil, or separate for LV/HV/RF?
- Supported by ORNL electrical engineering

# Technological Survey

- Kapton-Cu flex foils are available from various vendors
  - Cheap (~$100/3pcs), quick (3-4 weeks)
  - Can produce many prototypes for a more experimental approach
- Low mass Kapton-Al is more specialized and expensive
  - Not worth it for prototypes at this point
- Max size: 1m?
  - Depends on vendor, but can fit very long traces on moderately sized foils in any case…

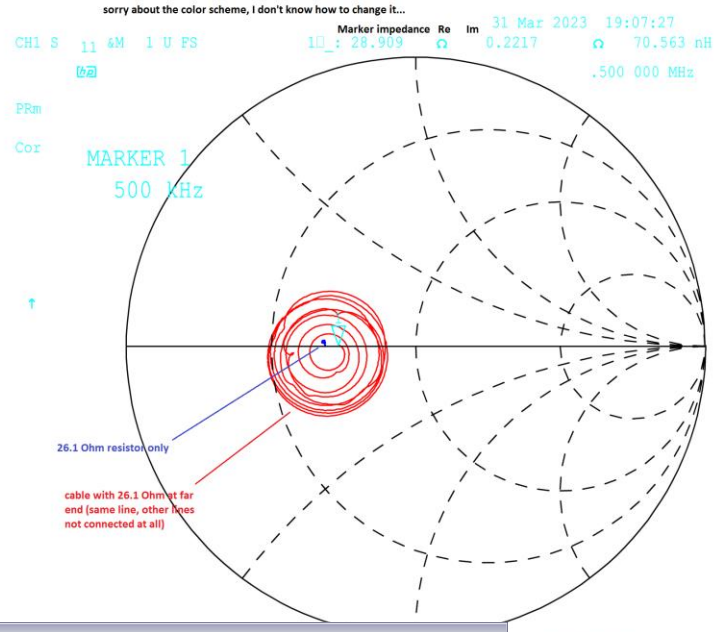
# The “Experimentalist Approach”

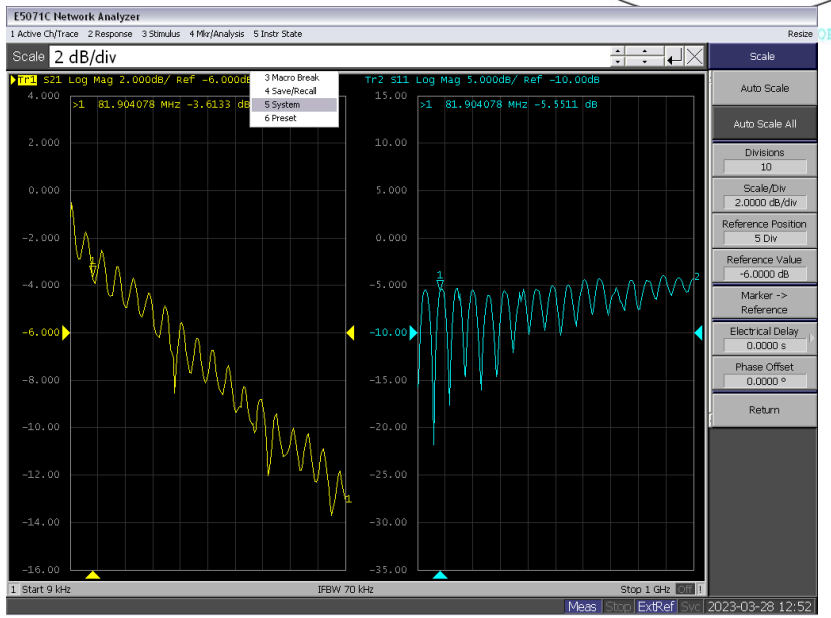
- Still identifying the right ORNL engineering resources…
- Producing cheap Cu-flex prototypes instead
  - 2x 1.5m differential pairs on 40cm flex
- Using DPTS (ITS3 test structure) CML driver as test bench driver
  - 65nm CMOS line driver
- First attempt does not yield useful data on the scope
  - Not sure if due to transmission line or connectors



# Vector Network Analyzer Measurements

- Measurements by G. Visser (Indiana) and ORNL
- Our first attempt at transmission line is not 50Ohm…
  - "Easy" fix for next attempt…



# Available Equipment

- 4ch Vector Network Analyzer – available
  - Insertion loss
  - Inter-line crosstalk
  - Need proper 50R transmission line to make sense of measurements
- Time domain reflectometer – still looking
  - Characterize impedance mismatches along length of transmission line

# DC Resistance Measurements

- 0.595Ohm along strip
  - 1.49 m length, 1mm pitch, 35um thickness
  - 2.35E-8 Ohm*m (c.f. 1.8E-8 Ohm*m for Cu)
- Inter-strip resistance
  - Could not get reliable measurement so far (capacitive effects dominate)
  - Tested up to 500V without notable leakage