ePIC Service Hybrids

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AC-LGADs Workfest@ePIC collaboration meeting
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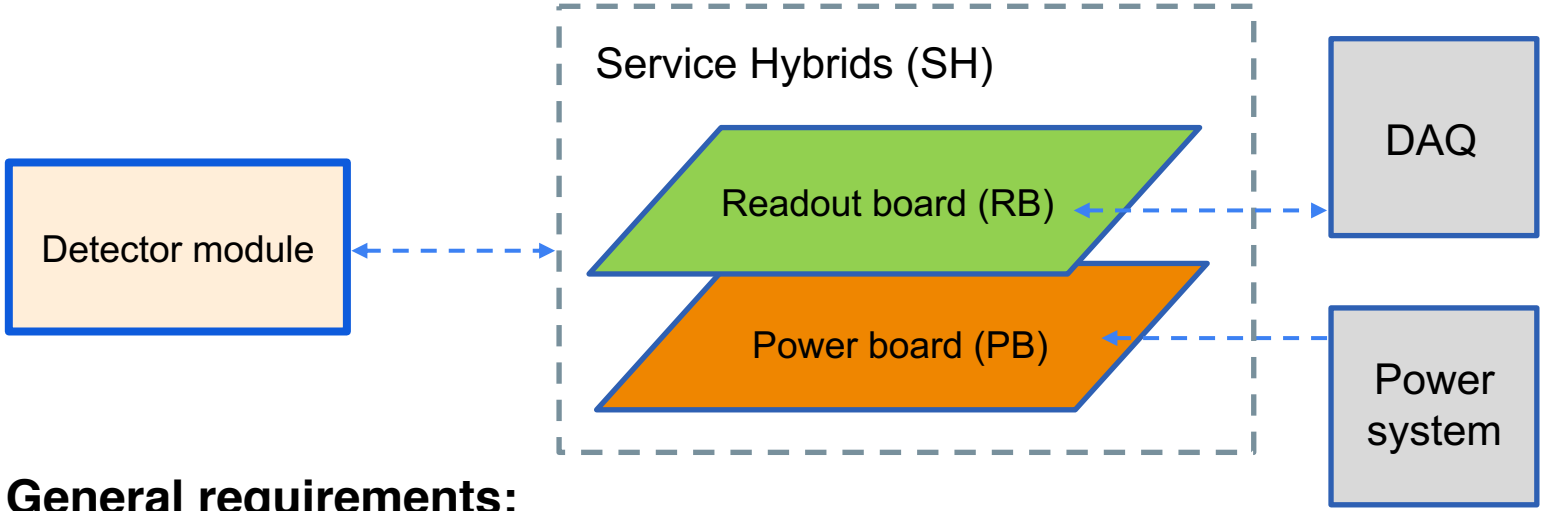
Electron-Ion Collider

BROOKHAVEN NATIONAL LABORATORY | Jefferson Lab | U.S. DEPARTMENT OF ENERGY | Office of Science

Service hybrids overview

Essential functionalities independent of BTOF or FTOF



General requirements:

- Magnetic field tolerant up to ~2T.
- Radiation tolerant over the EIC lifetime (up to 100 krad)
- Low power consumption.
- As small as possible to fit within the space limitation of BTOF and FTOF
- As little material as possible (low weight, not too much metal).

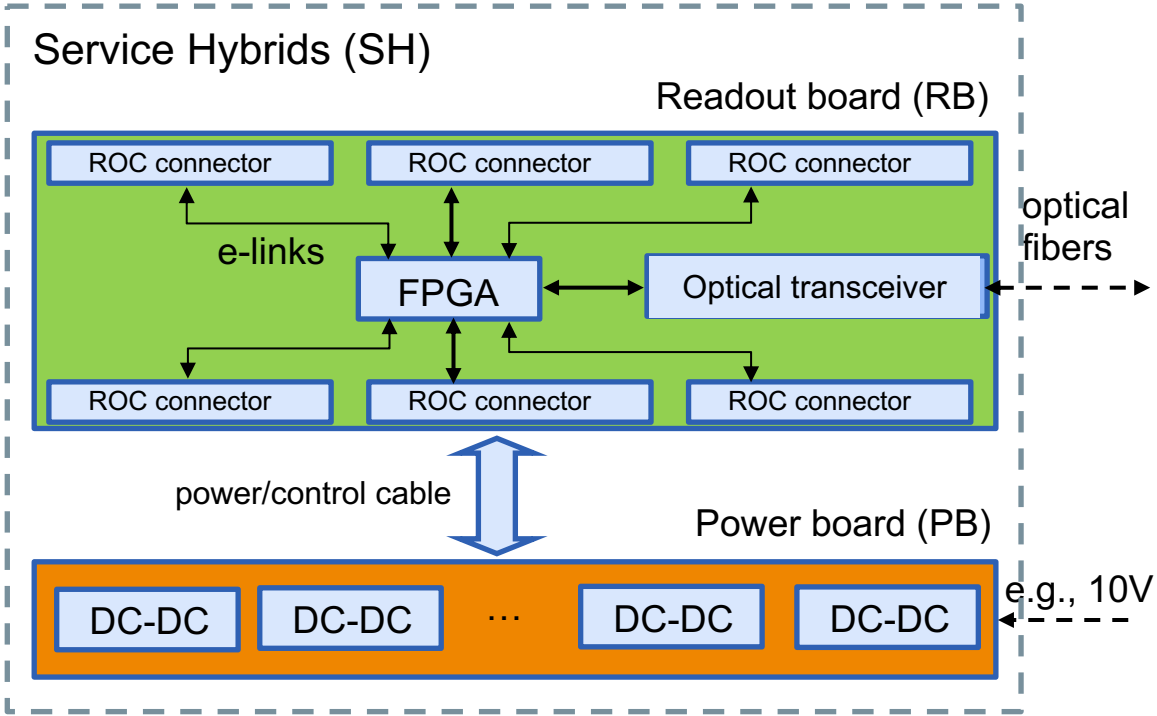
Service hybrids overview

Readout board:

- Aggregate data of up to ~16 ROCs and transmit them to the DAQ via optical links
- Slow control and monitor
- Clock distribution

Power board:

- Converts LVPS to lower voltages for powering ROCs, FPGA, etc.
- Connection to HVPS (may also be on the RB)



Service Hybrids R&D plan (eRD109)

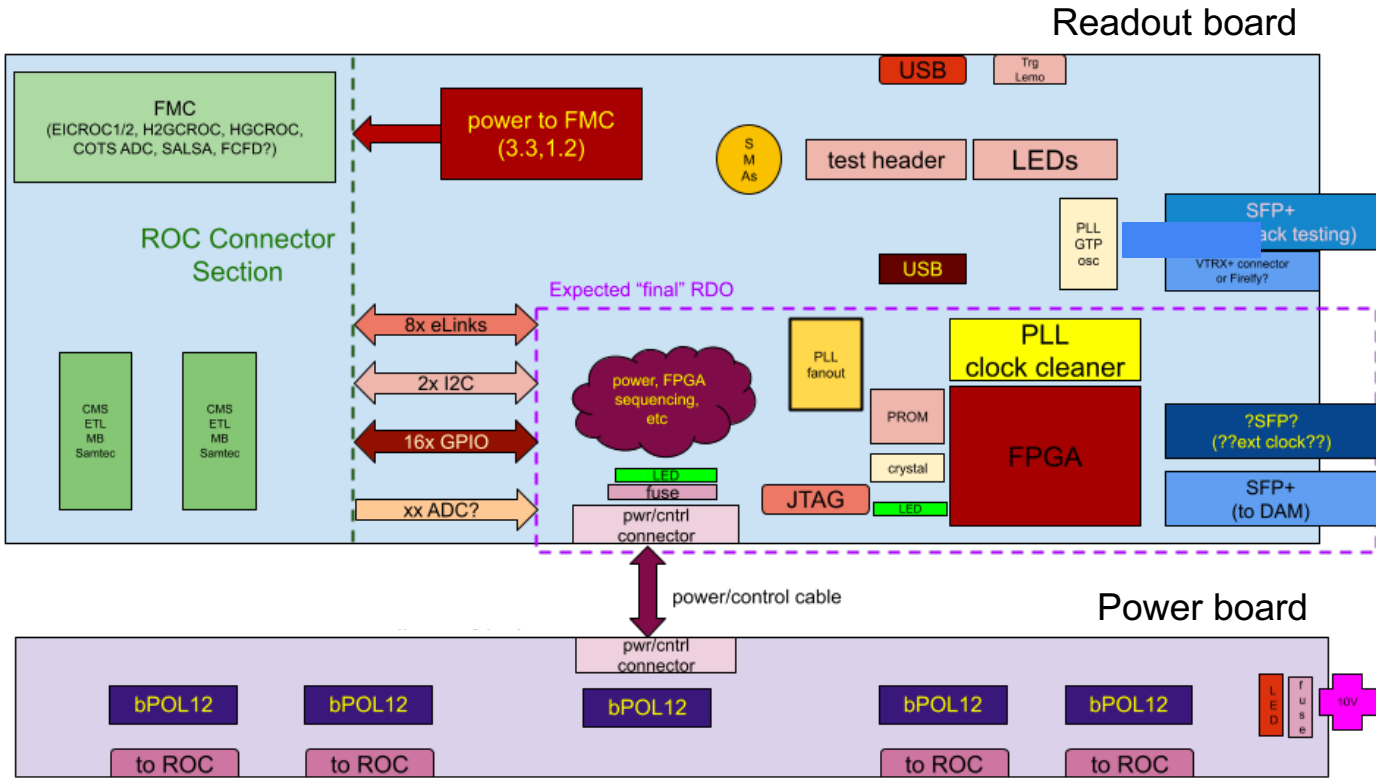
Main goals in FY24:

- Design and build a first generic prototype of service hybrids
- Demonstrate the readout chain from EICROC->SH->DAQ (Xilinx KCU105)
- Demonstrate precision clock distribution

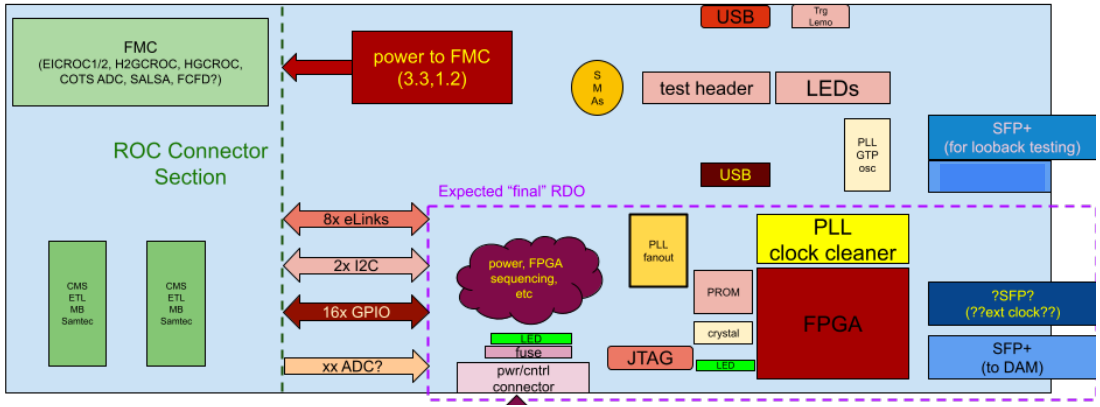
A collaboration among BNL, LBNL and Rice

- Rice: board schematics/layout, fabrication/assembly, QA
- LBNL: FPGA firmware development
- BNL: integration and full chain test with Xilinx dev kit

Sketch of first SH prototype (v0) schematics



Readout board prototype v0 design



FPGA section:

- Xilinx Artix Ultrascale+ family
- PROM for remote reconfiguration
- PLL for clock jitter cleaner

- essentially serves functionalities of lpGBT+SCA/MUX64

Optical fiber - SFP+ modules

- 1 for data/timing, 10Gbs
- 1 transceiver for direct clock timing-only, 100MHz
- 1 for various loopback tests (NOT on the final RB)

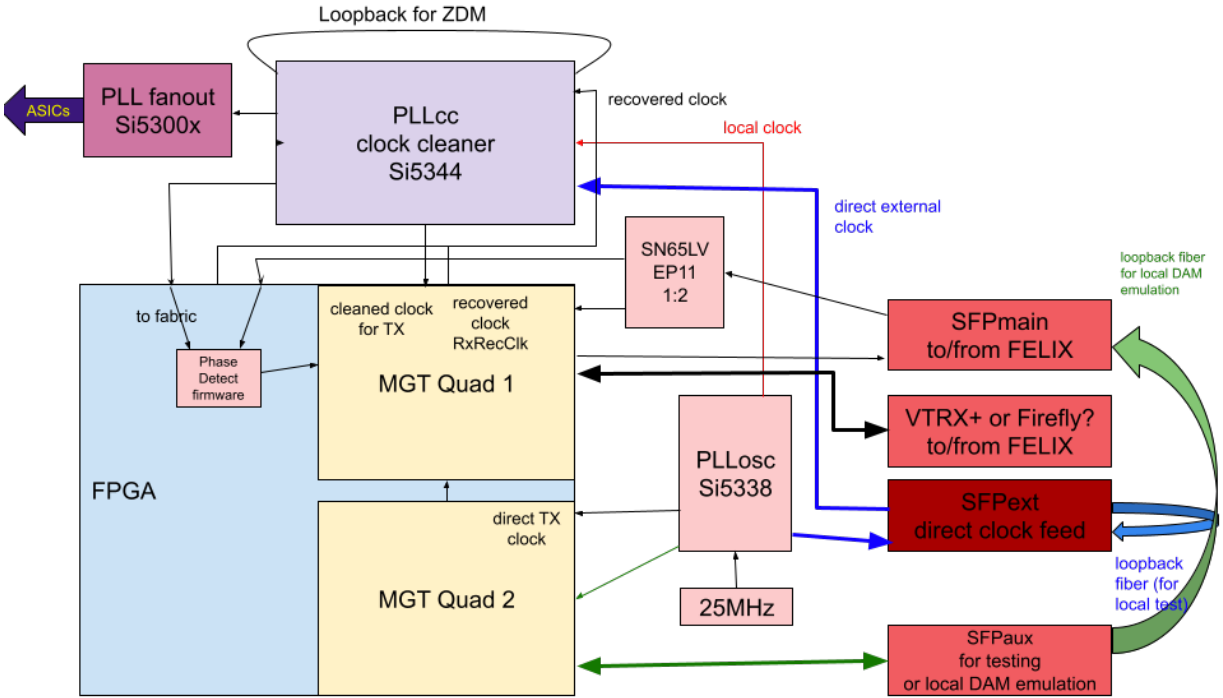
ROC connector:

- Connection to EICROC FMC test board
- Connection to CMS ETROC2 module board

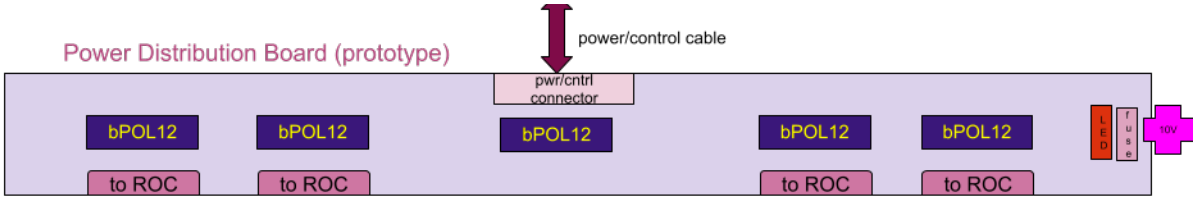
First very preliminary PCB schematic done! Lots of details to be worked out next.

Readout board prototype v0 design

Clock & Fiber Interconnect Scheme



Power board prototype v0 design



Output voltages needed:

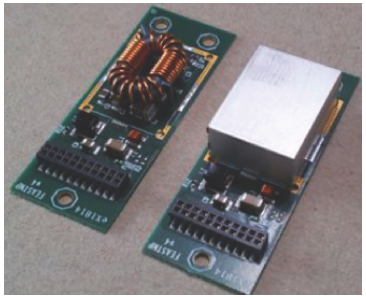
- EICROC: 1.2 V (for 16 ROCs)
- FPGA: a variety of 0.85V-3.3 V (probably 5 different voltages)
- SFP+: 3.3 V

Possible choices of DC-DC convertors:

- CERN **bPOL12V** or **bPOL48V**
- Commercial linear regulators

One possible is to use CERN FEASTMP_CLP modules

CERN FEASTMP_CLP module



For the v0 prototype, we decided to build a single board focusing mainly on the RB using linear regulators for powering FPGA/SFP+ and addressing a separate PB at a later step (including powering the EICROCs).

Preliminary road map and timeline

2024: **Prototype v0** (pre-prototype): establish all essential functionalities and readout chain.

2025: **Prototype v1**: first prototype with realistic dimensions, and meeting requirements/constraints for FTOF and BTOF.

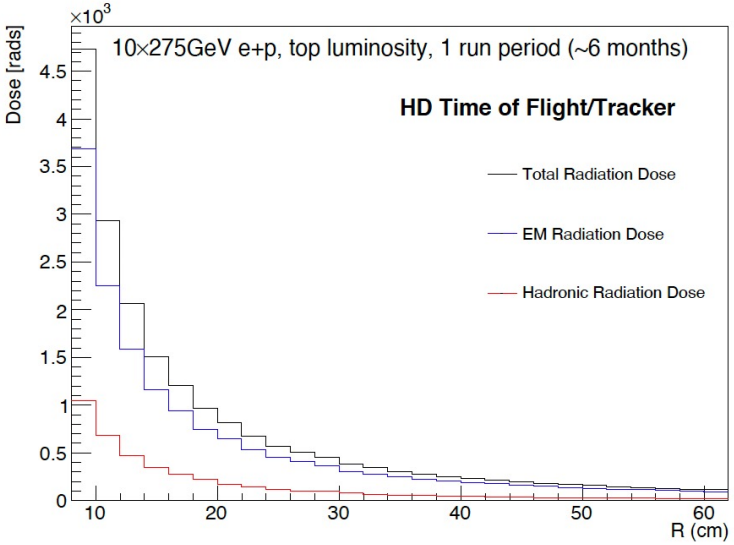
2026: **Prototype v2**: final prototype

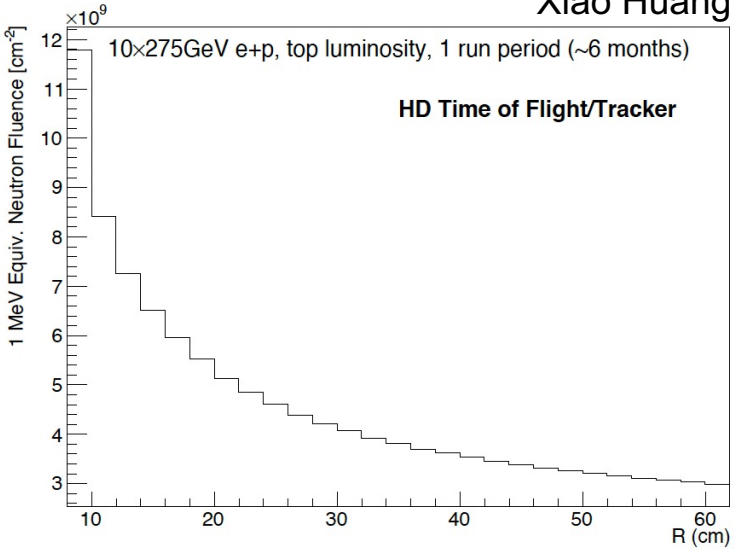
There is still lots of work/iterations ahead for design, prototyping and testing toward the final production but we are off to a good start with a strong team

Backups

FTOF radiation dose

Xiao Huang





Equivalent numbers for CMS ETL at HL-LHC is up to ~10^6x higher

- R-dependent HV map is necessary to maintain unform gains toward the end of lifetime
- Each SH is designed to provide up to 4 different HVs (thus 4 HV cables)

Necessity of multiple HV values per SH at ePIC to be determined by irradiation tests

- If needed, in which region? Possibly only needed for a small inner region, which can be implemented for a small set of SHs.

Service Hybrids R&Ds via eRD109

Institution	Contact	Milestones	Approximate dates
Rice	**Wei Li** **wl33@rice.edu**	Schematics 50% complete; major parts established	March 1, 2024
		Order major parts	March 1, 2024
		Schematics 100% complete (with internal review)	June 1, 2024
		Order all parts	June 1 , 2024
		PCB layout complete (with internal review)	Aug 1, 2024
		Board assembly complete. 5 pieces delivered.	Sep 31, 2024
		Basic electrical & power Q&A. FPGA loads a simple example FW from PROM and blinks LEDs.	Sep 31, 2024
LBNL	**Zhenyu Ye** **yezhenyu@lbl.gov**	Understand the interfaces between the Artix FPGA evaluation kit and ETROC2, and finalize the plan to use evaluation kit to communicate with ETROC2	Feb 1, 2024
		Obtain ETROC2 test board, Artix FPGA evaluation kit, extension board and cables needed to connect FPGA Kit and ETROC2 test board	March 1, 2024
		Complete 50% of the initial version firmware to communicate with ETROC2 using FPGA evaluation kit	April 1, 2024
		Compete the initial version of the firmware to communicate with ETROC2 using FPGA evaluation kit	May 1, 2024
		Finalize the firmware to communicate with ETROC2 using FPGA evaluation kit	June 6, 2024
BNL	**Prithwish Tribedy** **ptribedy@bnl.gov**	Continue Integration & understanding of EICROC0 ASIC + sensor with Xilinx dev kit (demonstration of full chain compatibility)	May 1, 2024
		Read the EICROC0 with the prototype board when available	Sep 30, 2024
		Understanding the interface of EICROC1 to the prototype board and finalize the plan for integration	Sep 30, 2024

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