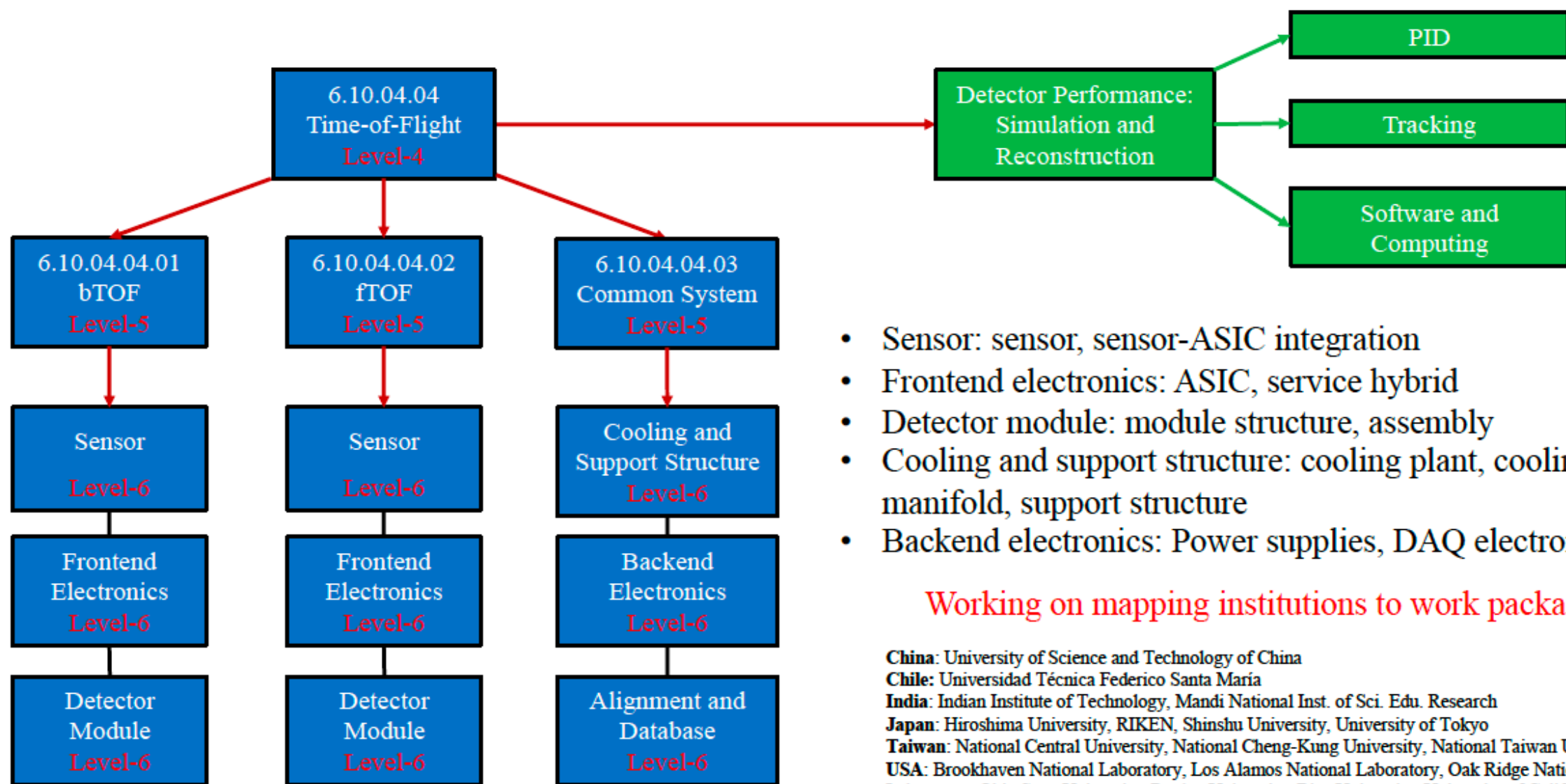


Backend electronics (common system)

Zhangbu Xu (BNL)

Tim Camarda, Jeff Landgraf, Prithwish Tribedy (BNL), Souvik Paul (SBU),
Tonko Ljubicic (Rice)

Proposed Working Package Structure



- Sensor: sensor, sensor-ASIC integration
- Frontend electronics: ASIC, service hybrid
- Detector module: module structure, assembly
- Cooling and support structure: cooling plant, cooling manifold, support structure
- Backend electronics: Power supplies, DAQ electronics

Working on mapping institutions to work packages

China: University of Science and Technology of China

Chile: Universidad Técnica Federico Santa María

India: Indian Institute of Technology, Mandi National Inst. of Sci. Edu. Research

Japan: Hiroshima University, RIKEN, Shinshu University, University of Tokyo



Taiwan: National Central University, National Cheng-Kung University, National Taiwan University

USA: Brookhaven National Laboratory, Los Alamos National Laboratory, Oak Ridge National Laboratory, Ohio State University, Purdue University, Rice University, University of California - Santa Cruz, University of Illinois at Chicago

Schedule and cost tasks for common system

- Mechanic structure
 - Support structures
 - Cooling systems
 - Cooling manifolds
- Alignment and Database
 - Computers and software
- Backend Electronics
 - High-Voltage Power Supplies
 - Low-Voltage Power Supplies
 - Patch Panels?
 - Cooling Infrastructures
 - Timing systems

Backend electronic systems

	Detector Name	Specification/ requirements	Comments from BNL EE group
	Sensor Type	AC-LGAD strip sensor	
	Sensor Details	TBD. Current assumption is each sensor has a size of 3.2*4 cm2 with 64*4=256 strips. The strip pitch and length are 0.5 and 10mm, respectively.	
	# Sensors	9216 assuming 144 BTOF modules, each with 64 sensors with a size of 3.2*4 cm2	
	# Readout Channels	2359296 assuming 9216 sensors with 64*4=256 strips per sensor	1mW / chanel = 2400W. power / FEB? is there power conversion on FEB? System total: 50W / 0.7 = 10.8kw => 10.8kW/ 10Vin = 1,080A
	LC current /FEB or module	ASICs will consume 2.4kW/144=16.4W per module assuming 1mW per channel. ASICs will be biased at 1.2V. There will be DC-DC conversion from 11V to 1.2V on FEB/RDO (TBD) with ~66% efficiency. The power consumption will be 25W and current 25W/11V=2.3A per module. If the ASIC power consumption is 2mW/channel, the power consumption will be 50W and current 4.5A per module.	
	HV System(s)	TBD. Possible choices include CAEN SY4527 chasis and A1625 modules, or something similar	require 18x A1625 modules & 2x SY4527 crates => 18 unit rack space
	HV current	<10 mA at 200-400V per detector module	
	Readout ASIC	TBD. Candidates include EICROC modified for strip sensor readout, FCFD, HPSOC/ASROC/FAST	
	ASIC details /requirements	TBD. Geometry match strip sensor design, zero suppression, digital output with TDC for signal time-of-arrival and ADC for signal amplitude measurements, power consumption <1mW/channel, jitter contribution from ASIC < 15ps for MIP signals, ASIC+Sensor+clock timing resolution < 35ps, spatial resolution < 30 microns.	
	ASIC modes	Streaming readout, zero suppression with digital output with TDC and ADC info	
	Front-End Board	Low mass kapton flexible PCB, mounted with AC-LGAD sensors and frontend ASICs	
	FEB Data Transport	Electric Signals	LVDS over copper?
	System Timing	clock jitter < 5ps	
	Timing Requirements	clock jitter < 5ps, ASIC+Sensor+clock timing resolution < 35ps	
	Readout Board	288 RDO with FPGA and Fibre links, mounted near the end of BTOF from both sides at z=+-120cm (TBD)	
	Patch Panel	TBD. If space near the ends of the BTOF is limited and RODs have to be placed at some distance, we may need to put PPs between BTOF modules and RDOs, with 144 PPs from each side of BTOF.	
	Design Workforce	ASIC: EICROC by OMEGA/IJCLab/CEA-Irfu, FCFD by FNAL, HPSOC/ASROC/FAST by UCSC BNL/ORNL/OSU/Rice/UIC	FEB/ROB:

Common System Schedule/cost in the TOF Project

1	Activity ID	Activity Name	OD	Start	Finish	START	STOP
2	ECE06-10-04 EEW.10.04.04.03 TOF Common System						
3	EEW.10.04.04.03.01	TOF Support Structure and Cooling System				1-Oct-23	31-Dec-28
4	EEW.10.04.04.03.01.01	TOF Support Structure				1-Oct-23	31-Dec-28
5		TOF Support Structure Design				1-Oct-23	31-Mar-25
6		TOF Support Structure Prototyping				1-Apr-25	30-Sep-26
7		TOF Support Structure Production				1-Oct-26	31-Dec-28
8	EEW.10.04.04.03.01.02	TOF Cooling System				1-Oct-23	31-Dec-28
9		TOF Cooling System Design				1-Oct-23	31-Mar-25
10		TOF Cooling System Prototyping				1-Apr-25	30-Sep-26
11		TOF Cooling System Production				1-Oct-26	31-Dec-28
12	EEW.10.04.04.03.02	TOF Backend Electronics				1-Oct-23	31-Dec-28
13	EEW.10.04.04.03.02.01	TOF LV Power Supply				1-Oct-23	31-Dec-28
14		TOF LV Power Supply Design				1-Oct-23	31-Mar-25
15		TOF LV Power Supply Prototyping				1-Apr-25	30-Sep-26
16		TOF LV Power Supply Production				1-Oct-26	31-Dec-28
17	EEW.10.04.04.03.02.02	TOF HV Power Supply				1-Oct-23	31-Dec-28
18		TOF HV Power Supply Design				1-Oct-23	31-Mar-25
19		TOF HV Power Supply Prototyping				1-Apr-25	30-Sep-26
20		TOF HV Power Supply Production				1-Oct-26	31-Dec-28
21	EEW.10.04.04.01.02.03	BTOF Patch Panel and Cables (move to common)				1-Jan-24	30-Jun-28
22		BTOF Patch Panel and Cable Design				1-Oct-23	31-Mar-25
23		BTOF Patch Panel and Cable Prototyping				1-Apr-25	30-Sep-26
24		BTOF Patch Panel and Cable Production				1-Oct-26	31-Dec-28
25	EEW.10.04.04.03.02.04	TOF DAQ System				1-Jan-24	30-Jun-28
26		TOF DAQ System Design				1-Oct-23	31-Mar-25
27		TOF DAQ System Prototyping				1-Apr-25	30-Sep-26
28		TOF DAQ System Production				1-Oct-26	31-Dec-28
29	EEW.10.04.04.03.03	TOF Alignment System and Database				1-Oct-23	31-Dec-28
30	EEW.10.04.04.03.03.01	TOF Alignment System				1-Oct-23	31-Dec-28
31		TOF Alignment System Design				1-Oct-23	31-Mar-25
32		TOF Alignment System Prototyping				1-Apr-25	30-Sep-26
33		TOF Alignment System Production				1-Oct-26	31-Dec-28
34	EEW.10.04.04.03.03.02	TOF Database				1-Oct-23	31-Dec-28

EHTOF Low and High Voltage Power Supplies

ePIC power supply / system budget for AC LGAD TOF Detectors
Estimations based on previous or simular quotes plus %10 contingency
2023 T. Camarda

Item	Qty.	Description
LV cable feed	5k feet	6- 8AWG 2 conductor cable with sense wire (custom jacket)
LV Power supplies + bins	11x	PL506 with 6x modules and power bins (1 spare channel each)
LV power dist. boards	11x	20 channel power dist. board (powers 20 TOF modules)
LV Power Board (prototype)	1x	DC DC power conversion board prototype
LV Power Board	30x	DC DC power conversion production boards
HV crate	2x	Wiener MPOD crate for 500V modules
HV modules	18x	HV modules, 12 channel 5W/ch (500V @ 10.0ma)
HV multipair cable	18x	REDEL Multipair cable assembly: 12 channels/ cable

BTOF Low and High Voltage Power Supplies

Item	Qty.	Description
LV cable feed	1k feet	6- 8AWG 2 conductor cable with sense wire (custom jacket)
LV Power supplies + bins	2x	PL506 with 6x modules and power bins (1 spare channel each)
LV power dist. boards	2x	20 channel power dist. board (powers 20 TOF modules)
LV Power Board (prototype)	1x	DC DC power conversion board prototype
LV Power Board	4x	DC DC power conversion production boards
HV crate	1x	Wiener MPOD crate for 500V modules
HV modules	2x	HV modules, 12 channel 5W/ ch (500V @ 10.0ma)
HV multipair cable	2x	REDEL Multipair cable assembly: 12 channels/ cable



Wiener PL506 LV PS

- The PL 506 is a high sophisticated, high density, programmable 6-channel floating low-voltage power supply system. Using the remote monitoring and control features either via USB or Ethernet it can be used to supply external load-channels with high power consumption also over long distances. Up to 3kW (3U box) DC output power can be provided.

PL506 Features

- Up to 6 independent, potential free DC outputs, 600W each, total up to 3 kW output power
- Extremely low noise and ripple
- Channels can be operated in Master-Slave mode for paralleling of two or more outputs (current boosting).
- Floating range: +/-100V (default, optimal for low noise). Can be increased up to +/- 500V
- Programmable voltages and thresholds on voltages, currents and temperatures, ramp rates, fully controlled, programmable trip levels and action / group behavior, voltage or current controlled mode
- Air cooled, self-ventilated, with over temperature protection
- CE conform EN 50 081/82 part 1 (EN 50 022 B), safety in accordance with EN 60 950
- Ethernet and USB interfaces for remote monitoring and control, Web interface / SNMP
- 94V – 265VAC world-wide auto-range AC input, with power factor correction / sinusoidal mains current EN 61000
- DC Output connections: 6mm threaded bolts (M6-150A), Sense and temperature sensor connections: 9 pin Sub D connector for 2 channels, senses wired to terminals on rear side.
- Optional alphanumeric display
- Optional with Power fail- and System Reset- Signal
- Optional with Interlock input
- Optional direct water cooling with same size as air cooled ones
- Dimensions: 430mm x 3U (133mm) x 325mm [whd], weight: from 9.6 to 19 kg depending on the number of power modules

Wiener MPOD HV PS with 500V

- Multichannel High Voltage Modules
- WIENER presents with Mpod a new, universal multi-channel low voltage (LV) and high voltage (HV) computer controlled power supply system. Offering highest channel density the MPOD mainframe can house up to 10 plug-in modules which can be mixed in type and parameters. Up to 480 individually controlled high voltage channels are available in one mainframe
- MPOD high voltage modules of the ISEG EBS, EDS and EHS series have 4, 8, 16, 24, 32 or 48 channels with different maximum voltage and current ranges. Based on the patented sine-wave resonance inverter technology all ISEG MPOD high voltage modules are characterized by extremely low noise and ripple. Further all channels are individually controlled and monitored and have a variety of programmable features. The EHS / EDS high voltage modules for Mpod are available with common ground or floating outputs.



Features

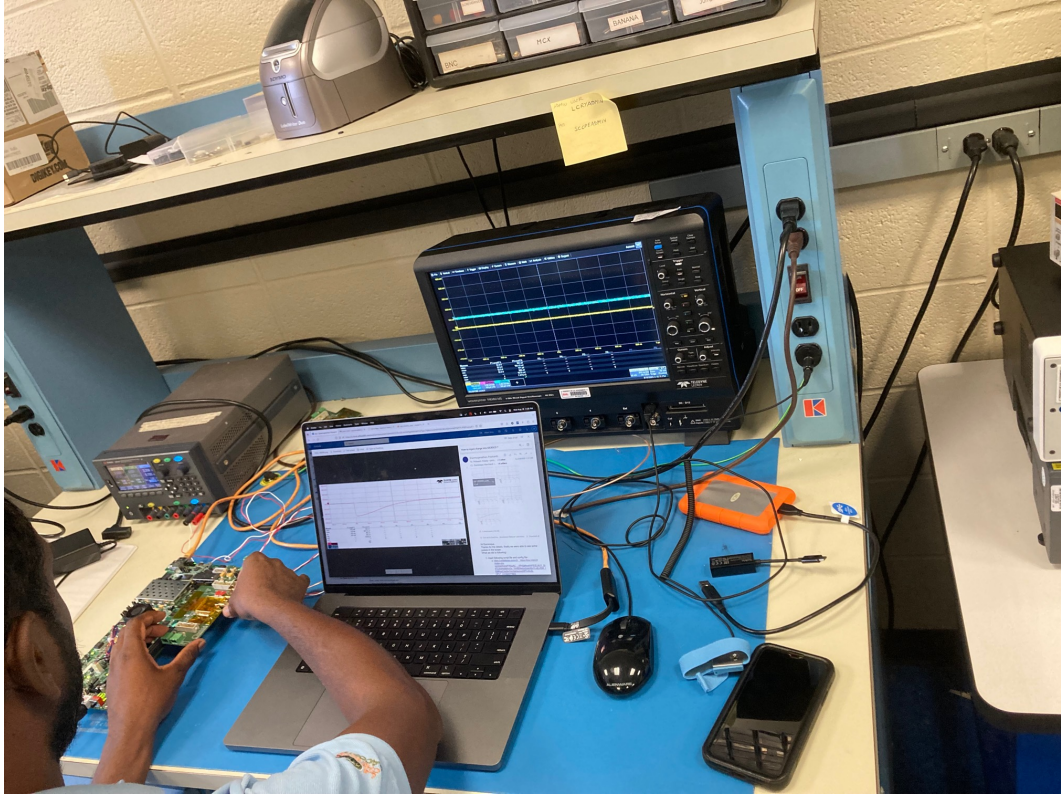
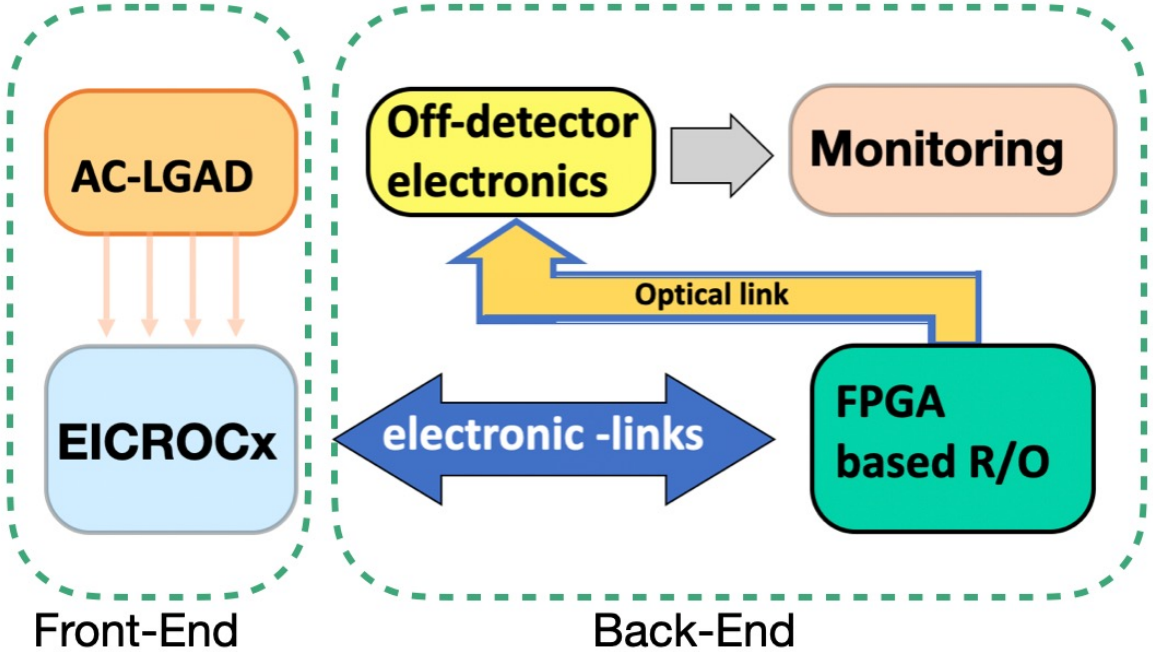
- 4, 8, 16, 24, 32 or 48 channels per module
- voltages up to 20 kV and currents up to 15 mA / channel
- high voltage channels with common GND or floating (20V or optional 200V/2000V max Potential difference)
- output connectors: 4 / 8 / 12 channel modules -> SHV; 16 channel modules -> SHV or REDEL multi pin; 32/48 channel modules -> REDEL multi pin
- Low ripple and noise (typically <10mVpp, High precision series <5mVpp)
- 16 or 21 bit voltage setting and measurement resolution
- 16 or 21 bit current measurement resolution
- Hardware current and voltage limit per module
- Programmable fast hardware current trip or software controlled trip for each channel
- Protection circuitry e.g. safety loop, optional individual channel inhibit
- Each channel fully remote controllable via software (CAN-bus or Ethernet)
- Dimensions: 6U x 40.64mm x 220mm Dimensions: 6U x 40.64mm x 220mm
- Weight: ca. 2 kg

DAQ

Tonko and Jeff

Detector Chain Costs (RDO -> Readout Computer)		
		#units
General DAQ (BTOF)		
	RDO	288
	Fiber (RDO -> Platform Trunk Patch Panel)	288
	Platform Trunk Patch Panel	288
	Fiber (Trunk)	288
	DAQ Room Patch Panel	288
	Fiber (Patch -> FELIX)	288
	FELIX	7
	Readout Computer	7
	labor for fiber install, rig, test, termination	288
	Total Cost (General DAQ Components)	
General DAQ (ETOF)		
	RDO	212
	Fiber (RDO -> Platform Trunk Patch Panel)	212
	Platform Trunk Patch Panel	212
	Fiber (Trunk)	212
	DAQ Room Patch Panel	212
	Fiber (Patch -> FELIX)	212
	FELIX	5
	Readout Computer	5
	labor for fiber install, rig, test, termination	212

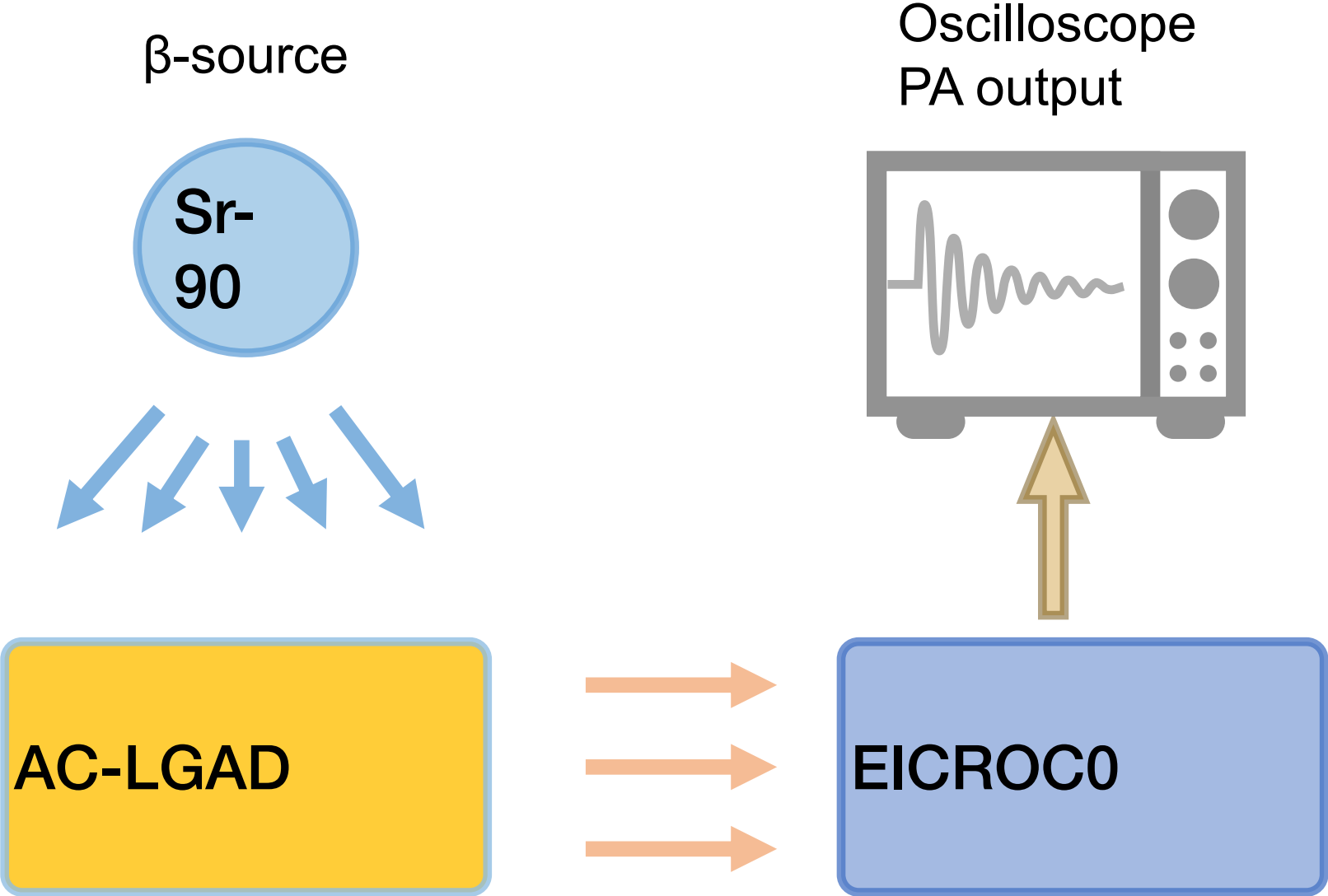
Full readout chain



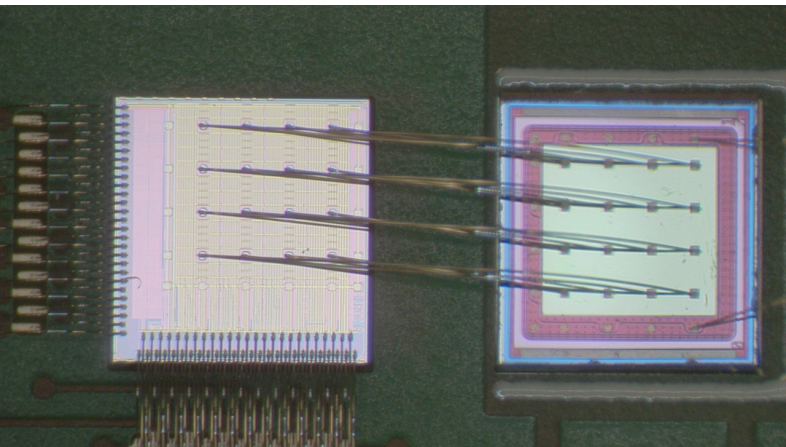
Setup at BNL

From Souvik Paul and Prithwish Tribedy

First signal with AC-LGAD + EICROC0 Sr 90 source (Schematic)

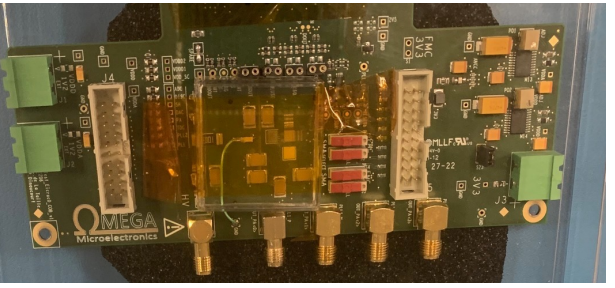
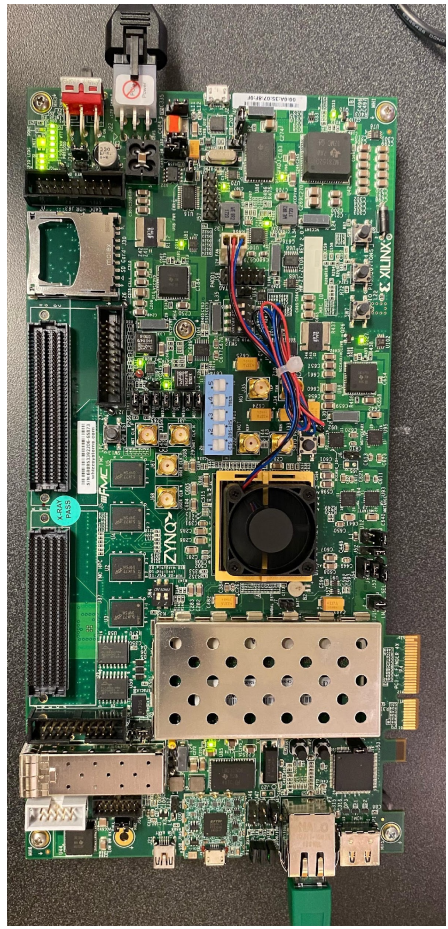


First signal with AC-LGAD + EICROCO Sr 90 source



EICROCO

AC-LGAD



Carrier board



First signal (analog pre-amplifier output) from sensor bonded to ASIC using Sr90 source was seen by the BNL team

Plans for FY 2024 RD

Institution	Contact	Milestones	Approximate dates
Rice	Wei Li wl33@rice.edu	Schematics 50% complete; major parts established	March 1, 2024
		Order major parts	March 1, 2024
		Schematics 100% complete (with internal review)	June 1, 2024
		Order all parts	June 1, 2024
		PCB layout complete (with internal review)	Aug 1, 2024
		Board assembly complete. 5 pieces delivered.	Sep 31, 2024
		Basic electrical & power Q&A. FPGA loads a simple example FW from PROM and blinks LEDs.	Sep 31, 2024
LBNL	Zhenyu Ye yezhenyu@lbl.gov	Understand the interfaces between the Artix FPGA evaluation kit and ETROC2, and finalize the plan to use evaluation kit to communicate with ETROC2	Feb 1, 2024
		Obtain ETROC2 test board, Artix FPGA evaluation kit, extension board and cables needed to connect FPGA Kit and ETROC2 test board	March 1, 2024
		Complete 50% of the initial version firmware to communicate with ETROC2 using FPGA evaluation kit	April 1, 2024
		Complete the initial version of the firmware to communicate with ETROC2 using FPGA evaluation kit	May 1, 2024
		Finalize the firmware to communicate with ETROC2 using FPGA evaluation kit	June 6, 2024
BNL	Prithwish Tribedy ptribedy@bnl.gov	Continue Integration & understanding of EICROC0 ASIC + sensor with Xilinx dev kit (demonstration of full chain compatibility)	May 1, 2024
		Read the EICROC0 with the prototype board when available	Sep 30, 2024
		Understanding the interface of EICROC1 to the prototype board and finalize the plan for integration	Sep 30, 2024
All			

Backend Electronic System: most are on EIC project side?

- HV and LV PS:
Zhangbu, Tim Camarda
- DAQ and Fiber:
Tonko, Jeff and Fernando
- Alignment and Database?
- Follow up with engineers from EIC project to work on the requirements and schedule, make sure that everywhere in TOF project and EIC project schedule/cost are consistent

To-do list

HV/LV PS and cables

- Work on and finalize more detailed requirements
 - Voltage and current limits
 - Channel counts and module numbers
 - Connectors and patch panels
 - Routing of cables and platform?
- Work on a pre-production assembly in 2024 and test in 2025-26
- Purchase order and assembly 2027-29?

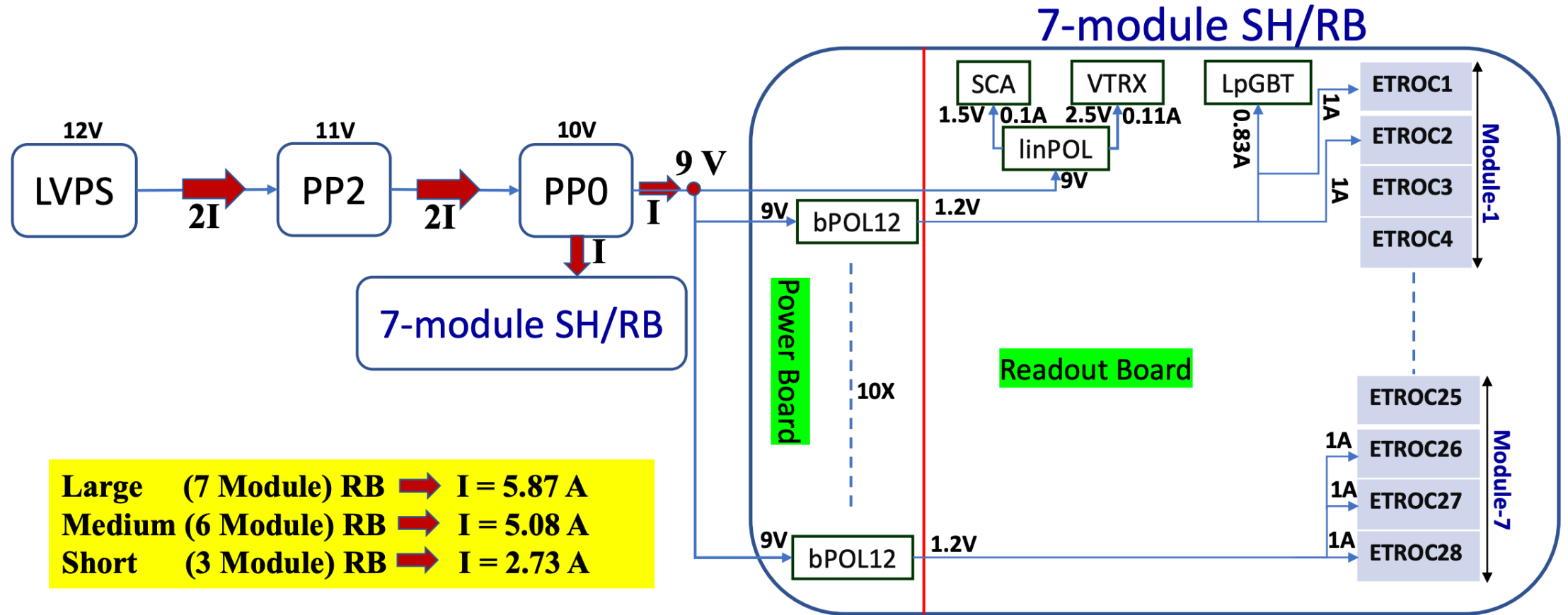
DAQ and fibers

- See Tonko's introduction and discussion
- EICROC1 DAQ chain R&D

backup

Service Hybrids

Powering of Readout board



Q&A from Tim

Q. slide # 5: This is the internal detector wiring?

Yes, correct. This is wiring on the readout PCB board.

Q. how is the power regulation done on the read-out board?

LV is regulated via DC-DC converters

I see here you have an inner assembly where everything is connected via a patch panel.

Q. Do you envision the patch panel as separate circuit boards mounted around the detector?

Yes, this is correct.

Q. Are you considering specific connector types or part numbers at this point, for both the modules and patch boards?

Yes, we have some preliminary estimate of numbers but they may change a bit as the design evolves

Q. What is the LV and HV requirement for the modules?

12V for LV and 200-350V for HV.

Q. slide #13: what is ~ space given here for cable routing?

We estimated total space requirement in z of about 7 cm max including all cables, service etc.

Optimizing the layout

0.5x0.5 mm² option

	Forward	Backward
Sensors/ASICs	8704	4608
LV cables	424	248
HV cables	424	248
Fibers	212	124



0.8x0.8 mm² option

	Forward	Backward
Sensors/ASICs	3112	1744
LV cables	248	184
HV cables	248	184
Fibers	124	92

For each module:

- 1 fiber to DAQ
- 2 LV cables (1 supply, 1 return)
- 2 BV cables (1 supply, 1 return)

ETOOF Power budget

0.8x0.8	Forward	Backward
Sensors	0.2kW	0.13kW
EPTROC	3.2kW (6.4kW)	1.8kW (3.6kW)
DC-DC	1.3kW	0.75kW
IpGBT, VTRx+, SCA	0.2kW	0.12kW
Power cables	0.2kW	0.12kW
Total	6.1kW	2.9kW

1.3x1.3	Forward	Backward
Sensors	0.1kW	0.05kW
EPTROC	1.2kW (2.4kW)	0.7kW (1.4kW)
DC-DC	1.3kW	0.75kW
IpGBT, VTRx+, SCA	0.2kW	0.12kW
Power cables	0.2kW	0.12kW
Total	3kW	1.8kW