

# Silicon Detectors

## part 1

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@BrookhavenLab

## Why sensors made of silicon?

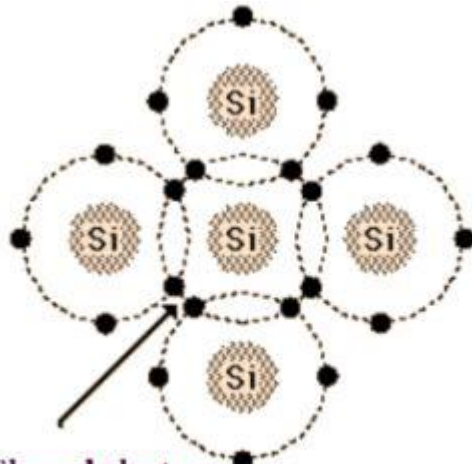
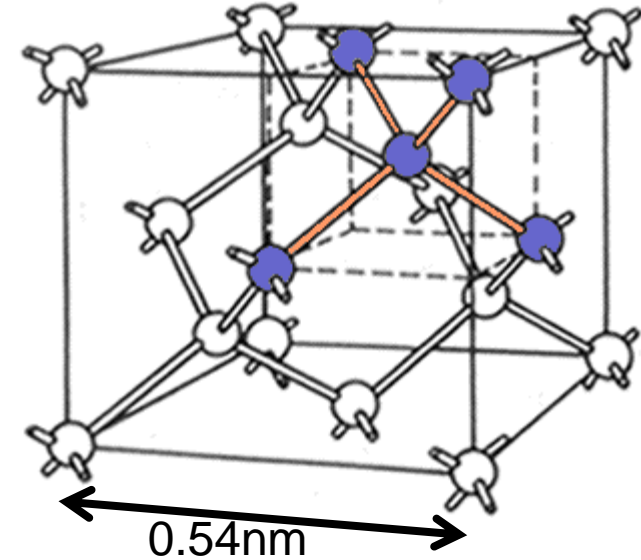
- Silicon is a semiconductor sensitive to photons and charged particles
  - Fair signals created, “easily” detected
  - No need of multiplication (in most applications)
- Silica ( $\text{SiO}_2$ ) everywhere
  - “easy” to make silicon crystals
- Very well-developed technology (simplified version of Integrated Circuits - IC)
  - Silicon dioxide excellent insulator
  - Possibility to finely segment the electrodes down to few tens of  $\mu\text{m}$
- Operation close to Room Temperature (RT)



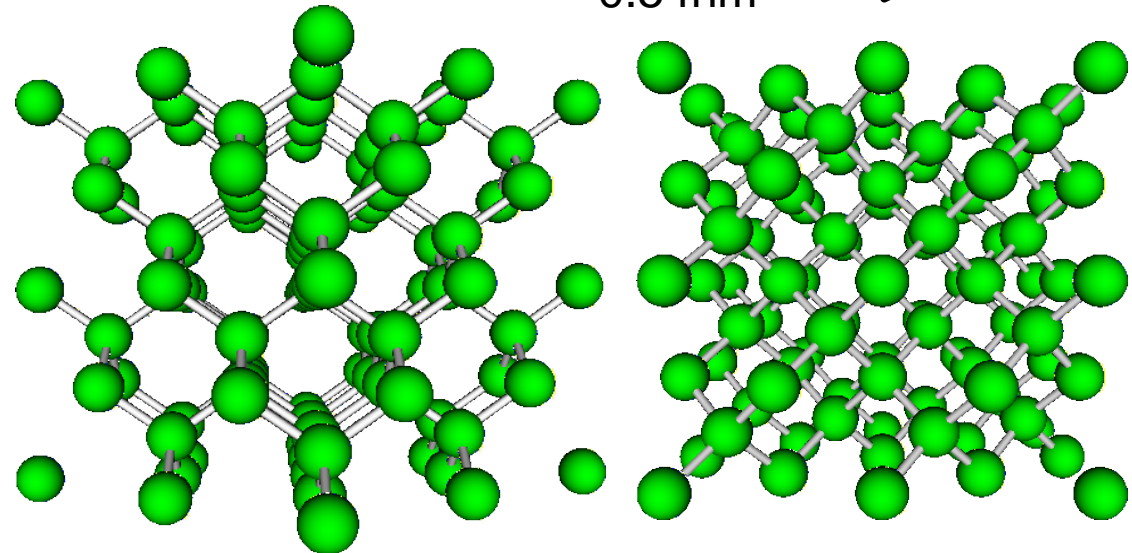
# The silicon crystal

Diamond structure (tetrahedron)  
Unit cell has 8 atoms

Group →	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Period ↓	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
1	1 H																	2 He
2	3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
3	11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
4	19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
5	37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
6	55 Cs	56 Ba	57 La	* 72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
7	87 Fr	88 Ra	89 Ac	* 104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Cn	113 Nh	114 Fl	115 Mc	116 Lv	117 Ts	118 Og
				* 58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu	
				* 90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr	



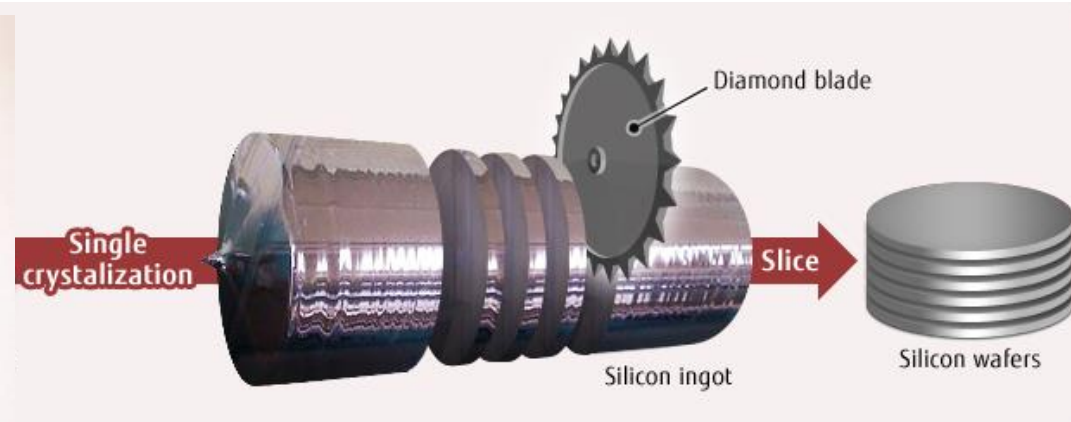
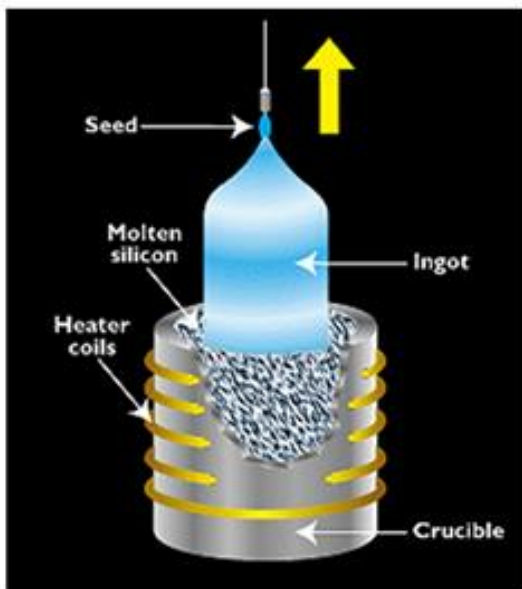
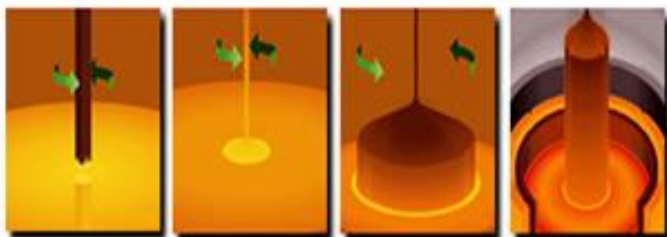
Shared electrons  
in covalent  
bond



110

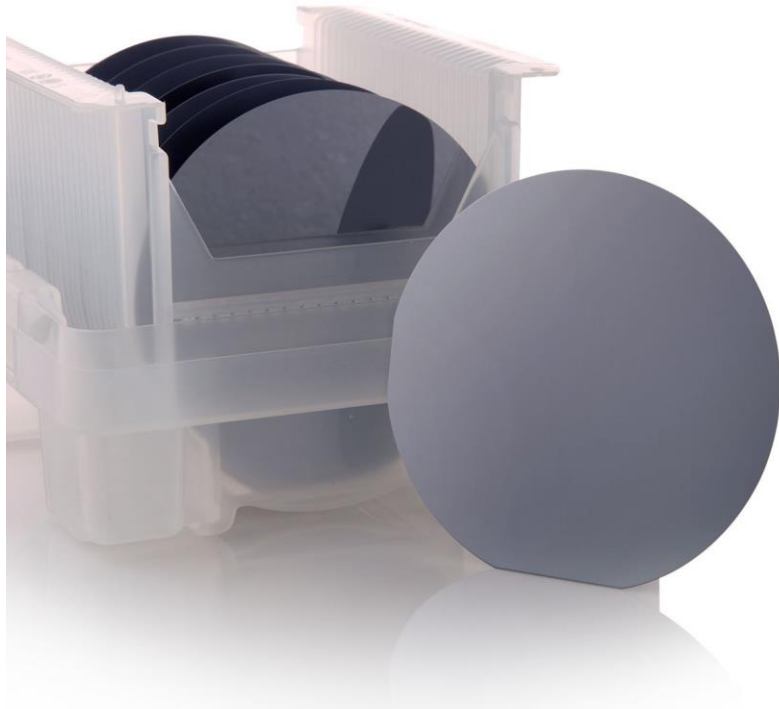
100

# Czochralski method

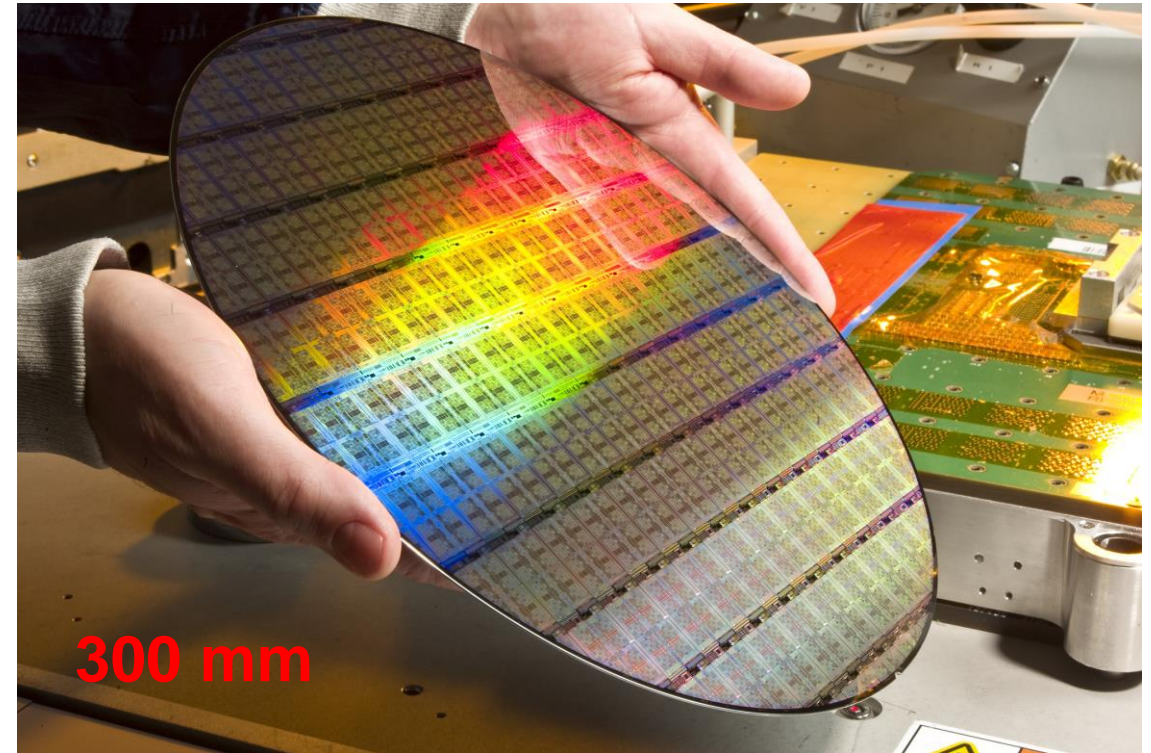




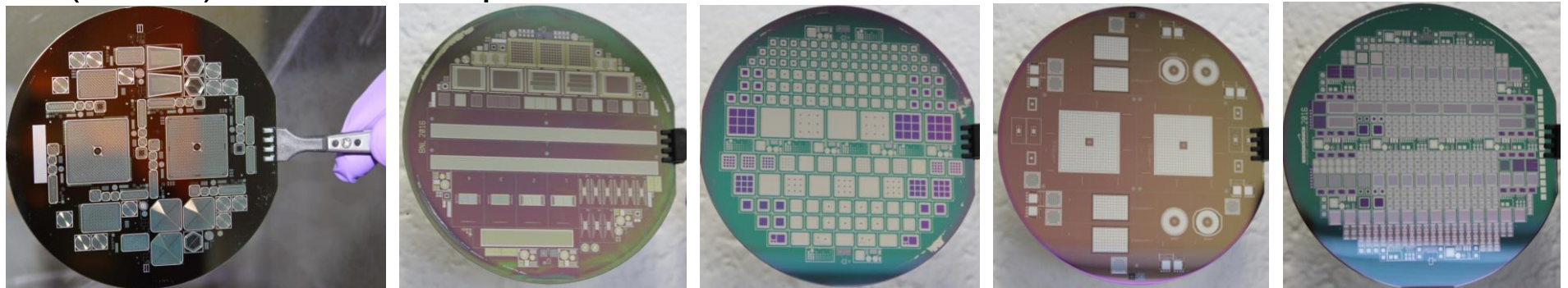
Silicon wafers as you can buy



Integrated Circuits (IC) on a Silicon wafer



4" (10-cm) silicon wafer processed at BNL





# Two great materials: Silicon vs Steel

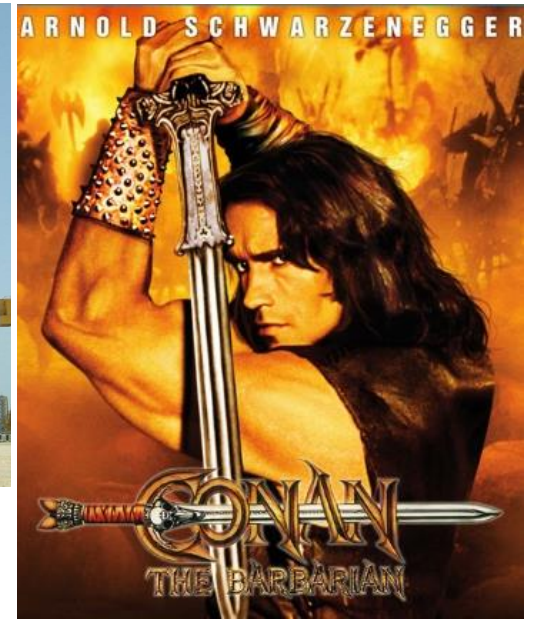
Shockley,  
Bardeen,  
Brattain 1950



Moore,  
Noyce,  
Grove  
at Intel 1978

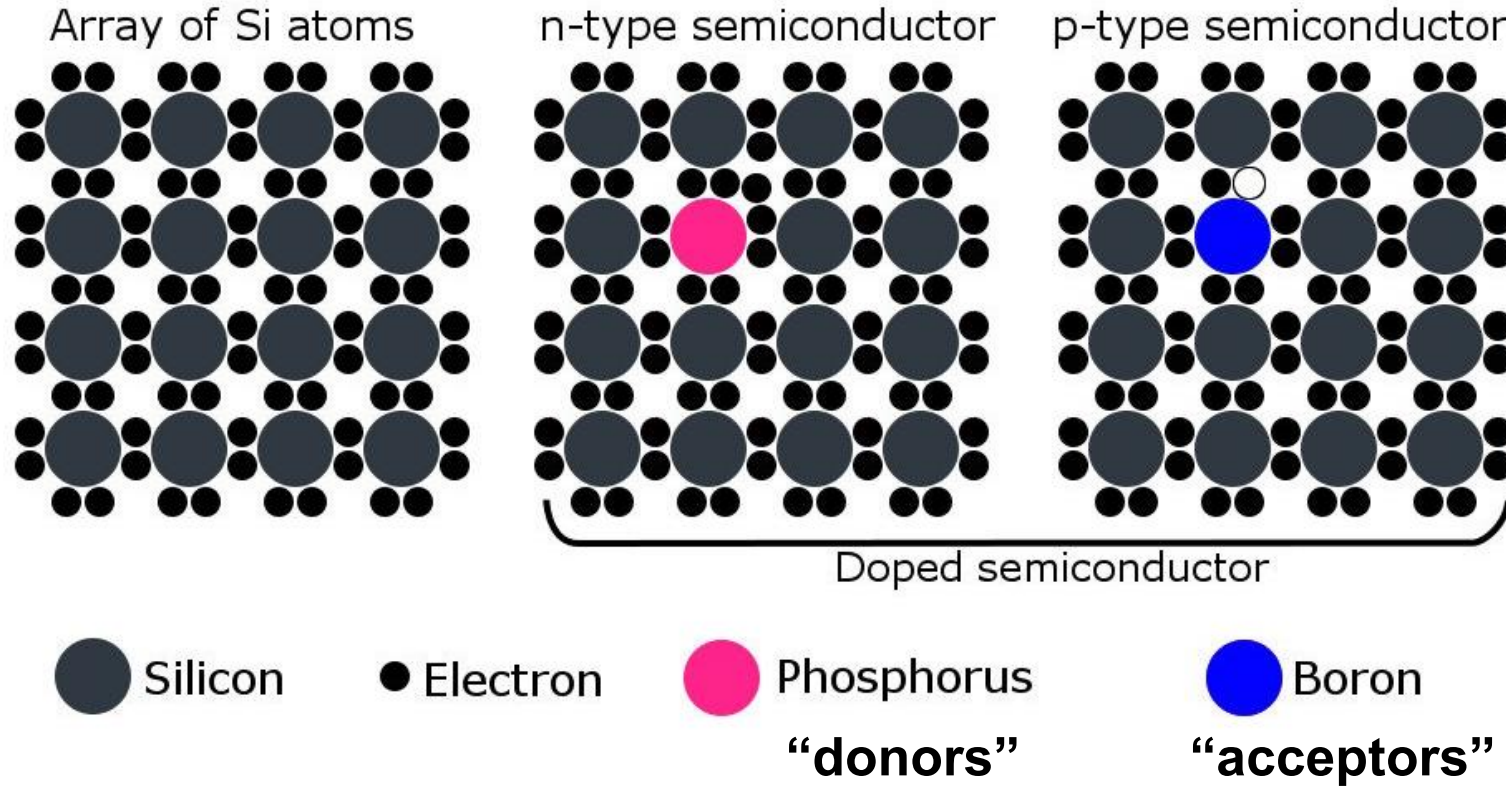


*Falcata*  
(4<sup>th</sup> century BC)





# Electrons and holes in semiconductors



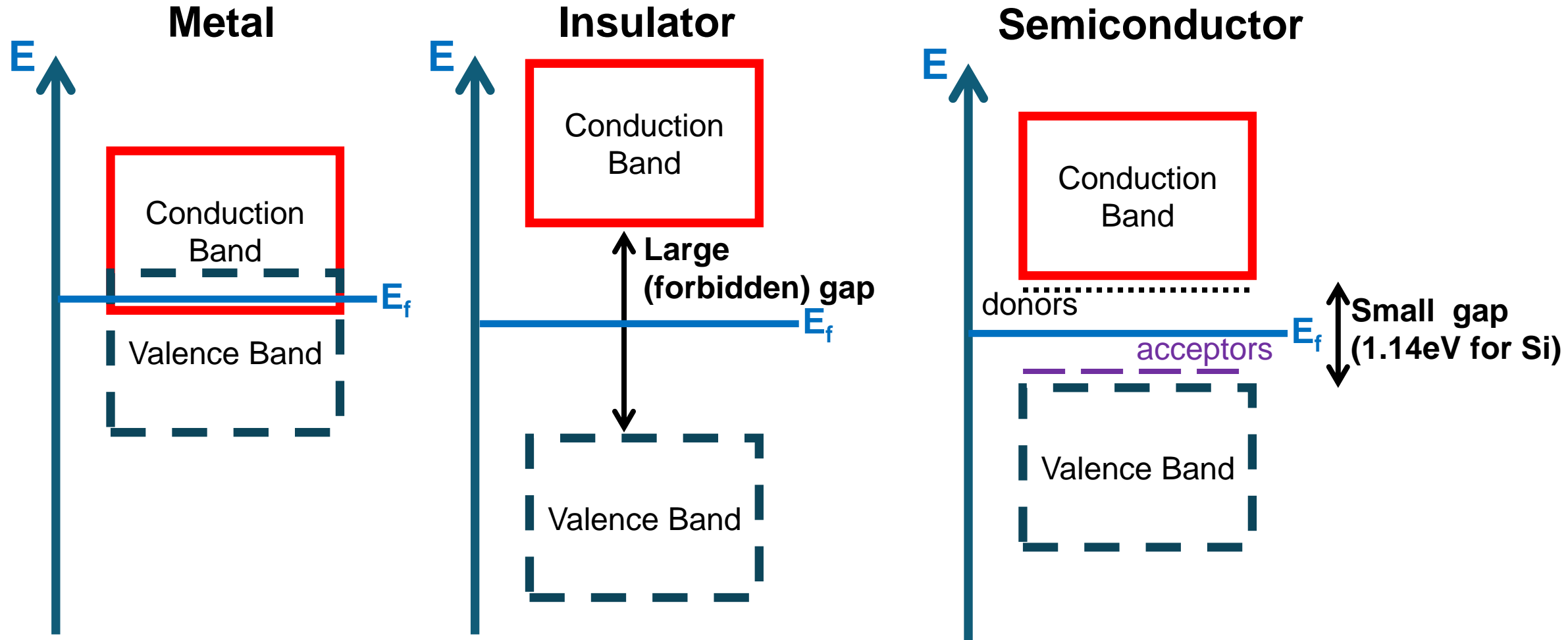
$\sim 10^{22}$  atoms of Si/cm<sup>3</sup>

High doping of B/P if their concentration is  $> \sim 10^{19}$  cm<sup>-2</sup> (low resistivity)

Low doping of B/P if their concentration is  $< 10^{12}$  cm<sup>-2</sup> (high resistivity)

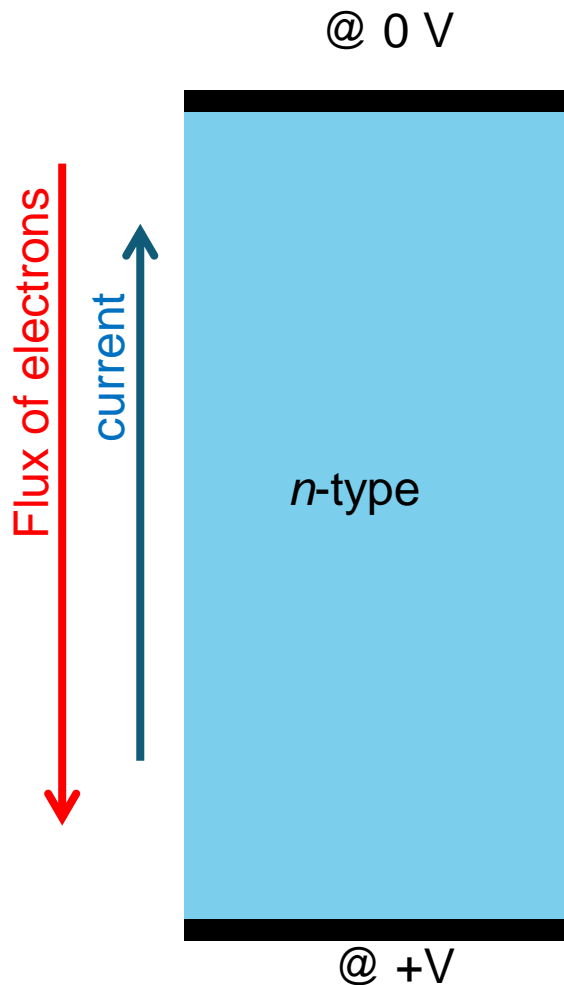
Electron and holes can be treated as “free” particles, negatively and positively charged. If tied on their atom, charge neutrality holds; if freed from the atom, a net charge develops.

# Band Structure





## A slab of (n-type) silicon



Upon application of a Voltage  $V$ , free electrons and holes distribute as to satisfy Maxwell Equations.

Gauss Law (in 1D) :  $d\mathbf{E}/dx = \rho/\epsilon$

N-type has negligible holes.  
Since charge neutrality holds,  $\rho=0$ .

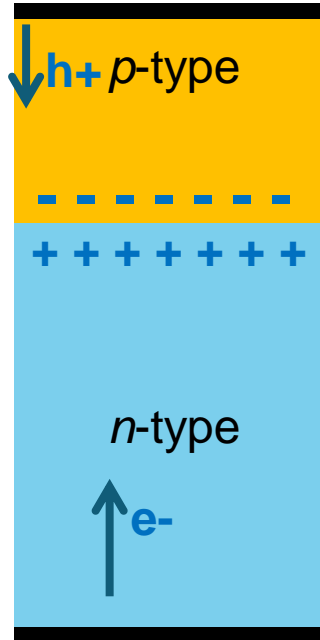
→  $\mathbf{E} = \text{constant} = V/\text{thickness}$

Electrons are emitted by electrode at 0V and drift to electrode at +V.  
Current is given by Ohm's law

## Two slabs face-to-face: n-type + p-type

### The junction Diode (forward bias)

Holes on the p-side diffuse to the n-side, leaving ionized (negative) Boron behind. Electrons on n-side diffuse to the p-side, leaving ionized (positive) Phosphorus behind.

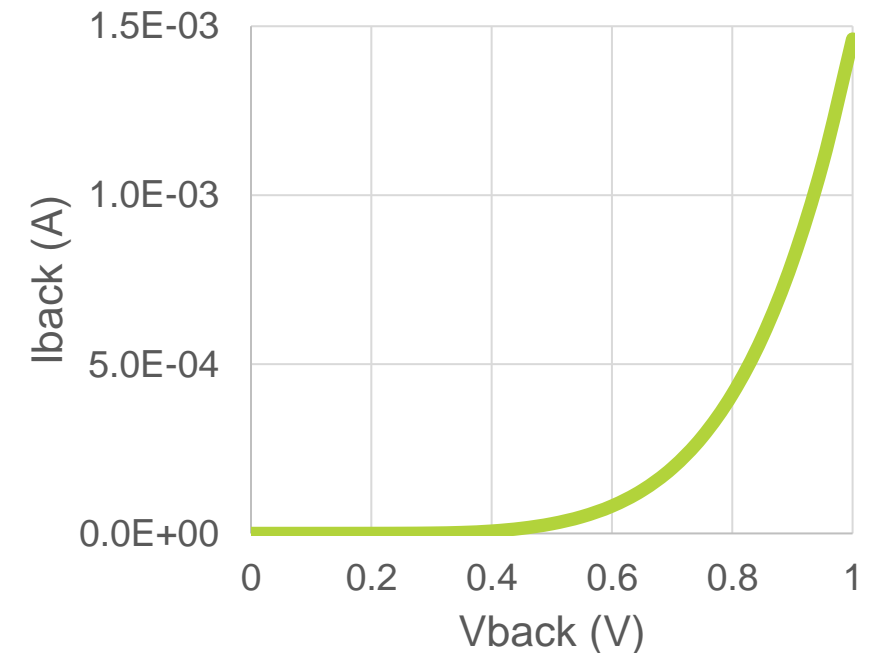


Charge density builds up and so electric fields (Maxwell equation) (or, a potential barrier) which counteracts the diffusion process.

At the junction, a charge region exists (even at zero bias) → built-in voltage.

If we lower the potential barrier by applying an external voltage, more electrons and holes can diffuse on the other side of the junction

→ **Forward bias.**



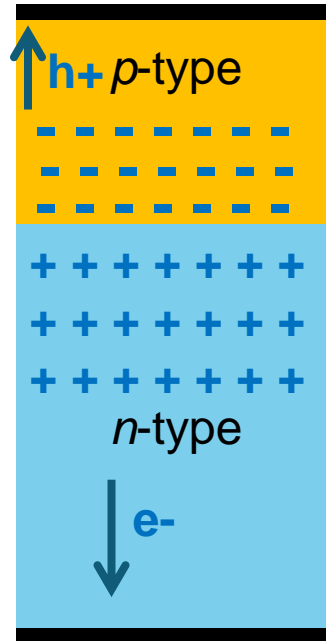


## Two slabs face-to-face: n-type + p-type

### The junction Diode (reverse bias)

If we increase the potential barrier by applying an external voltage, the flow of electrons and holes is inhibited: no current!!

@ 0



But Gauss law still holds:

If we have a voltage across the junction, a net charge must develop across the junction:

Electrons and holes are swept away from the n and p-type regions, leaving behind a charged volume, made by ionized donors and acceptors.

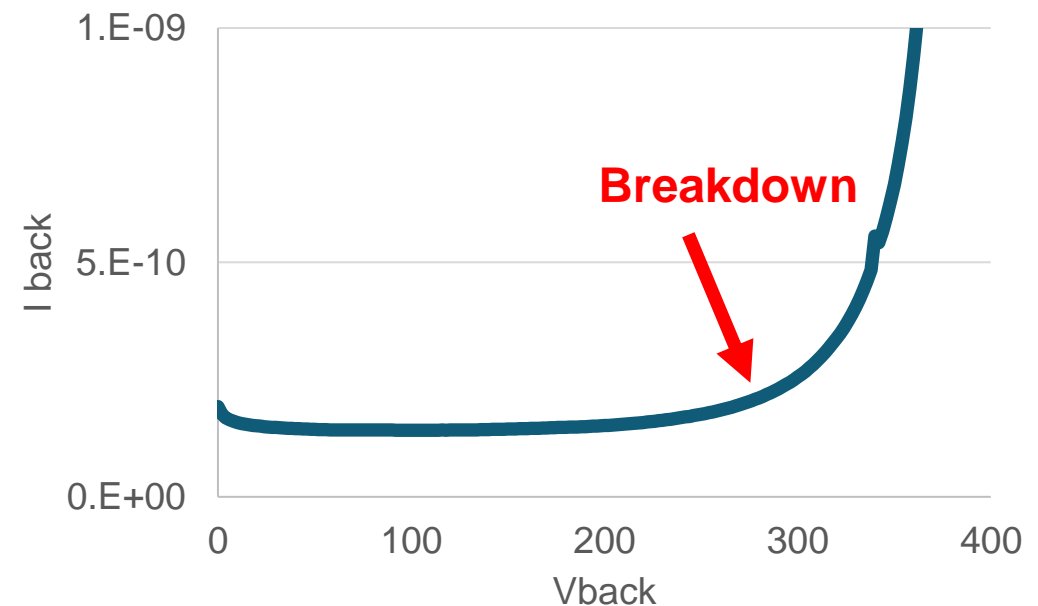
We speak of **Depleted** (from electrons and holes) **Region**.

Current is thermally generated in the depleted volume by SRH process.

(**leakage current, or dark current**)

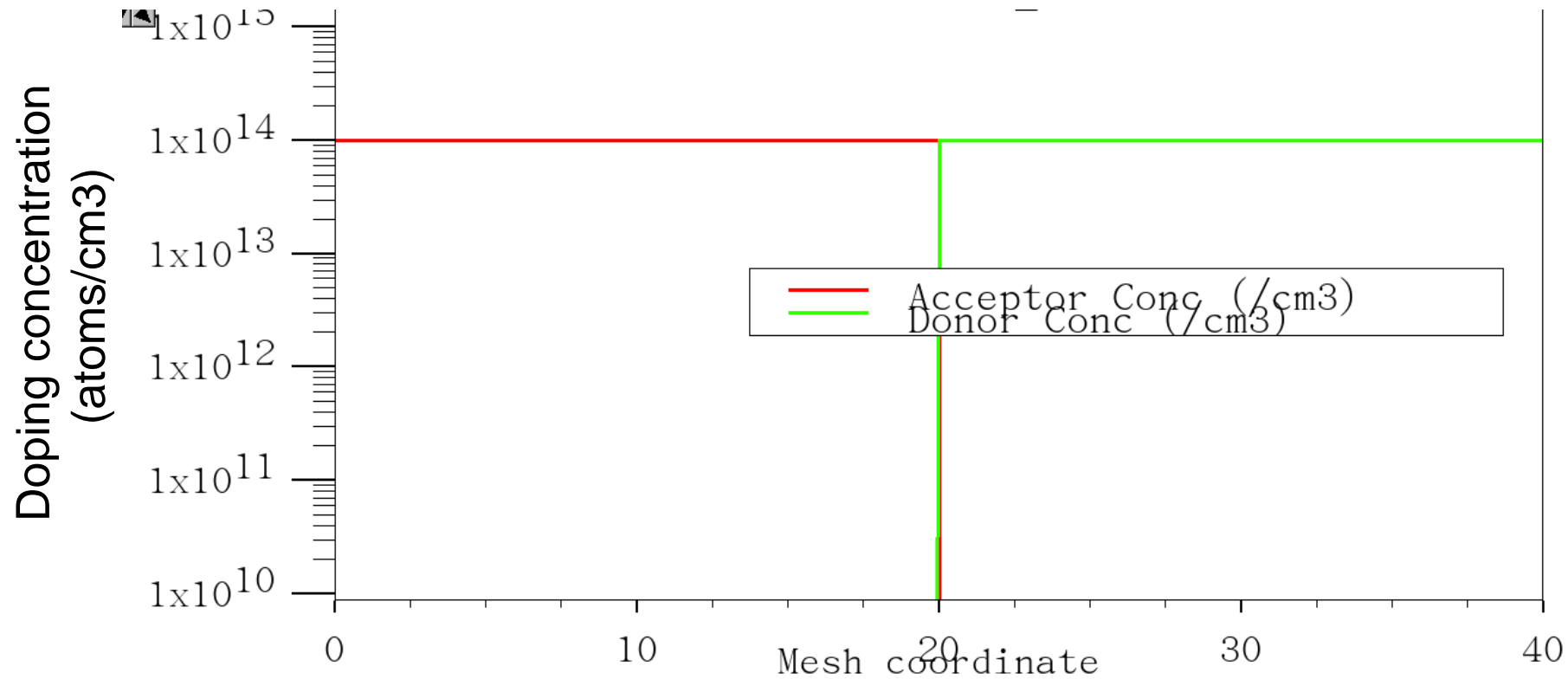
Max Voltage that can be applied is limited (breakdown will occur if electric field is too high,  $\sim 3e5$  V/cm in silicon)

@ +HV



# The depletion region - 1

Let's take a 1D diode, 40  $\mu\text{m}$  thick, with symmetric doping:  
20  $\mu\text{m}$  of p-type silicon in contact with 20  $\mu\text{m}$  of n-type silicon.  
Let's apply 10V at the n-type silicon.

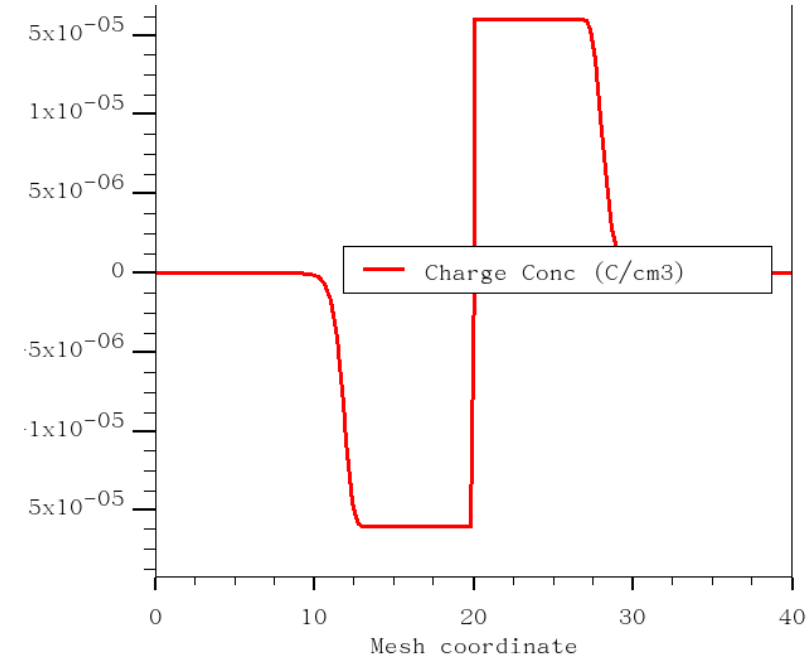
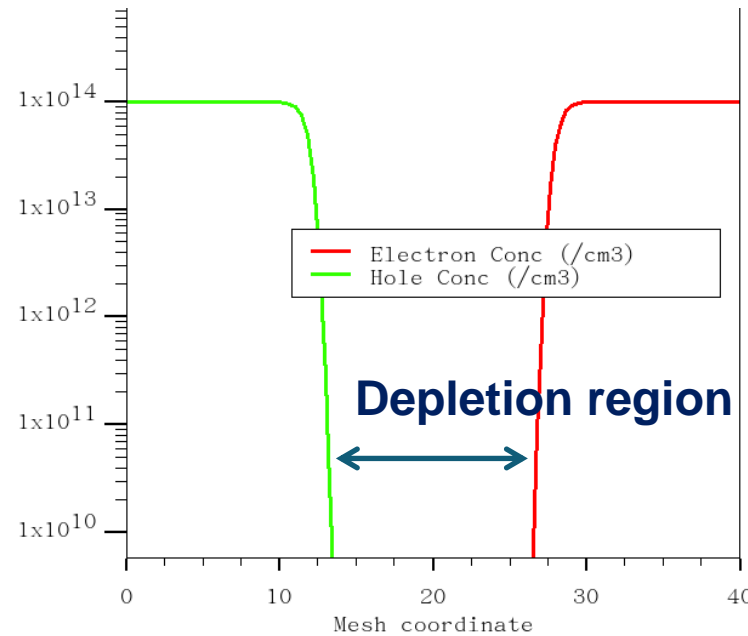




# The depletion region - 2

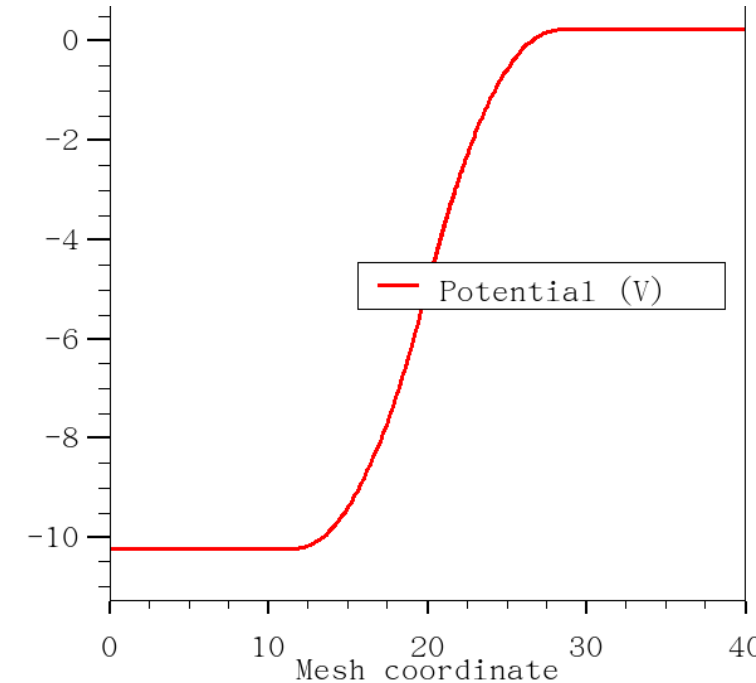
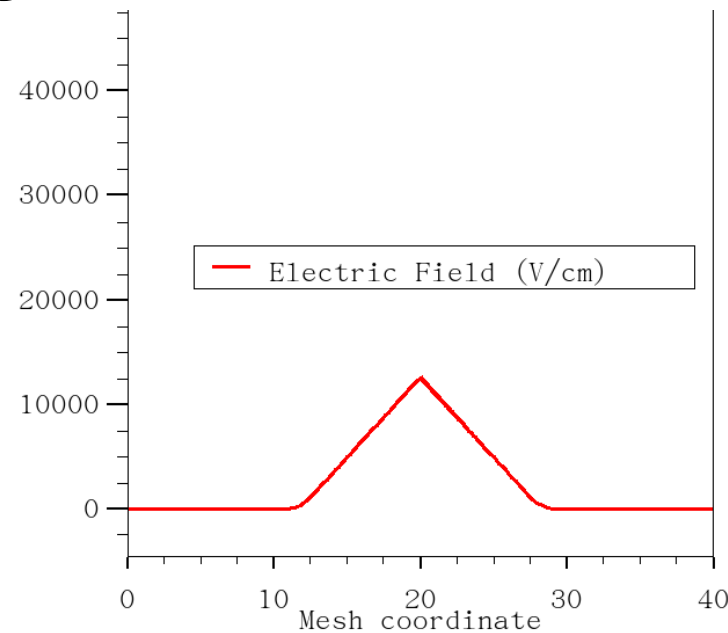
## In the depletion region:

- No electrons or holes
- Charge  $\neq 0$
- Electric field  $\neq 0$
- Potential barrier



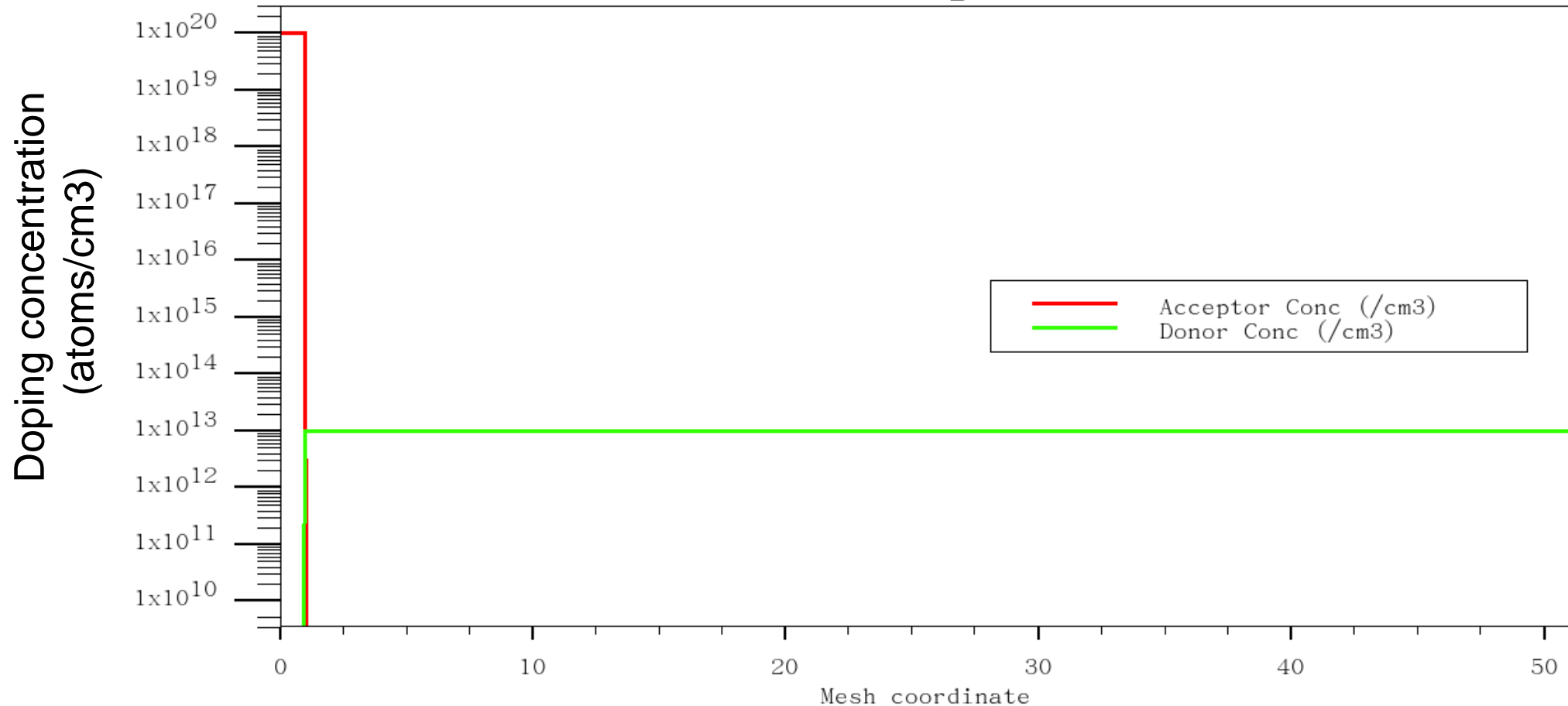
## Outside of the depletion region:

- electrons or holes = doping
- Charge = 0
- Electric field = 0
- equipotential



## The depletion region - 3

Let's take a 1D diode, 50  $\mu\text{m}$  thick, asymmetric doping:  
Shallow heavily doped p-type silicon in contact with 50  $\mu\text{m}$  of lightly doped n-type silicon.  
Let's apply 10V at the n-type silicon.





## The depletion region - 4

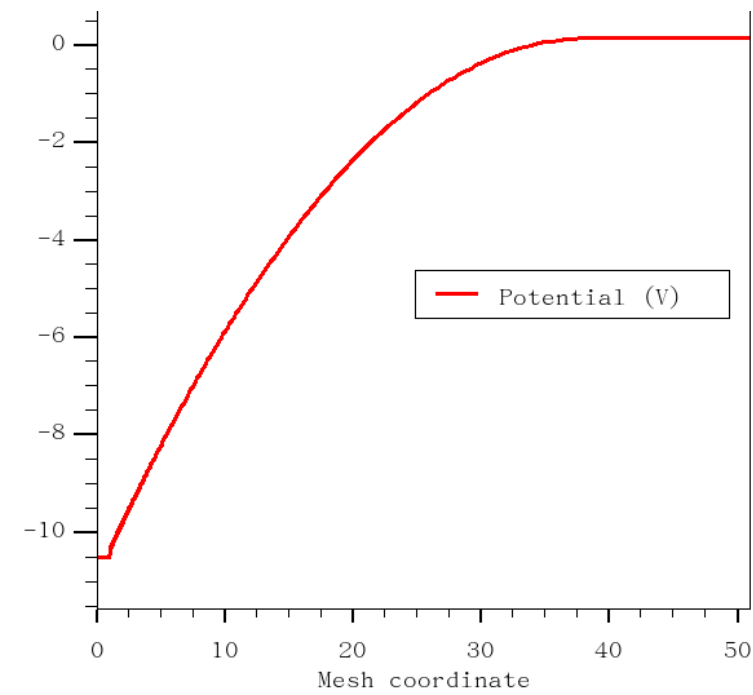
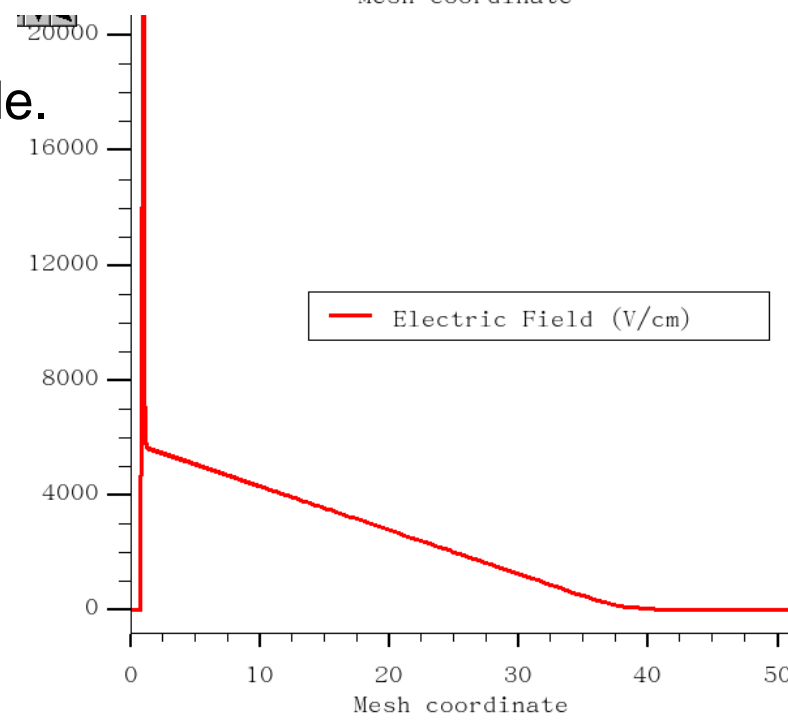
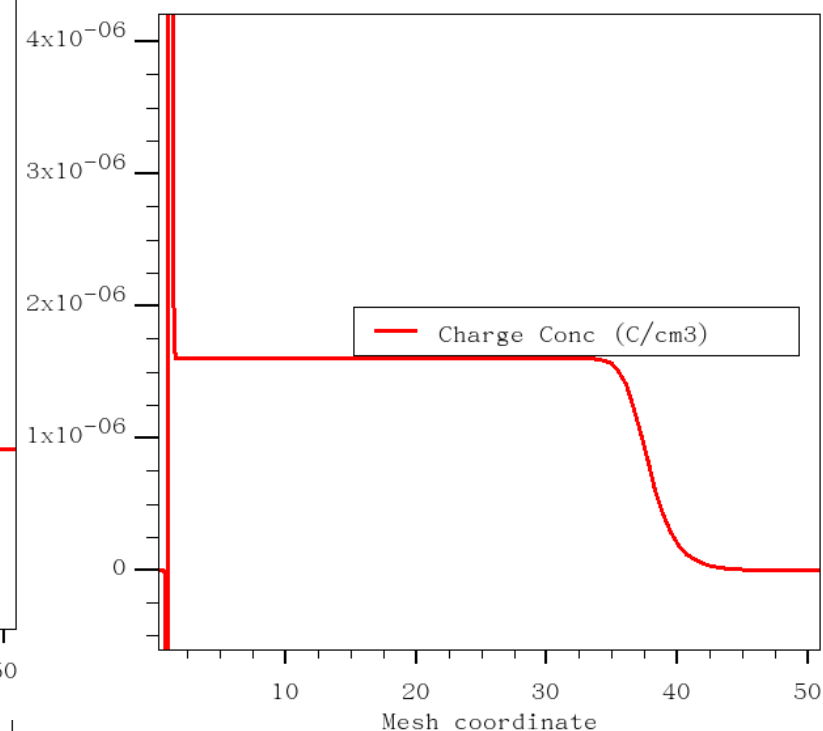
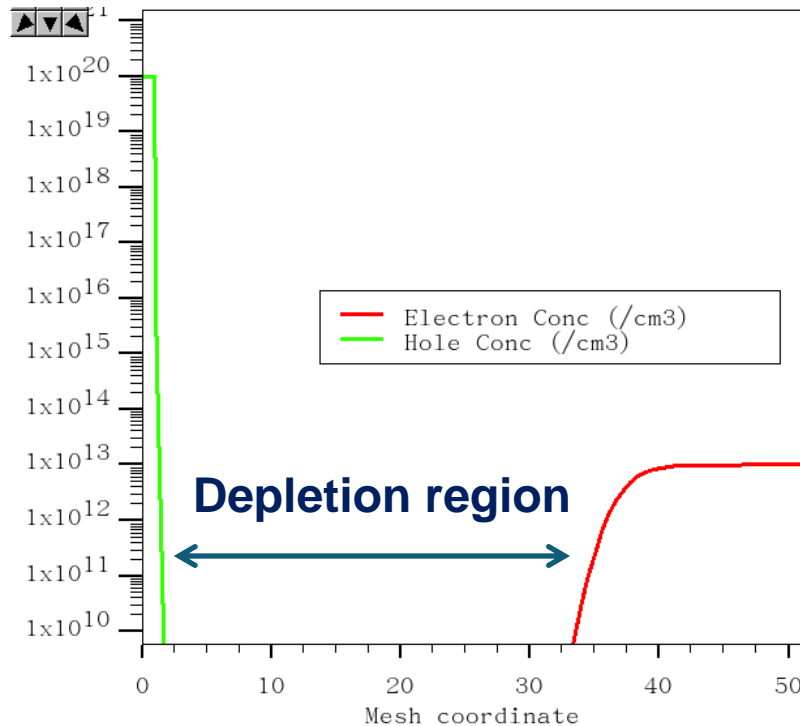
Again,  
in the depletion region:

- No electrons or holes
- Charge  $\neq 0$
- Electric field  $\neq 0$
- Potential barrier

But this time the depletion region extends only on the lowest doped side.

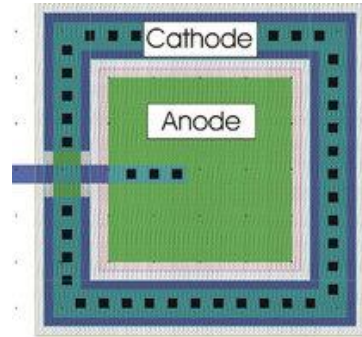
The n-side is almost fully depleted.  
**Sensors operate in full-depletion regime.**

$$\text{VFD} \sim \text{Thickness}^2 * N_{\text{doping}}$$



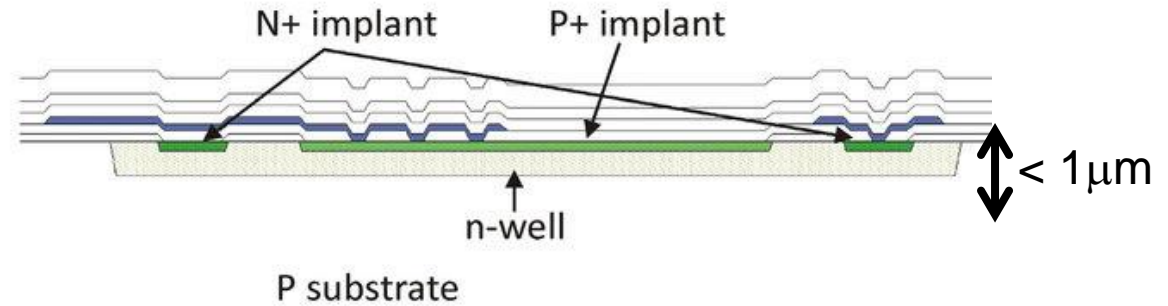
# Diode in integrated circuits

From the top



Highly doped,  
small depletion  
region

Section



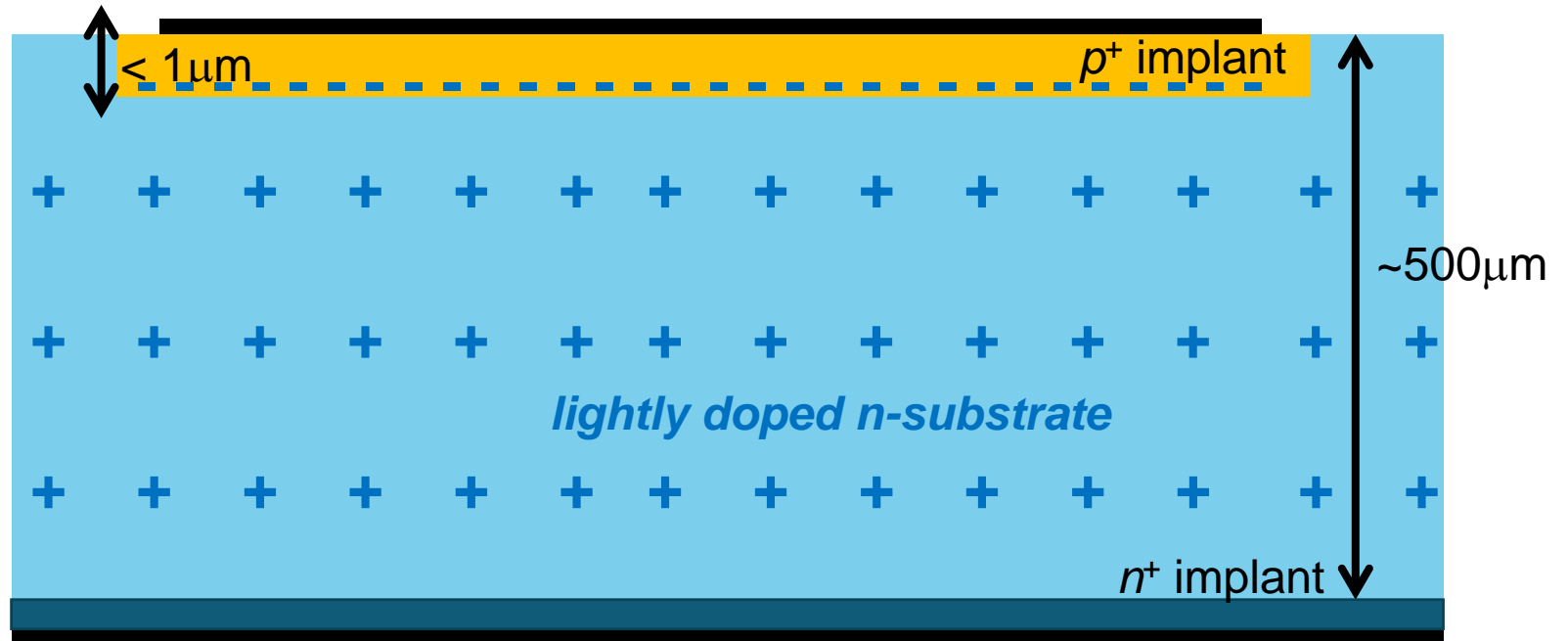
## Diode as a sensor unit

Substrate lightly doped

depletion region =  
substrate thickness

$V_{\text{full-depletion}} \sim 100\text{V}$ ,  
depending on thickness,  
application,...

$E$



# COMPANY FOUNDER

Silicon sensors by planar  
process since 1980

Dr. Josef Kemmer

FOUNDER and SENIOR PRESIDENT  
\* 1938 – † 2007



NUCLEAR INSTRUMENTS AND METHODS 169 (1980) 499-502; © NORTH-HOLLAND PUBLISHING CO.

## FABRICATION OF LOW NOISE SILICON RADIATION DETECTORS BY THE PLANAR PROCESS

J. KEMMER

*Fachbereich Physik der Technischen Universität München, 8046 Garching, Germany*

Received 30 July 1979 and in revised form 22 October 1979

*Dedicated to Prof. Dr. H.-J. Born on the occasion of his 70th birthday*

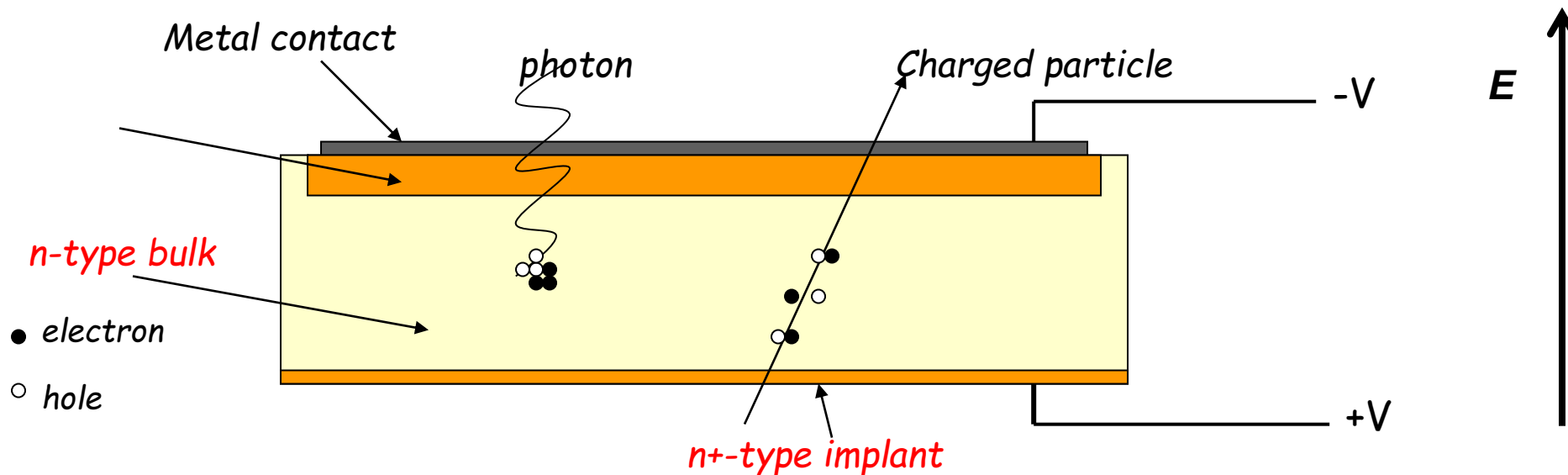
By applying the well known techniques of the planar process: oxide passivation, photo engraving and ion implantation, Si pn-junction detectors were fabricated with leakage currents of less than  $1 \text{ nA cm}^{-2}/100 \mu\text{m}$  at room temperature. Best values for the energy resolution were 10.0 keV for the 5.486 MeV alphas of  $^{241}\text{Am}$  at 22°C using  $5 \times 5 \text{ mm}^2$  detector chips.



## Mechanism of radiation detection

Ionizing radiation (photons or charged particles) creates free electron/hole pairs in the bulk, by releasing energy allowing the electrons in the valence band to hop into the conduction band, leaving a hole behind.

Electrons and holes drift in opposite directions, following the electric field lines. While this drift occurs, current pulses are generated at the electrodes.



# The Ramo theorem

Proceedings of the IRE, September 1939, page 584.

## Currents Induced by Electron Motion\*

SIMON RAMO†, ASSOCIATE MEMBER, I.R.E.

*Summary*—A method is given for computing the instantaneous current induced in neighboring conductors by a given specified motion of electrons. The method is based on the repeated use of a simple equation giving the current due to a single electron's movement and is believed to be simpler than methods previously described.

### INTRODUCTION

IN designing vacuum tubes in which electron transit-time is relatively long, it becomes necessary to discard the low-frequency concept that the instantaneous current taken by any electrode is proportional to the number of electrons received by



### METHOD OF COMPUTATION

The method is based on the following equation, whose derivation is given later:

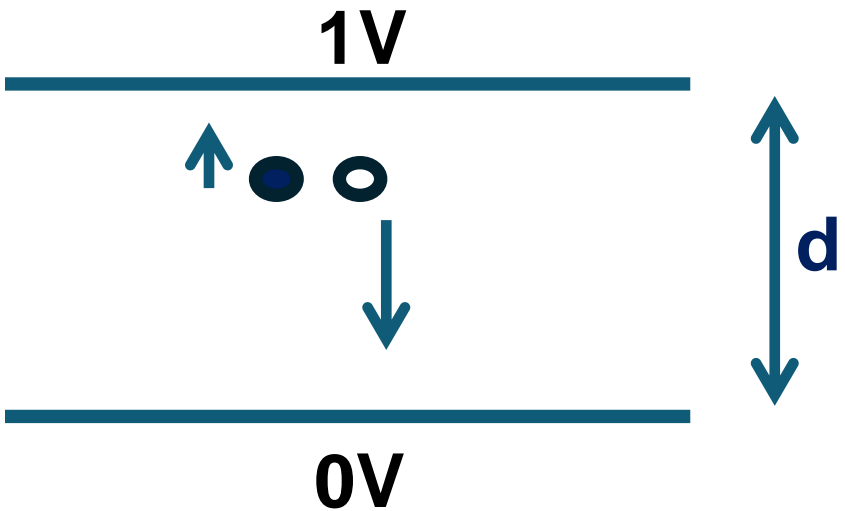
$$i = E_v ev \quad (1)$$

where  $i$  is the instantaneous current received by the given electrode due to a single electron's motion,  $e$  is the charge on the electron,  $v$  is its instantaneous velocity, and  $E_v$  is the component in the direction  $v$  of that electric field which would exist at the electron's instantaneous position under the following circumstances: electron removed, given electrode raised to unit potential, all other conductors grounded. The equation involves the usual assumption

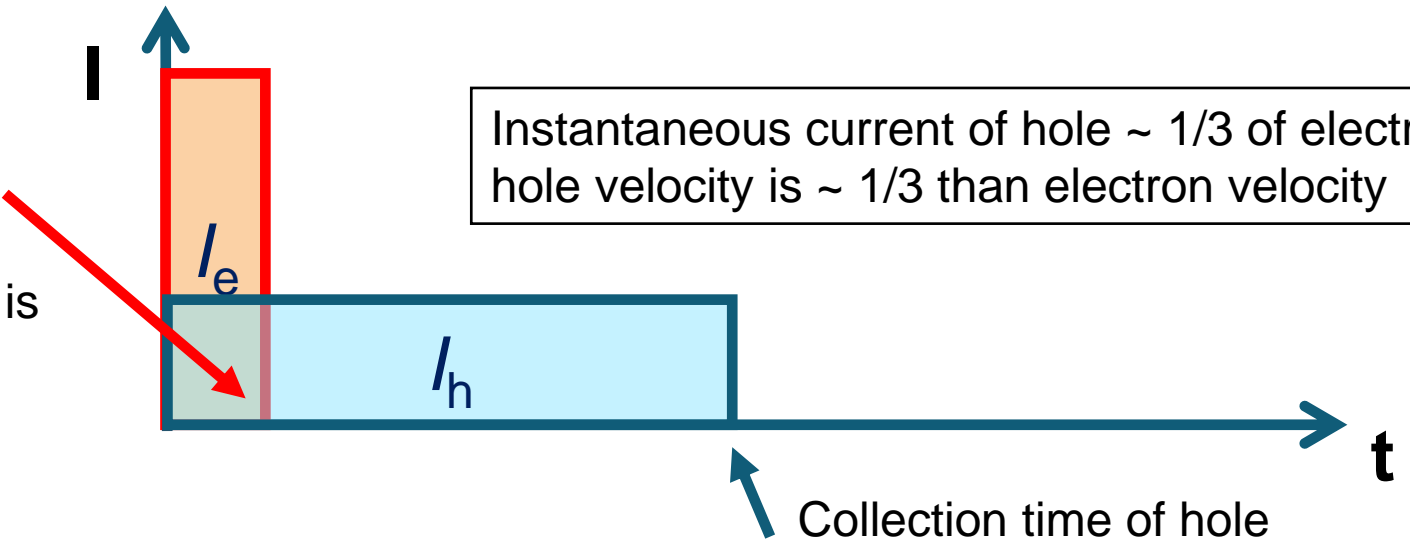
- Currents induced at the electrodes when charges are moving (no charge movement → no current)
- Concept of “weighting field”, units of an electric field but **it is not the electric field!!!!**

# Example: 1D diode

- Weighting field,  $\mathbf{W} = 1/d$  (V/cm)
- Electric field,  $\mathbf{E} \sim V/d$  (V/cm) (defines  $\mathbf{v}_e$ ,  $\mathbf{v}_h$ )
- If the electron drifts up with velocity  $v_e$ 
  - $I_e = -q v_e W$
- If the hole drifts down with velocity  $v_h$ 
  - $I_h = -q v_h W$



Collection time of electron. Pair is produced close to n-terminal, so signal of electron is smaller

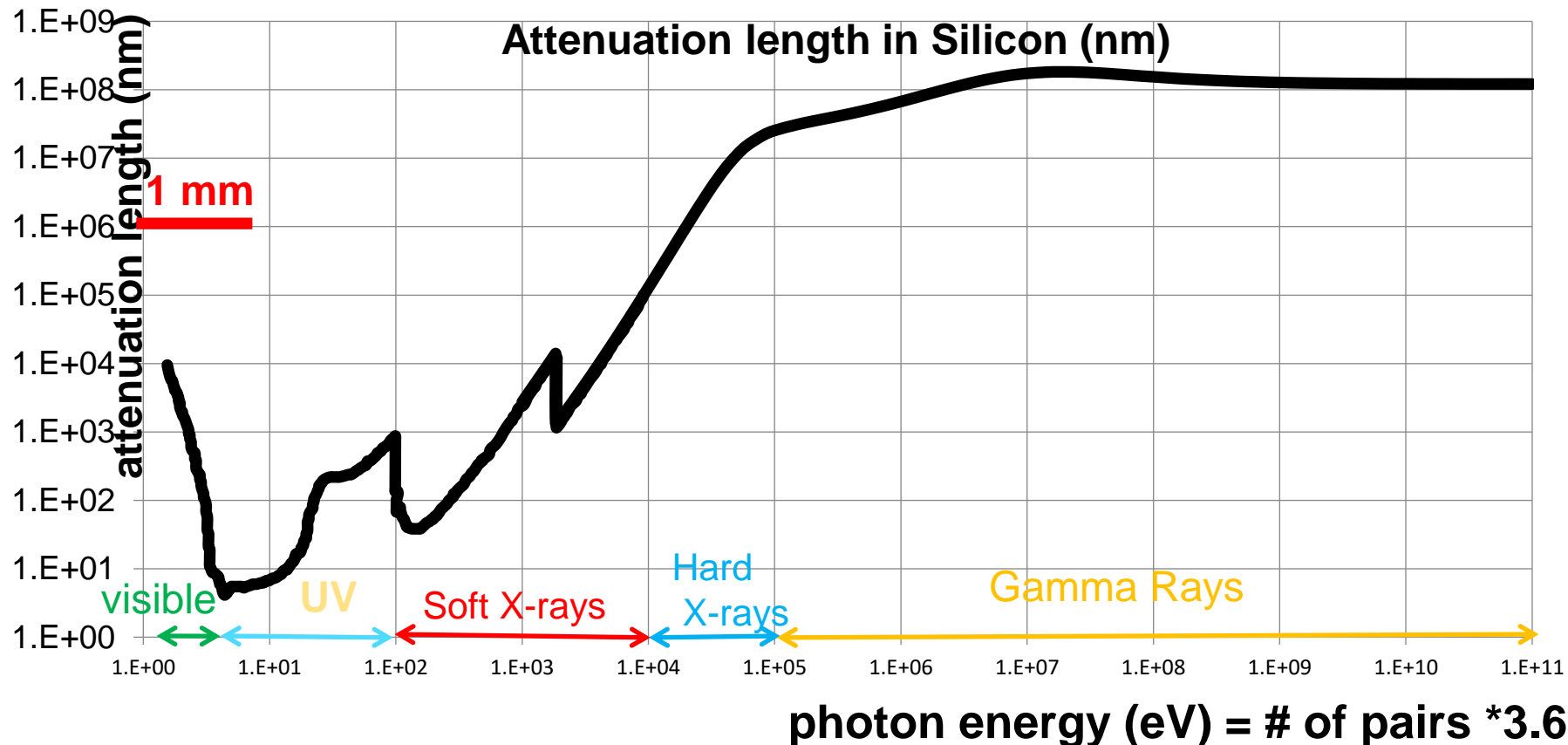


Instantaneous current of hole ~ 1/3 of electrons as hole velocity is ~ 1/3 than electron velocity



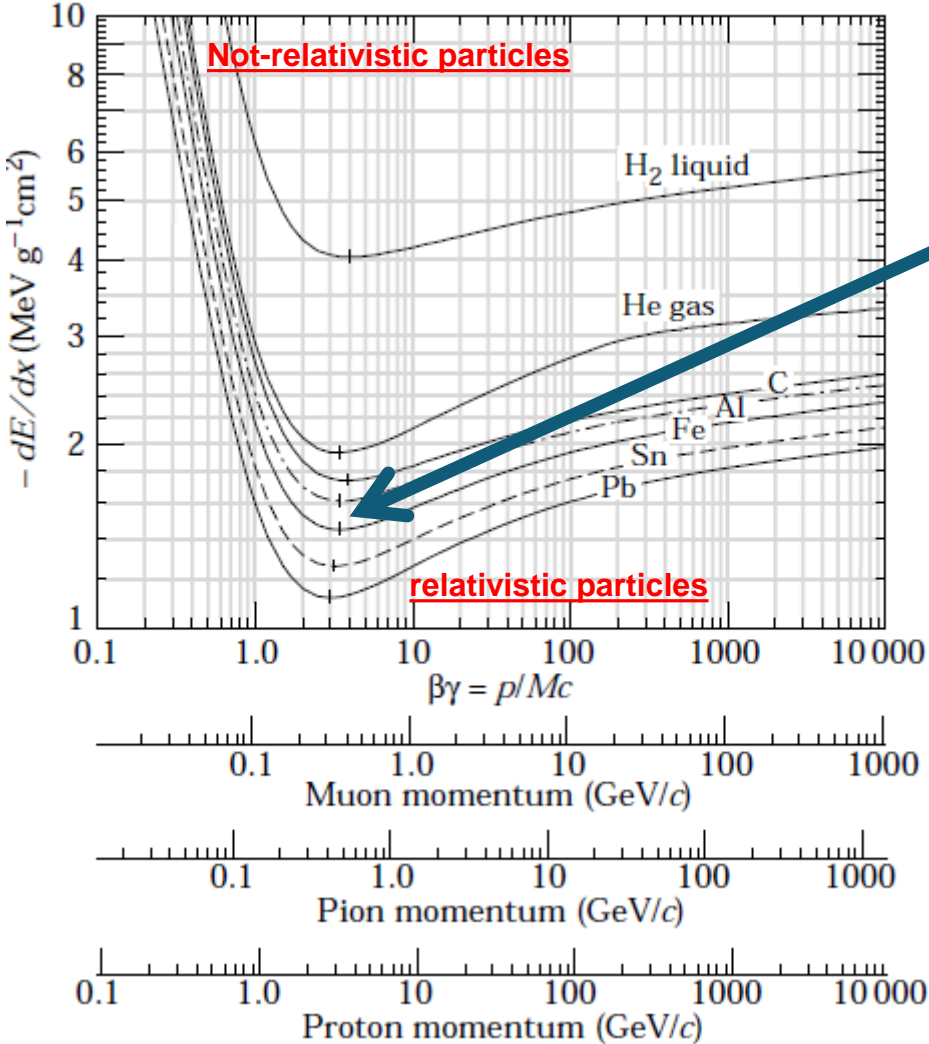
# Absorption of photons in Silicon

If  $N_0$  photons enter the silicon, after a distance  $L$ , the number of photons which have not been absorbed by silicon is:  $N = N_0 \exp(-L/l)$ , where  $l$  is the attenuation length



- Silicon detects with good efficiency above 20 eV and below 20 keV
- Visible photons create just one couple  $e^-/h^+$

# Interaction of charged particles with silicon: the Bethe Block formula

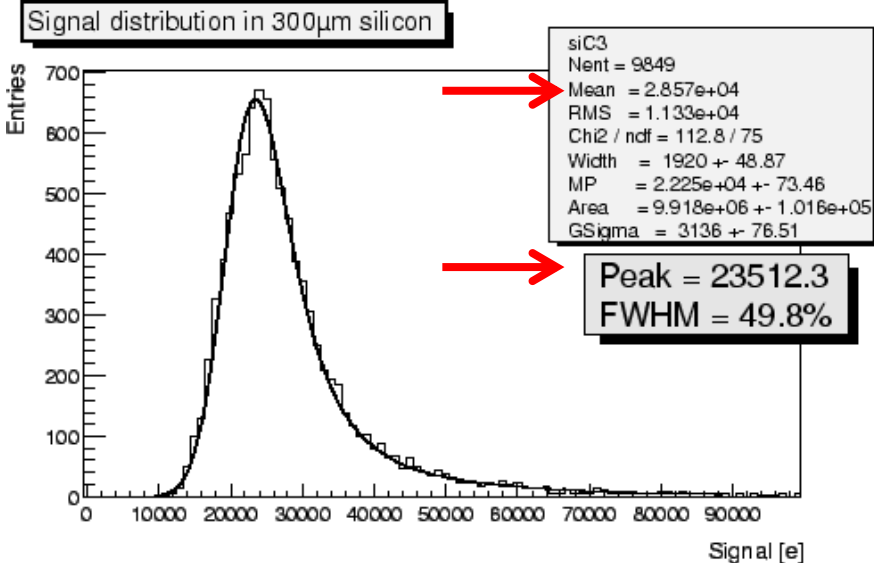


In most practical cases,

**we are here**

i.e. at the minimum of energy loss.  
Still, a **m.i.p.** (minimum ionizing particle) produces 80 pairs/ $\mu\text{m}$  in Silicon (for 300  $\mu\text{m}$   $\rightarrow$  24k electrons)

## Landau distribution



# End of Part 1

# Questions?

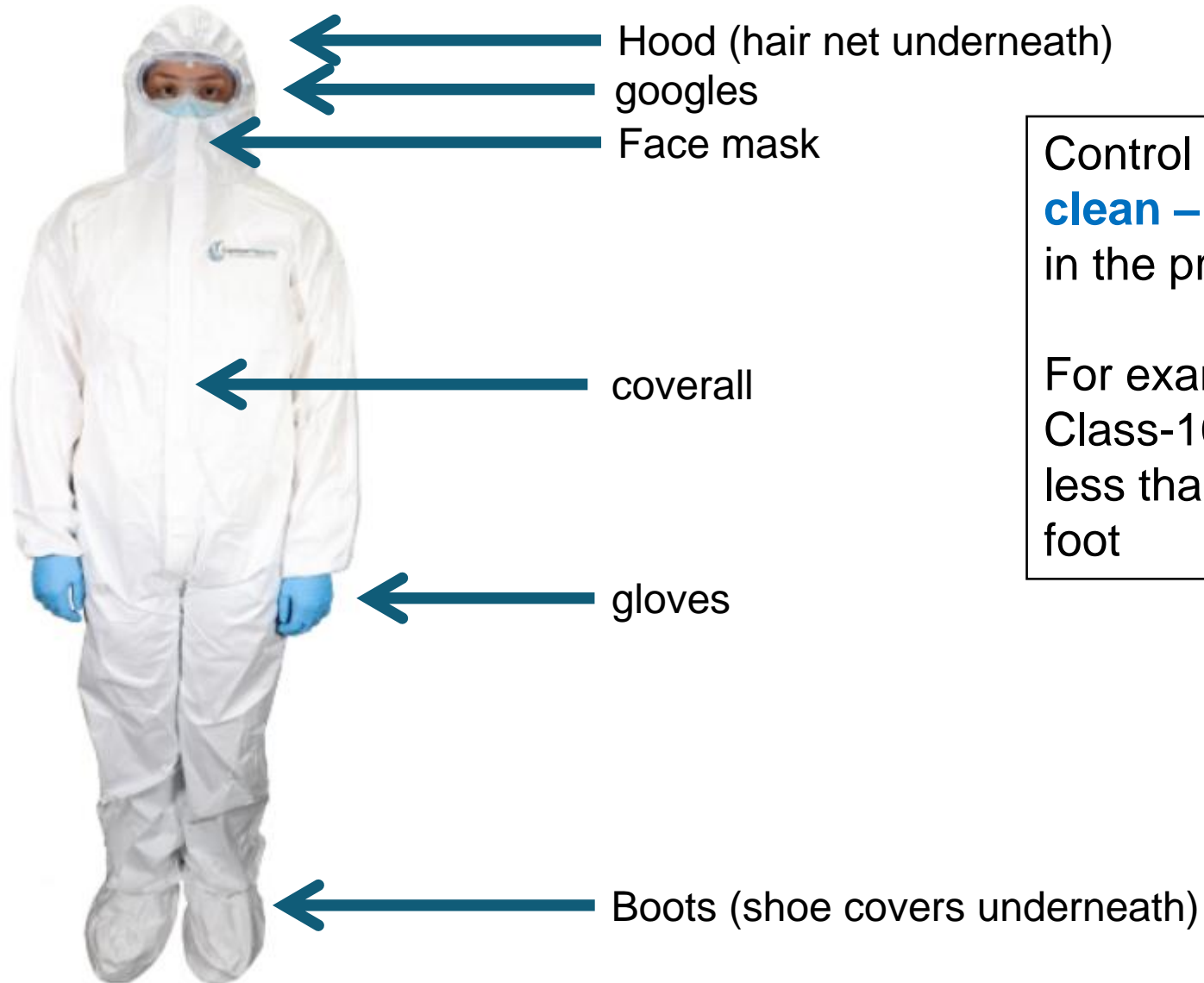


# BACK UP

# Fabrication:

## let's make a diode

## Before starting: dress up properly!!!



Control of dust particles in the **clean – room** prevents defects in the process

For example:  
Class-100 Clean room means less than 100 particles/cubic foot

# Oxidation

Chemical reaction ...

Growth of pure high-quality silicon oxide films ranging in thickness from 100 angstroms to 1 micron.

Temperature from 200C to 1100C.

Nitrogen annealings also.

Quartz boats on cantilever arm host the wafers.






# Oxidation

**Initial wafer**



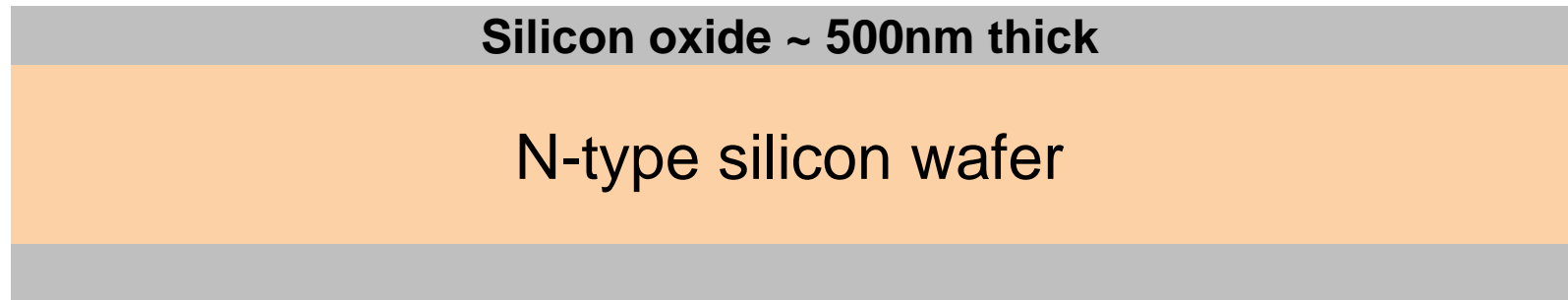
300um  
thick



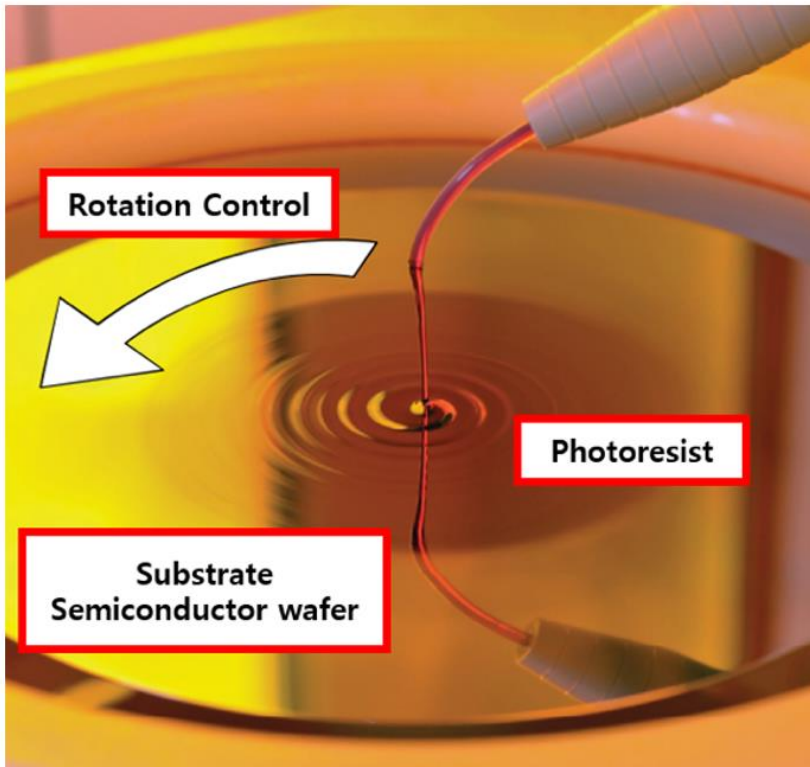
A vertical double-headed arrow indicating the thickness of the wafer.



**oxidation**



# Lithography



Photoresist is spun on the wafer

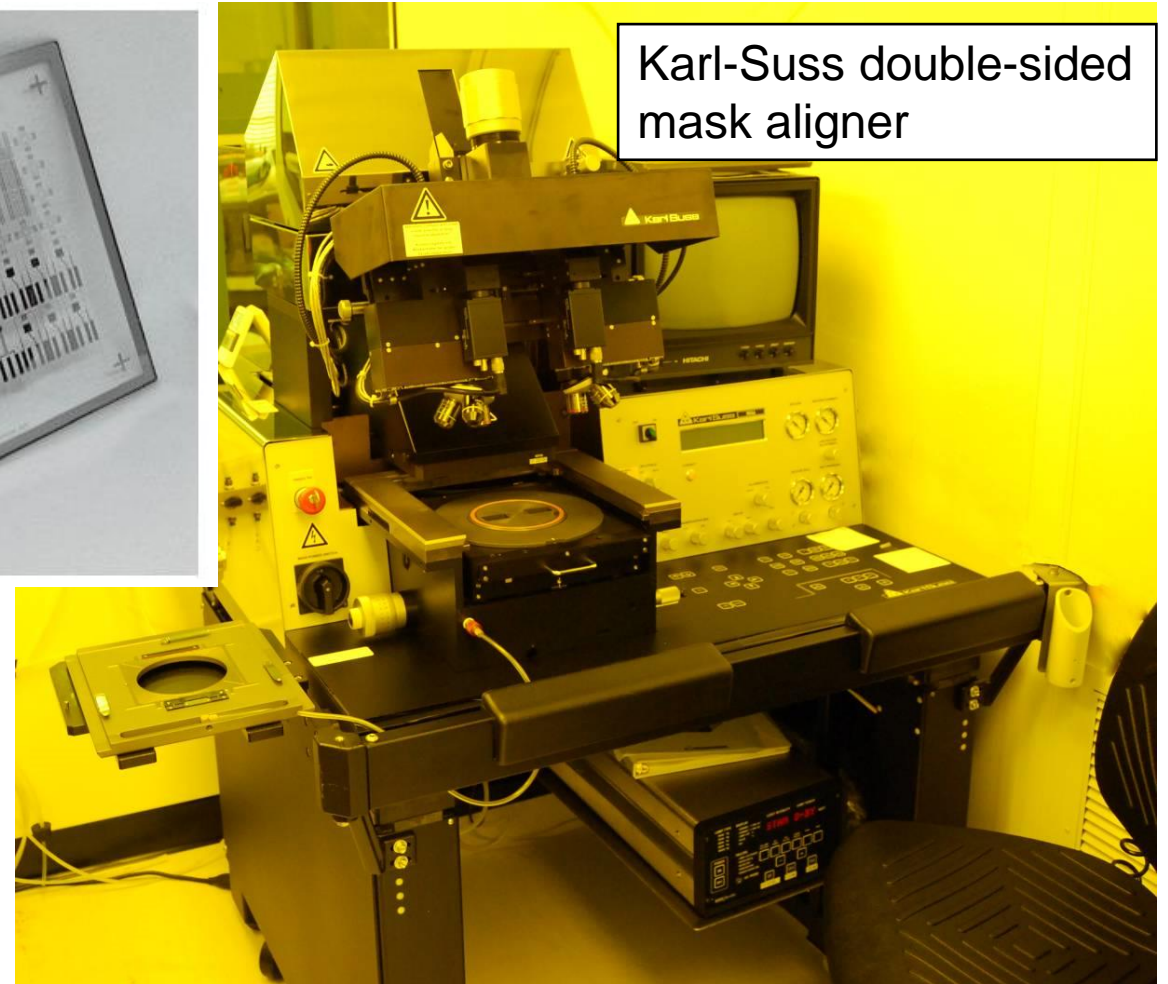
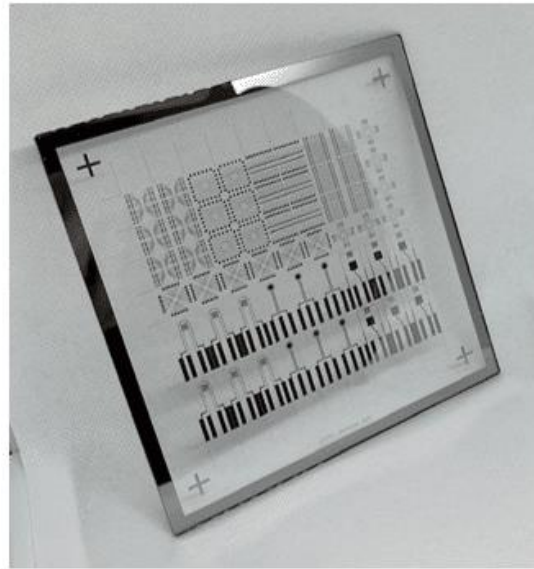
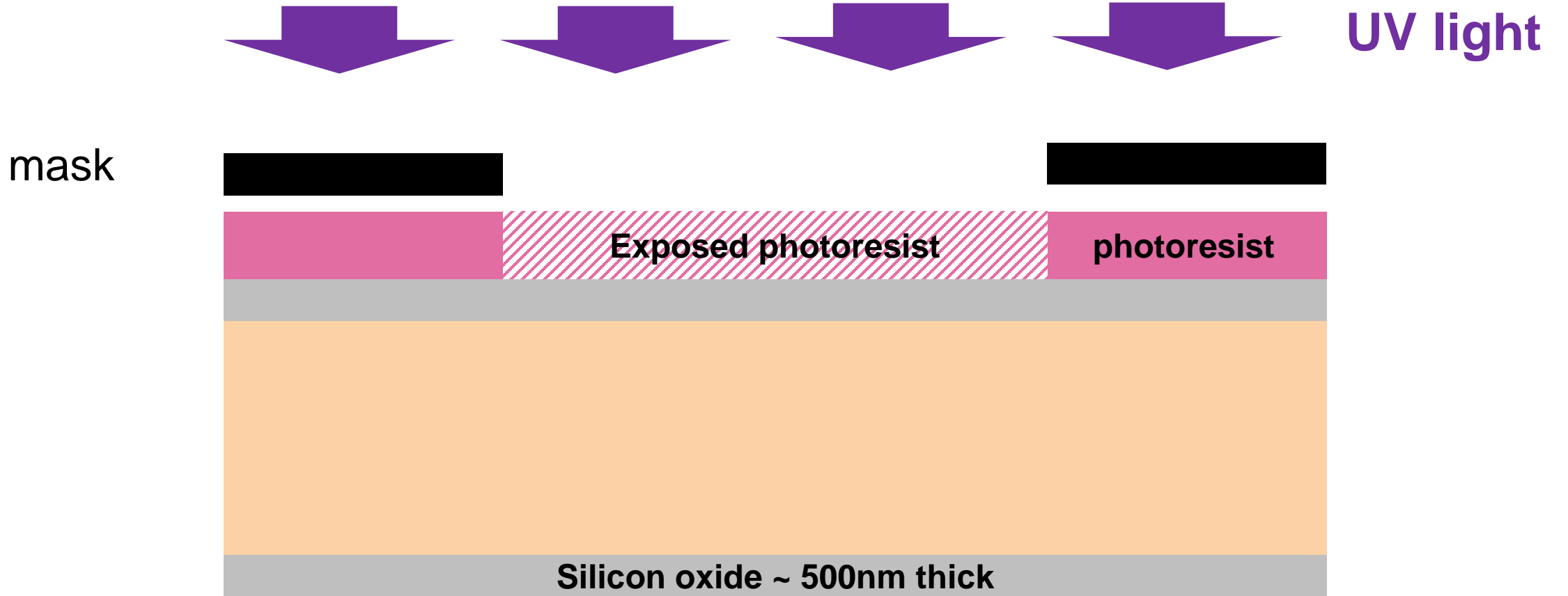


Image (layer) is on a photomask (glass with pattern in chrome), which is placed on the wafer and a UV light shines through the glass, exposing the photoresist.

# lithography



## Resist Development

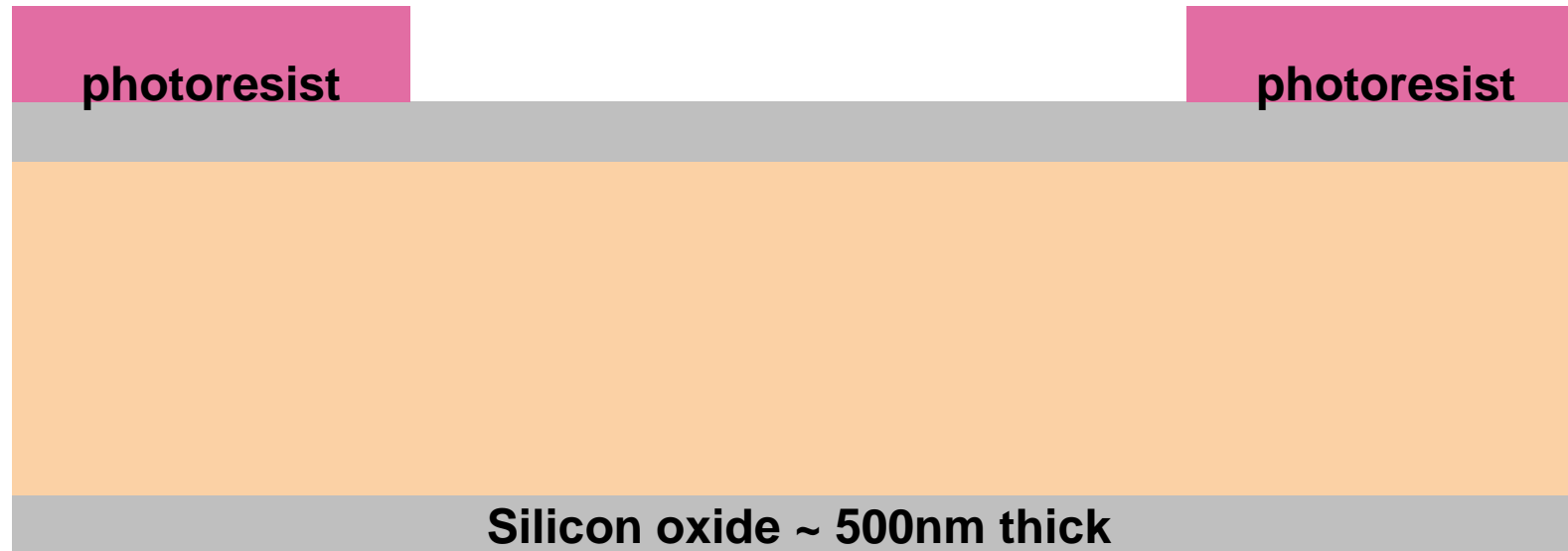
Developing solution is sprayed on the wafers, to get rid of the exposed photoresist.  
Wafer is then rinsed in DI and dried.





# Resist Development

Image is transferred from photolithographic mask to the resist covering the wafer.



# Etching

## Wet etch

- Very selective
  - HF for silicon oxide
  - HNO for polysilicon
  - Alu etch for aluminum
  - ...
- Unexpensive
- Unbreakable
- Very clean



## Dry etch

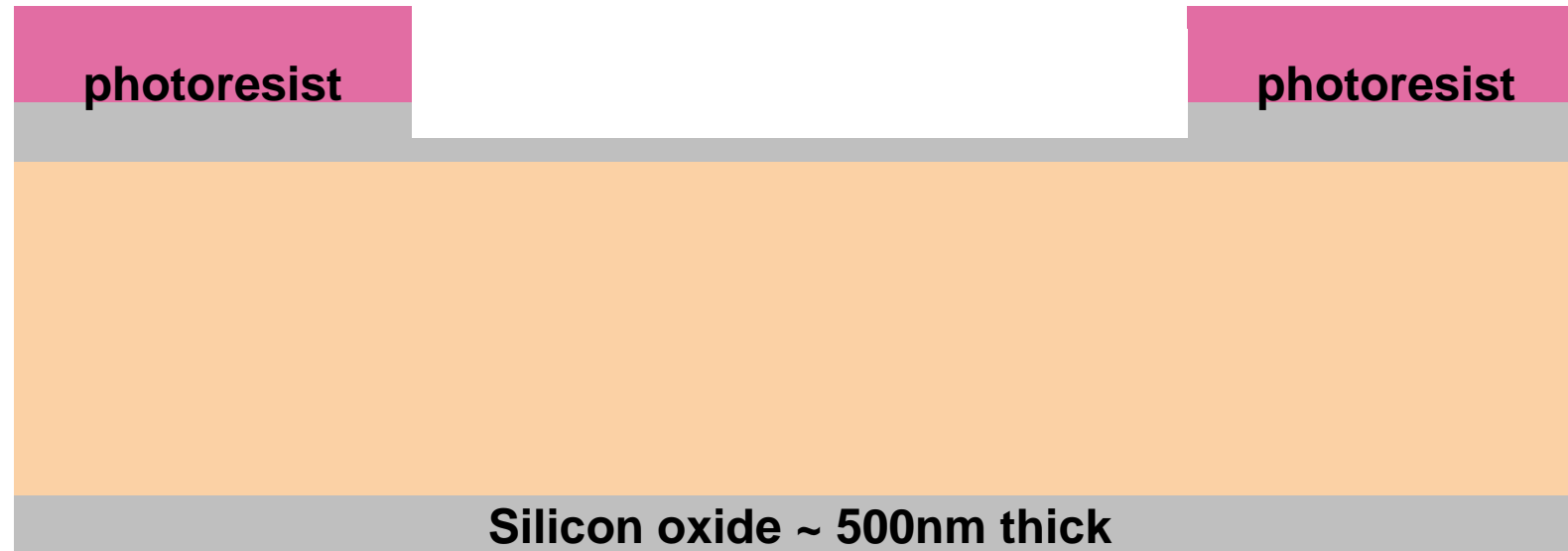


Wafers exposed to a gas in an RF field

# Etching

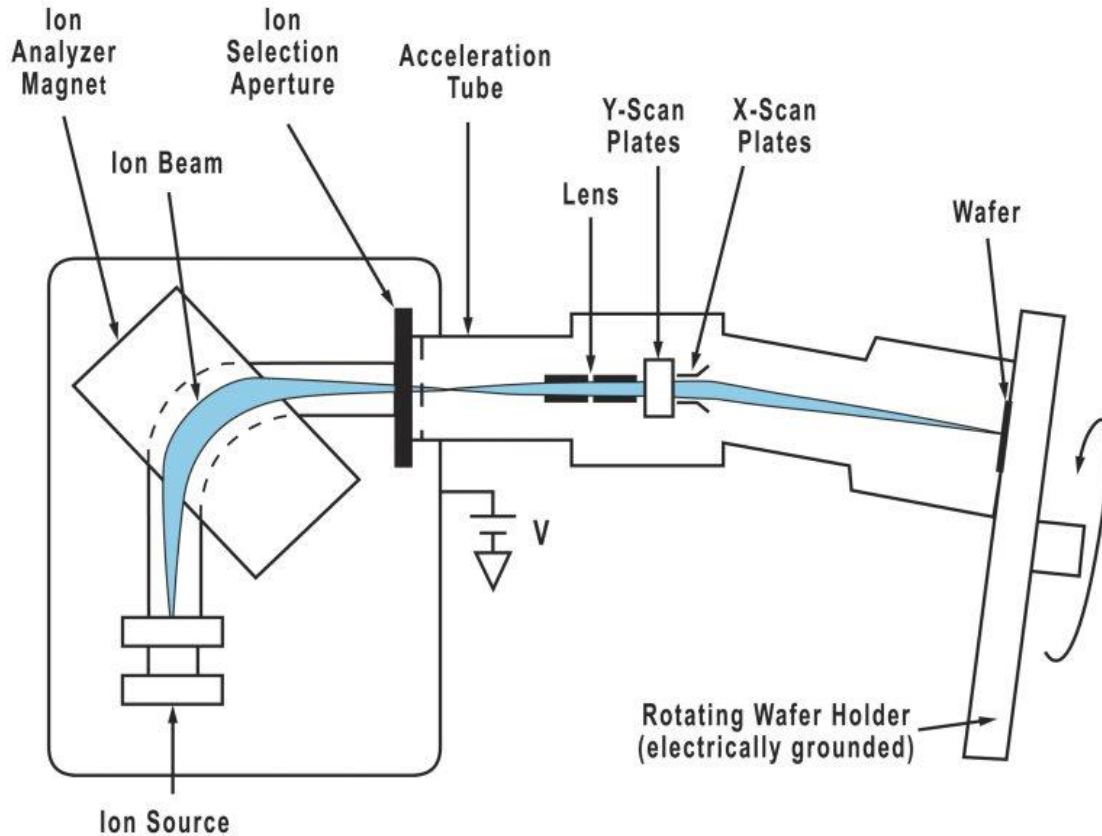
Photoresist “resists” acid attacks and RIE attacks (for some time).

In this example, oxide is thinned down.



# Ion Implantation

## Insertion of doping in silicon

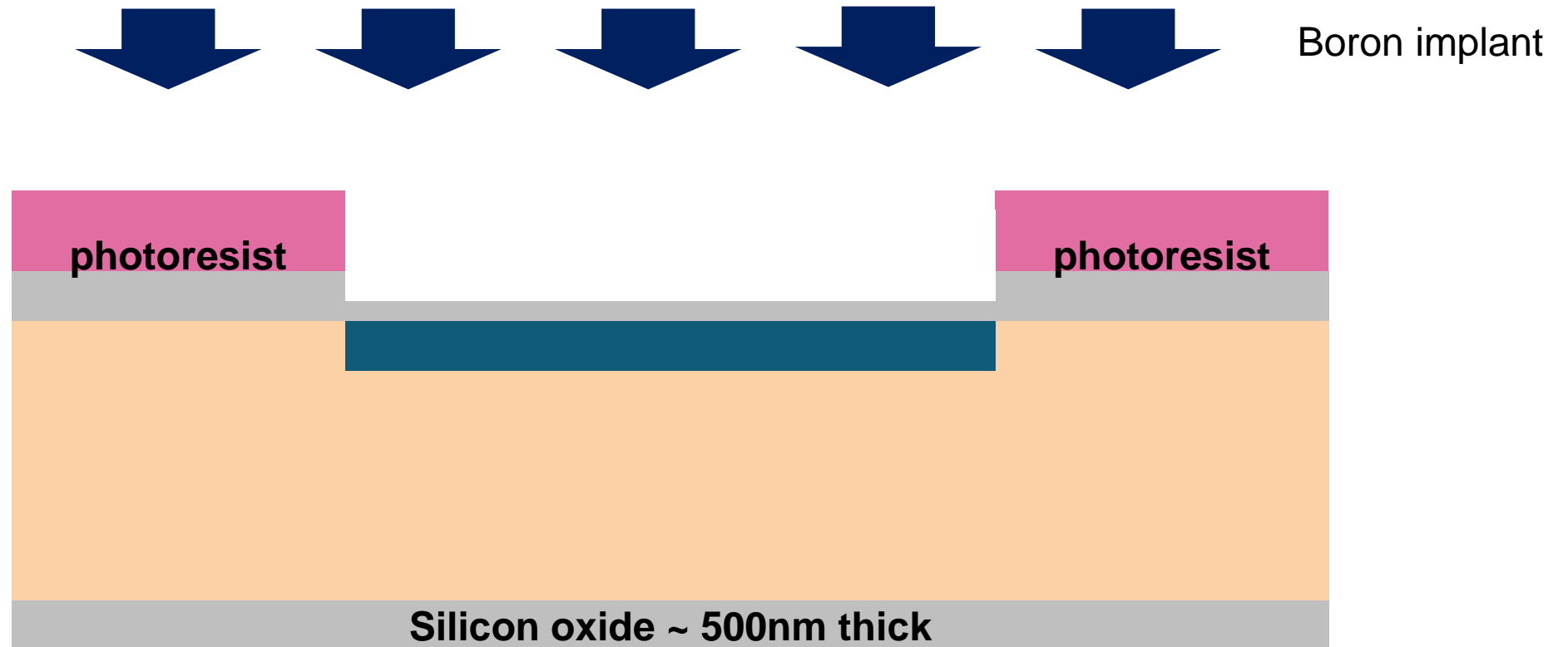


An Ion implanter is an accelerator, it requires a medium facility and fabrication volume to justify the cost. Often outsourced.

Tandem van Der Graaff @ BNL can be used as a (high energy) ion implanter as well!



# Ion Implantation



Resist stops the implant (also oxide does, so energy must be calibrated)

# Resist strip

## Wet method:

- stripper
- Piranha etch (Caro etch): sulfuric acid and hydrogen peroxide at  $> 100\text{C}$

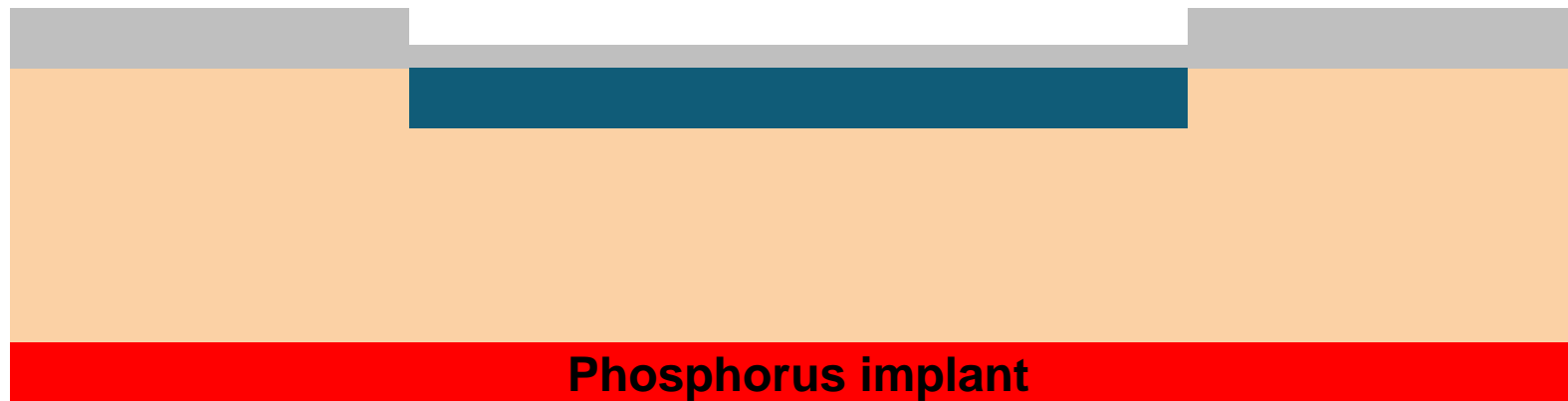
**Dry method:**  
ashing in oxygen plasma



# Resist stripping



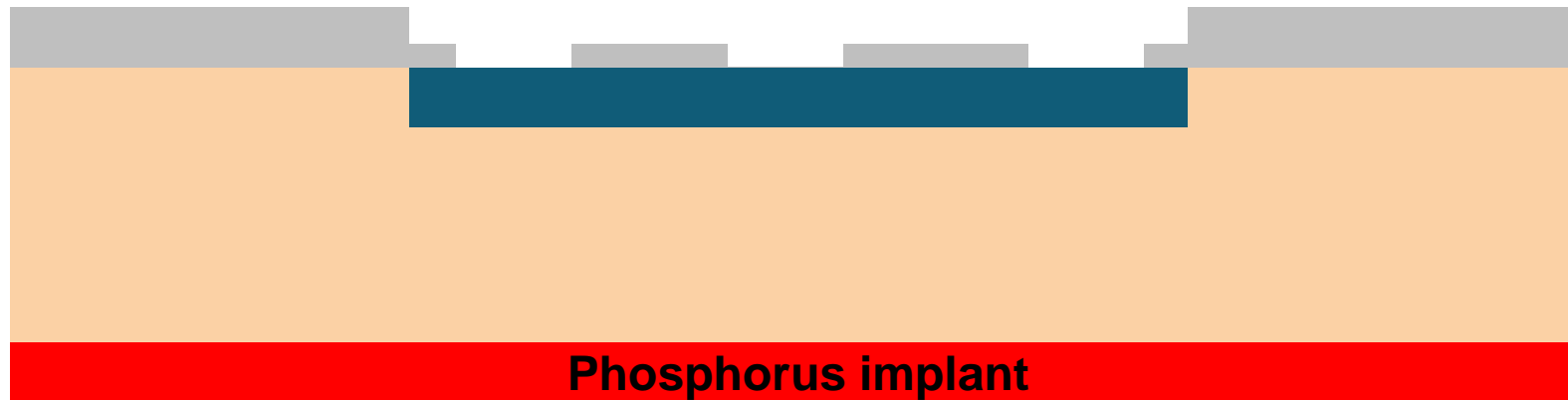
Ion implantation on the back of the wafer as well, same type as the substrate for a good ohmic contact



# Contact opening

Another lithographic step is required:

1. resist spinning,
2. photolithographic mask exposure,
3. etching to expose the silicon
4. resist stripping





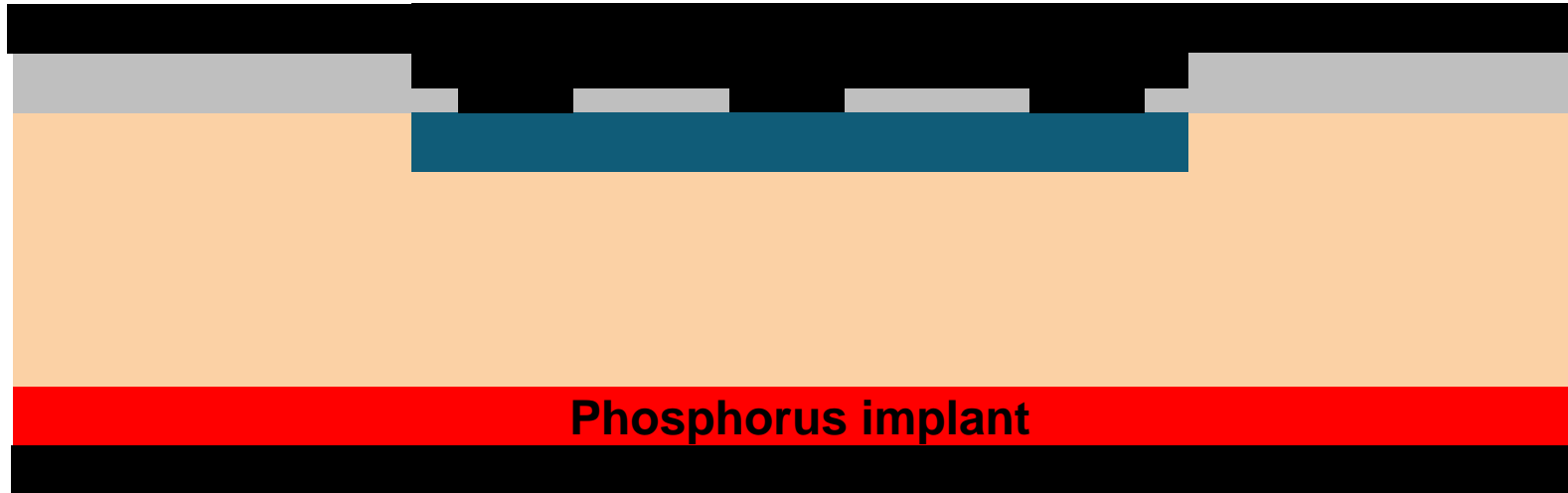
# Metal sputtering

- RF Sputtering System for high purity Aluminum/Titanium Metallization
- Ion Gun for removal of native oxide in Double metal applications

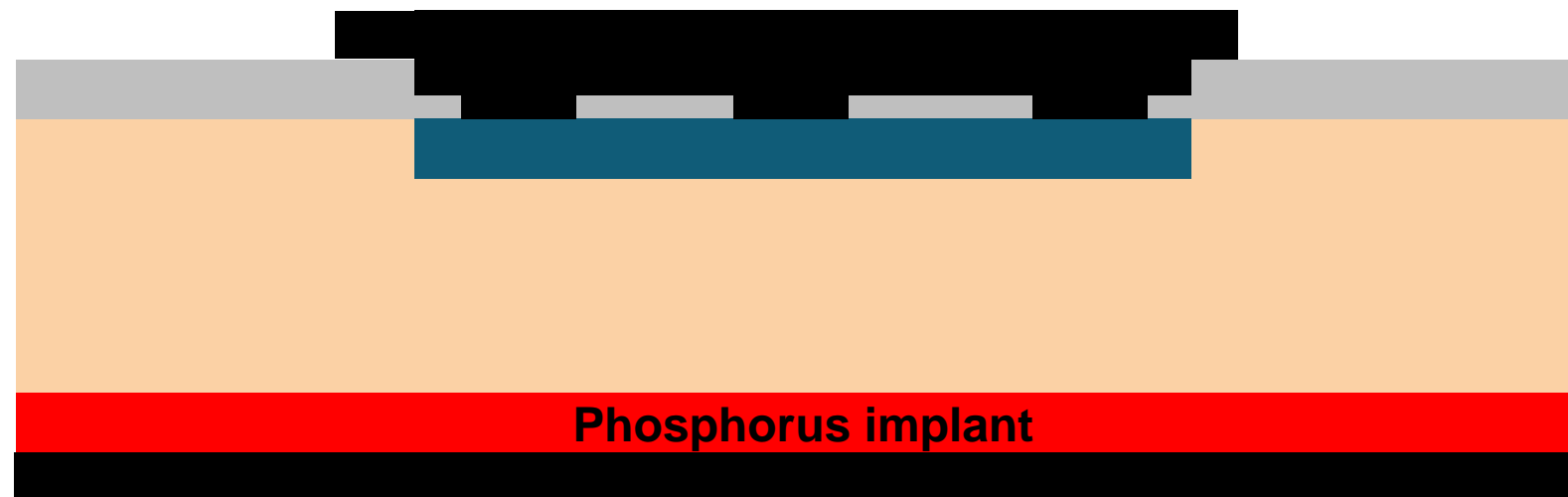


*Lesker sputtering system*

## Metal sputtering (both sides)



## Metal definition (lithography) – wet or dry



# Thin-Film deposition

Aluminum melts at 400C, so no more furnaces after its deposition.

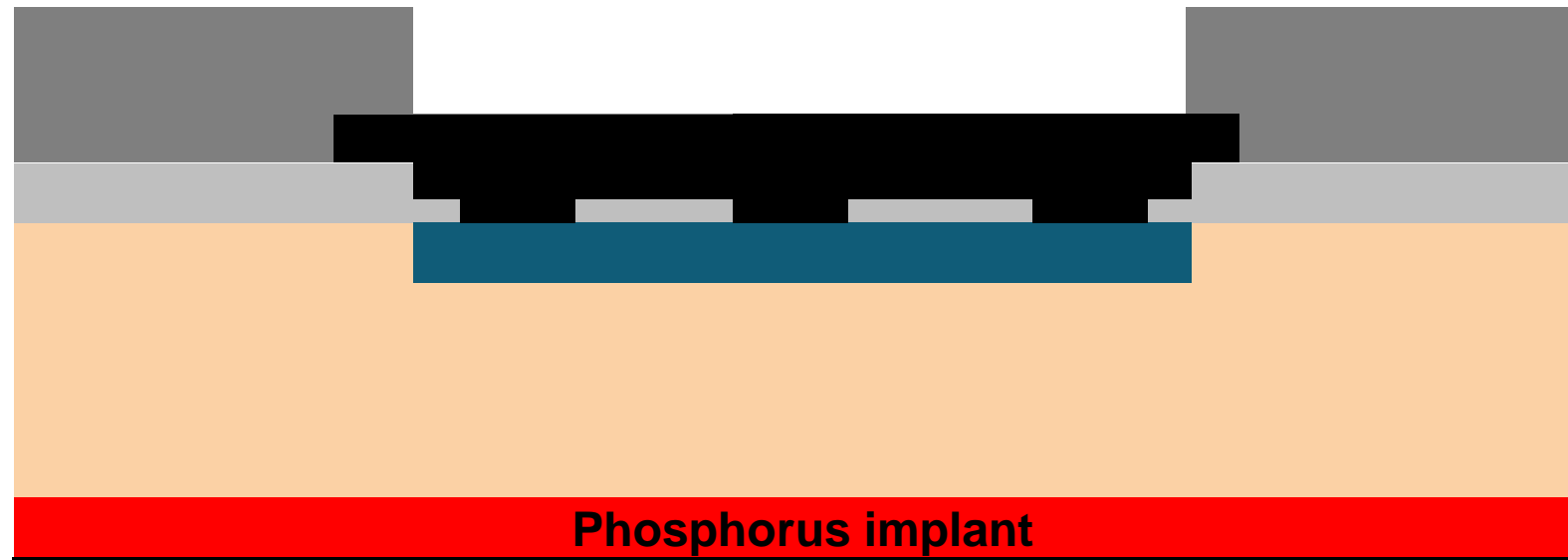
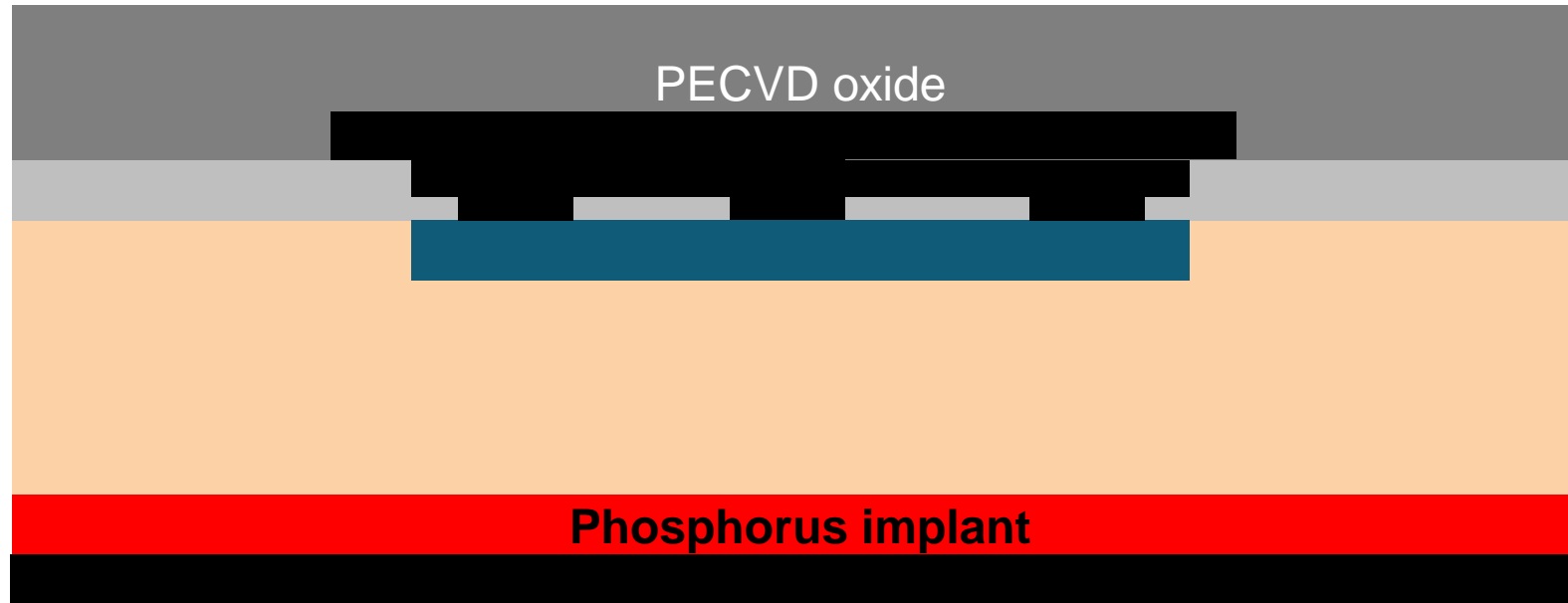
We may want to add some thin film as anti-scratch layer (passivation).

This can be done by PECVD deposition (plasma chamber) or LPCVD (low-temperature furnace).

Nitrides and oxides are usually deposited.

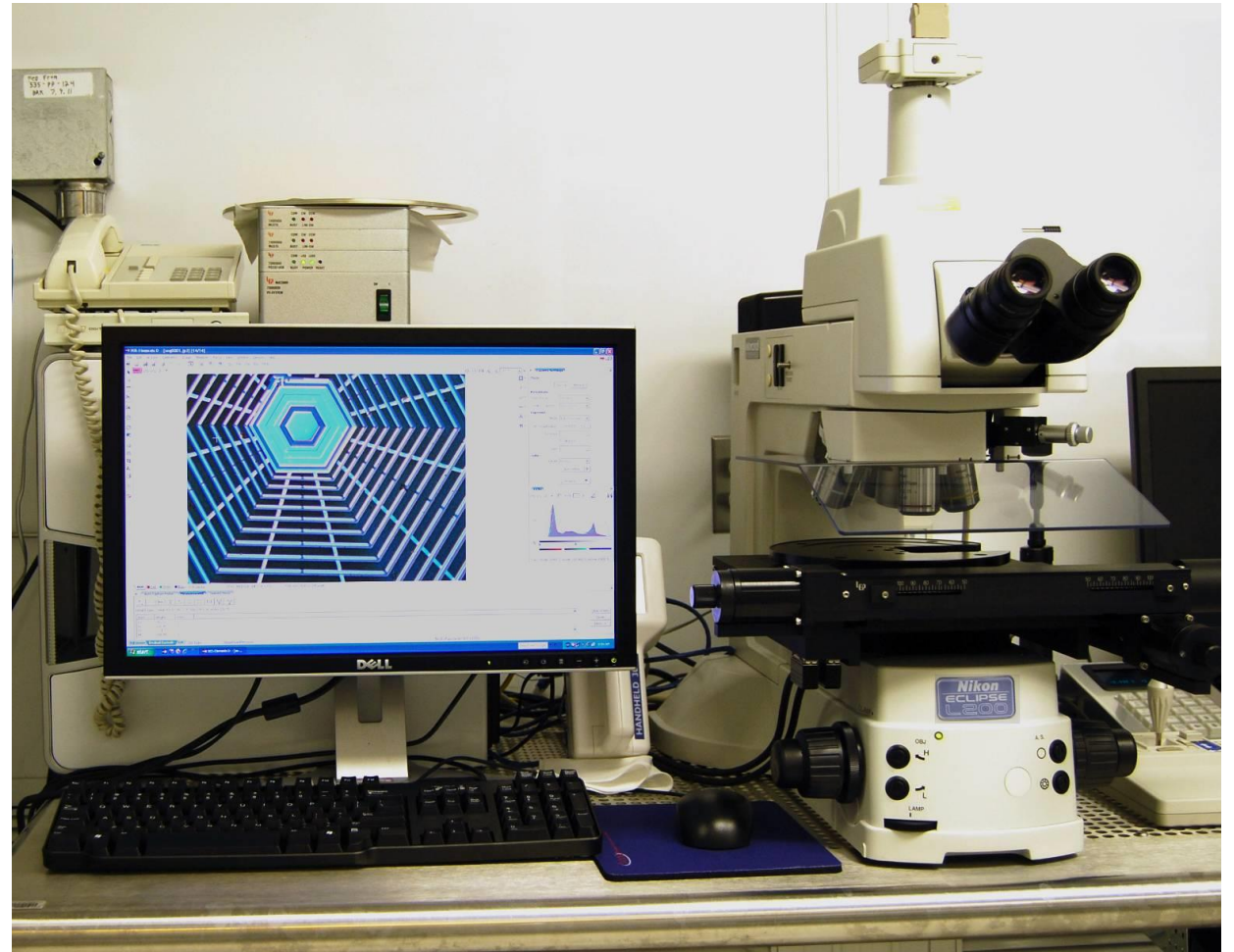


# Passivation deposition and opening



# Wafer Inspection

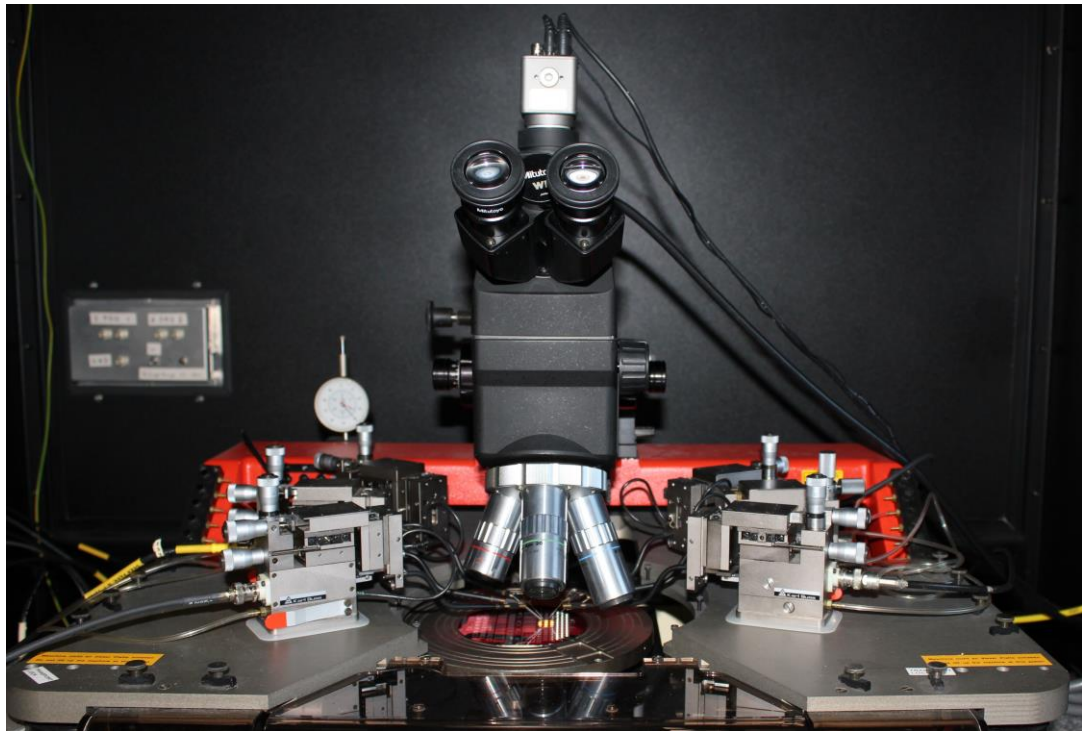
- Following every process step, each wafer needs to be methodically inspected for potential defects
- FILMETRICS<sup>®</sup> for thin-film thickness measurement
- Ellipsometer for  $n$  and thickness





# Testing

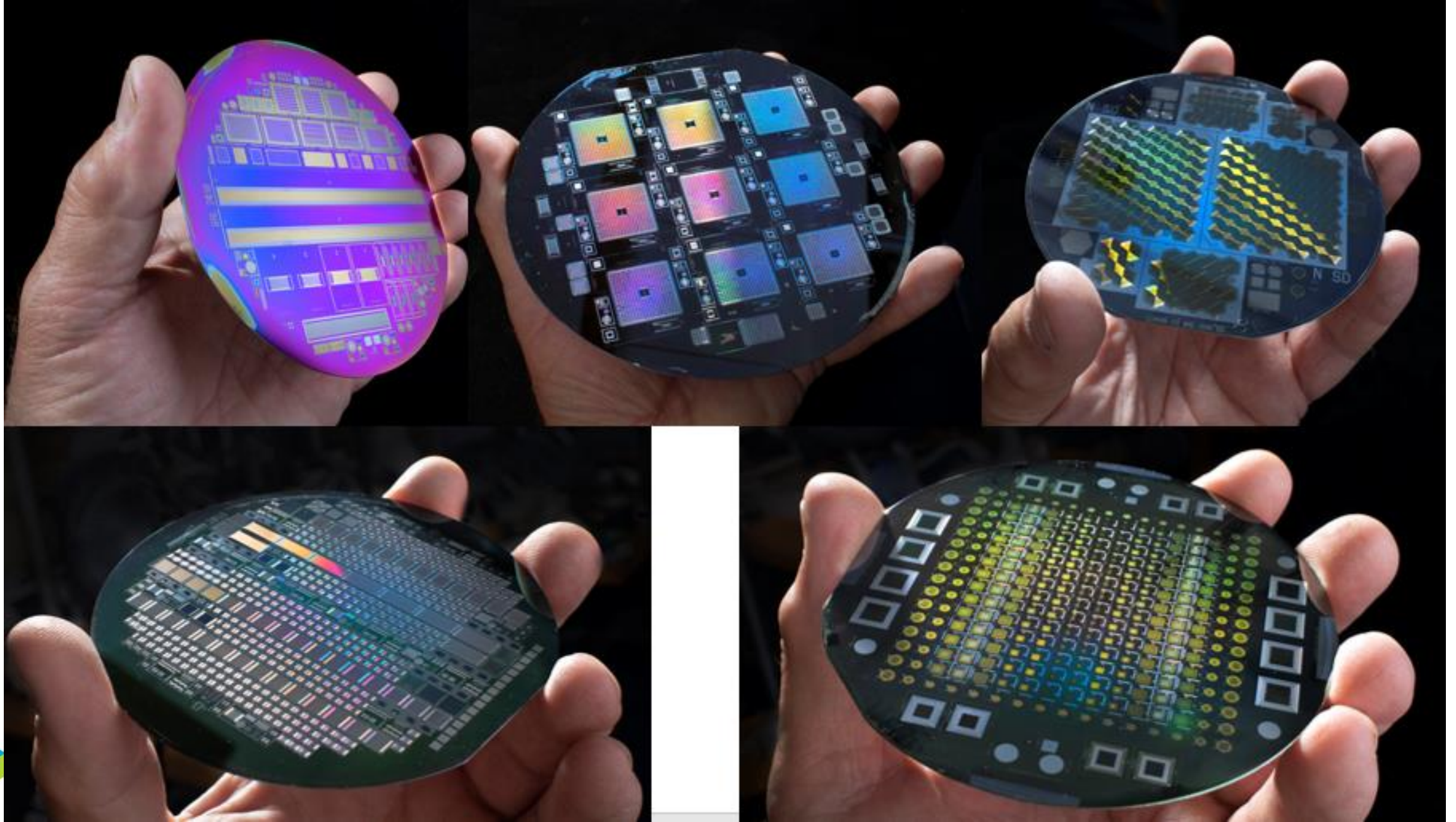
BNL manual probe station



Automatic probe station for volume productions



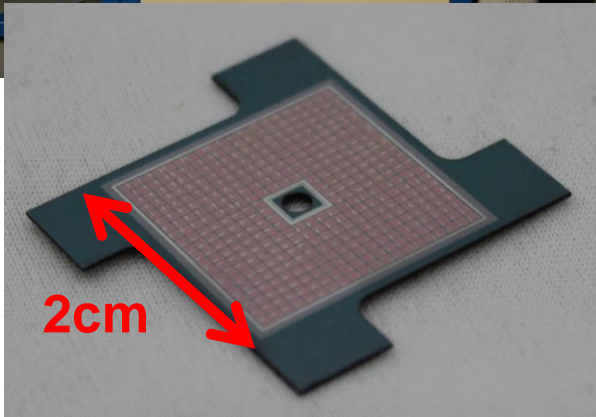
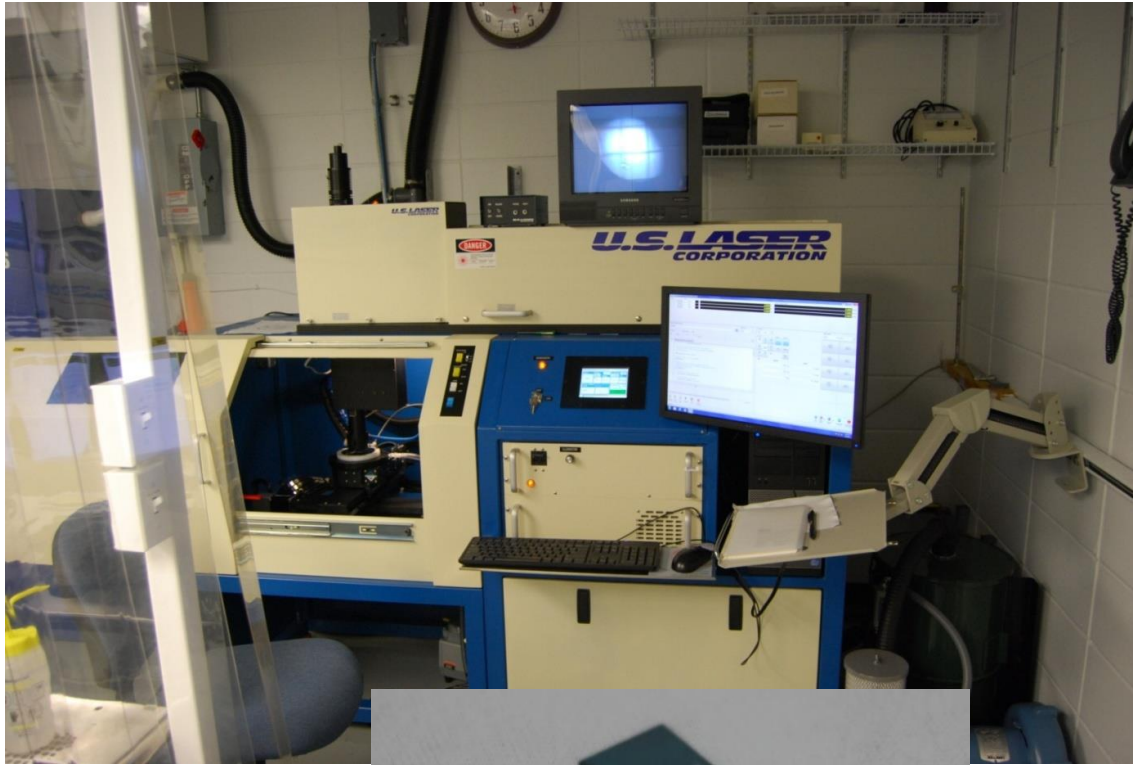
# The final wafer





# Dicing Systems

BNL laser dicing  
(allows arbitrary shapes, not only straight cuts)



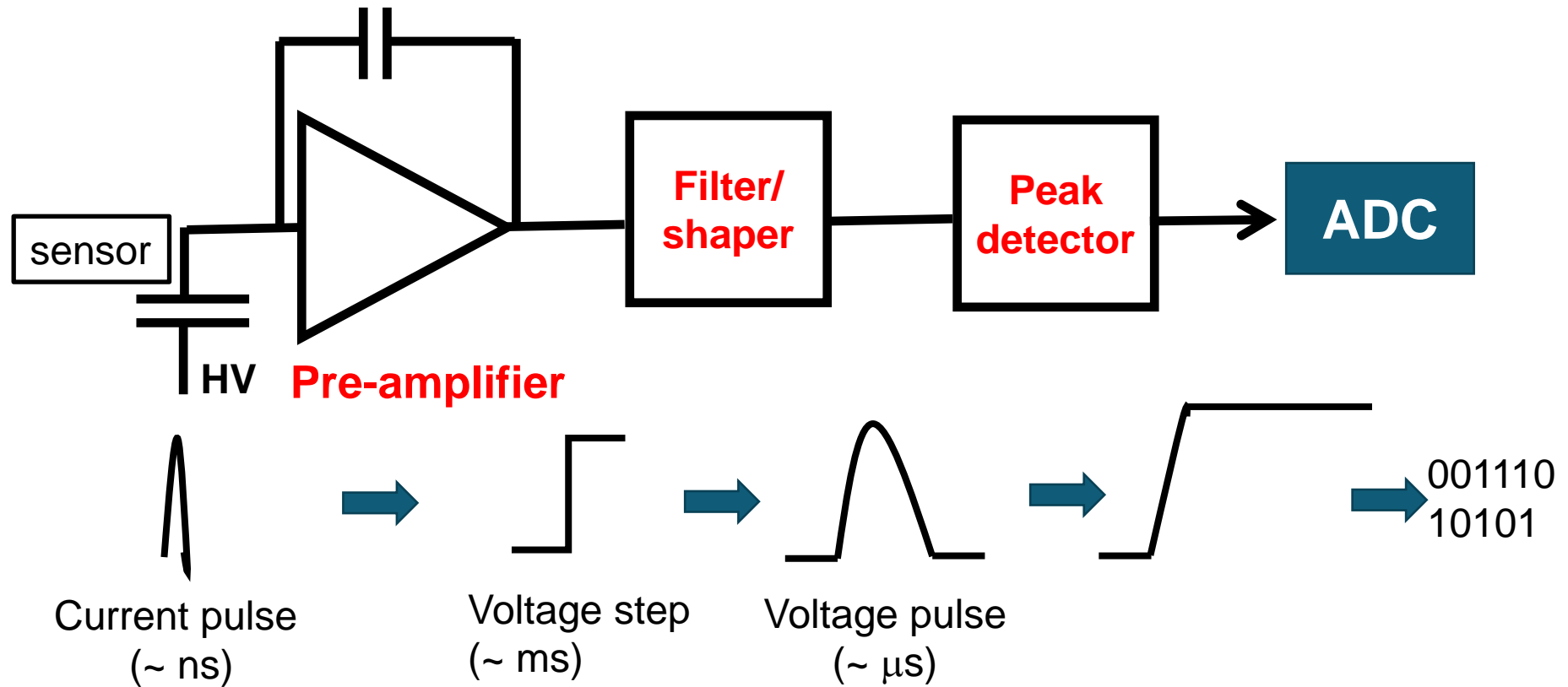
Disco © saw dicing



## More manual dicing systems



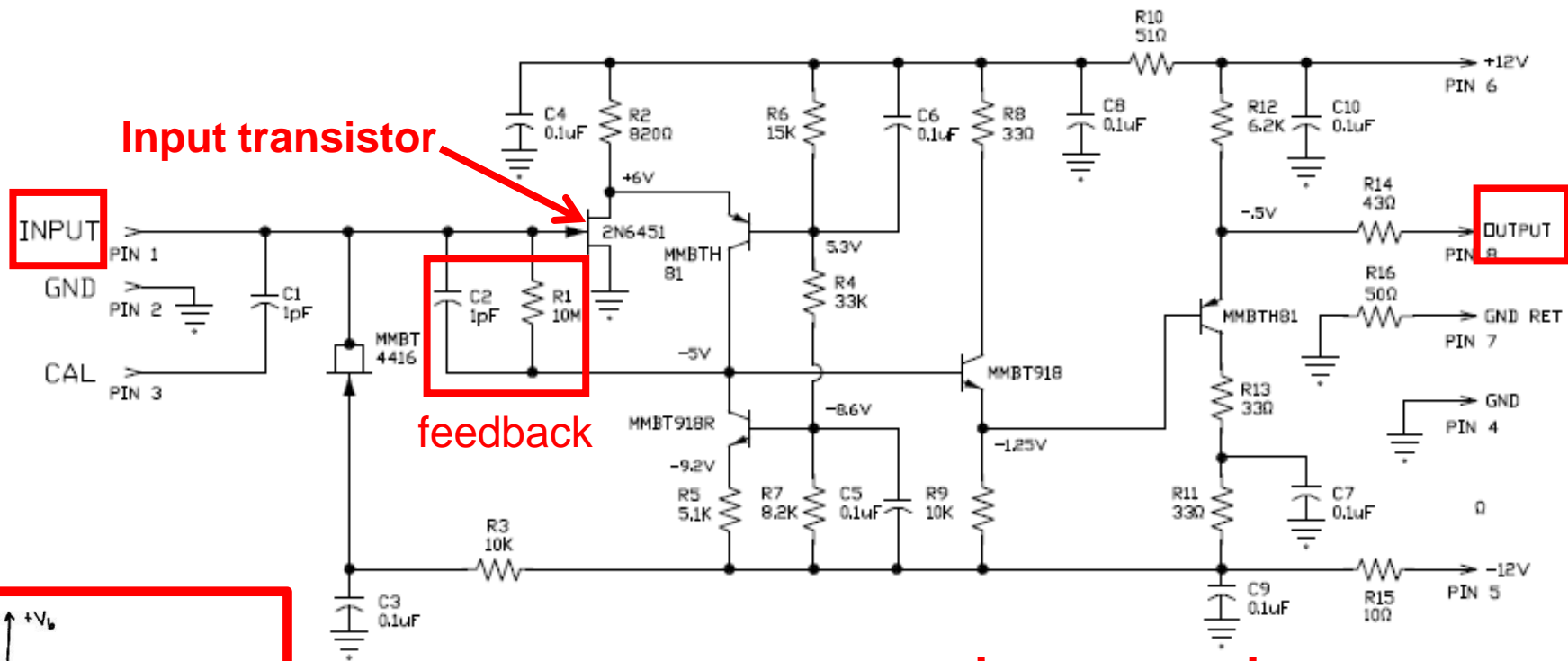
## (very basic) Read-out chain



- Can be made by separate blocks
- Modern trend: integrate everything in an IC (especially if # of channels is high)  
ASIC: Application Specific Integrated Circuit, designed in house but fabricated in TSMC, IBM, AMS, ST, ...



# Charge Sensitive Pre-Amplifier



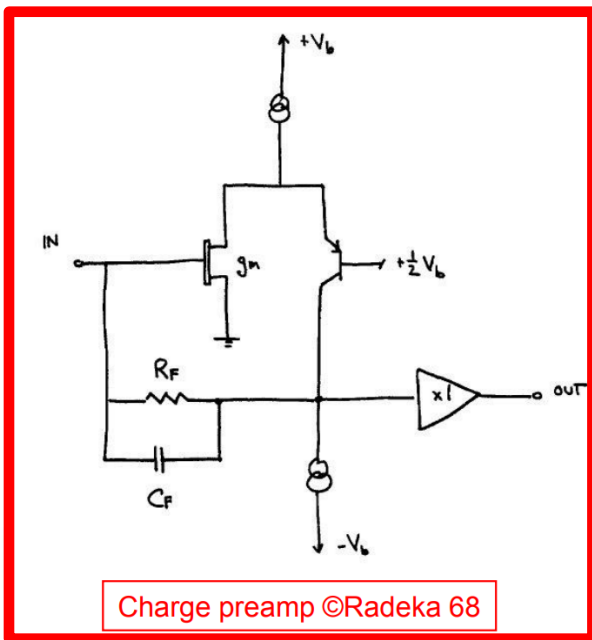
Input transistor

INPUT

feedback

OUTPUT

Double source-follower stage



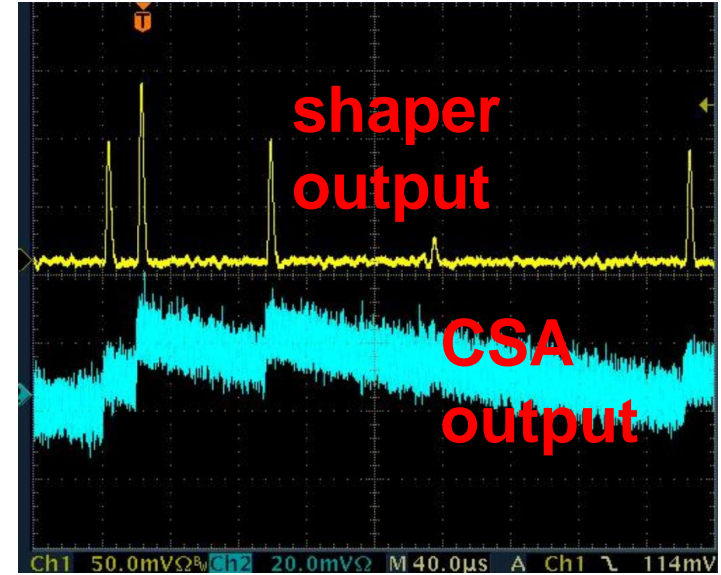
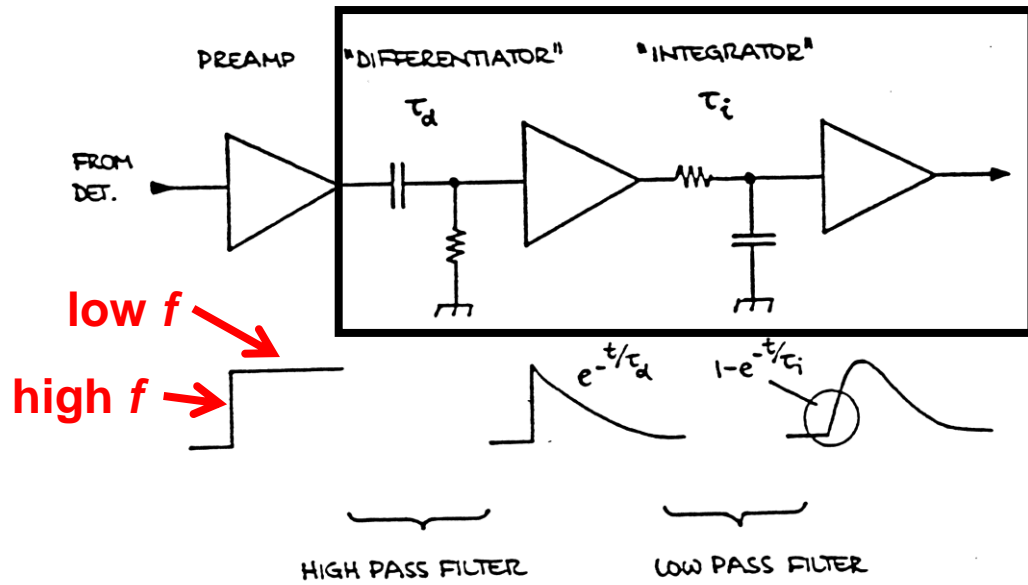
Charge preamp ©Radeka 68



The common trend is to fabricate the CSA in CMOS technology:

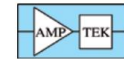
- smaller, good electrical properties, cheap.
- For example, state-of-the-art is CUBE (Politecnico Milano)  $\sim 1 \times 1 \times 1 \text{ mm}^3$

# Filter/shaper



- **Filtering** in the frequency domain = **Shaping** in the time domain
- Limit the bandwidth to limit the noise
- Noise depends on shaping time
- Modern trend: to go from analog to digital shaping

## NIM analog shaper



Digital Pulse Processor, MCA and Power Supply

PX5

### Features

- Includes digital shaping amplifier, MCA, and power supplies
- Compatible with all Amptek SDD, Si-PIN, and CdTe-diode detectors
- Supports detectors from other manufacturers, and both reset and feedback preamplifiers of either polarity
- Highly configurable
- Trapezoidal, and new Cusp shaping with wide range of peaking times to optimize performance
- High count rate capability with excellent baseline stability, throughput, and pile-up rejection
- Up to 8k output MCA channels
- Oscilloscope mode - DAC output monitoring and adjustment

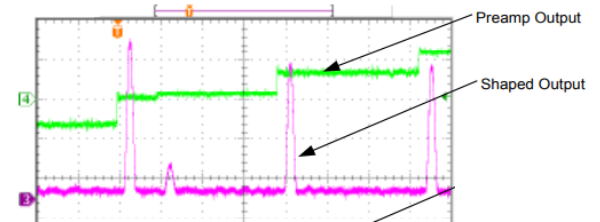


Front



### PX5 Waveforms

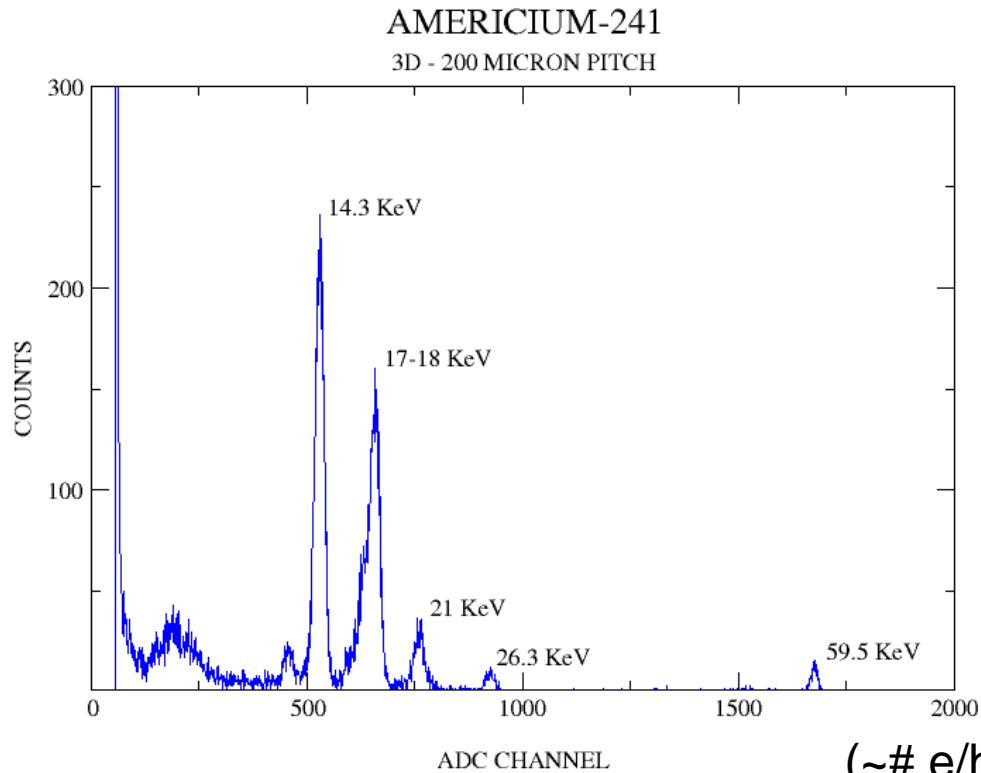
PX5 waveforms, showing from the preamp output to the shaped pulse etc.



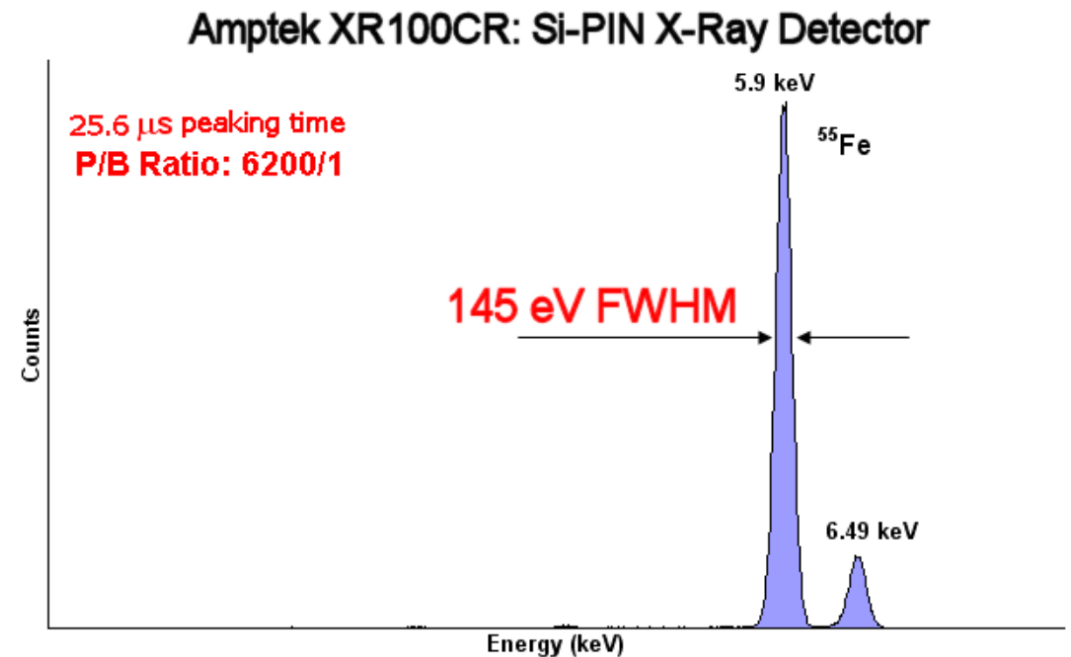
# Peak detection

# electron/hole pairs ~ amplitude of CSA output ~ amplitude of shaper output.

Stored for a short period of time, then fed to Analog-to-Digital Converter.  
Then sent out for processing



(~# e/h pairs, ~ energy)



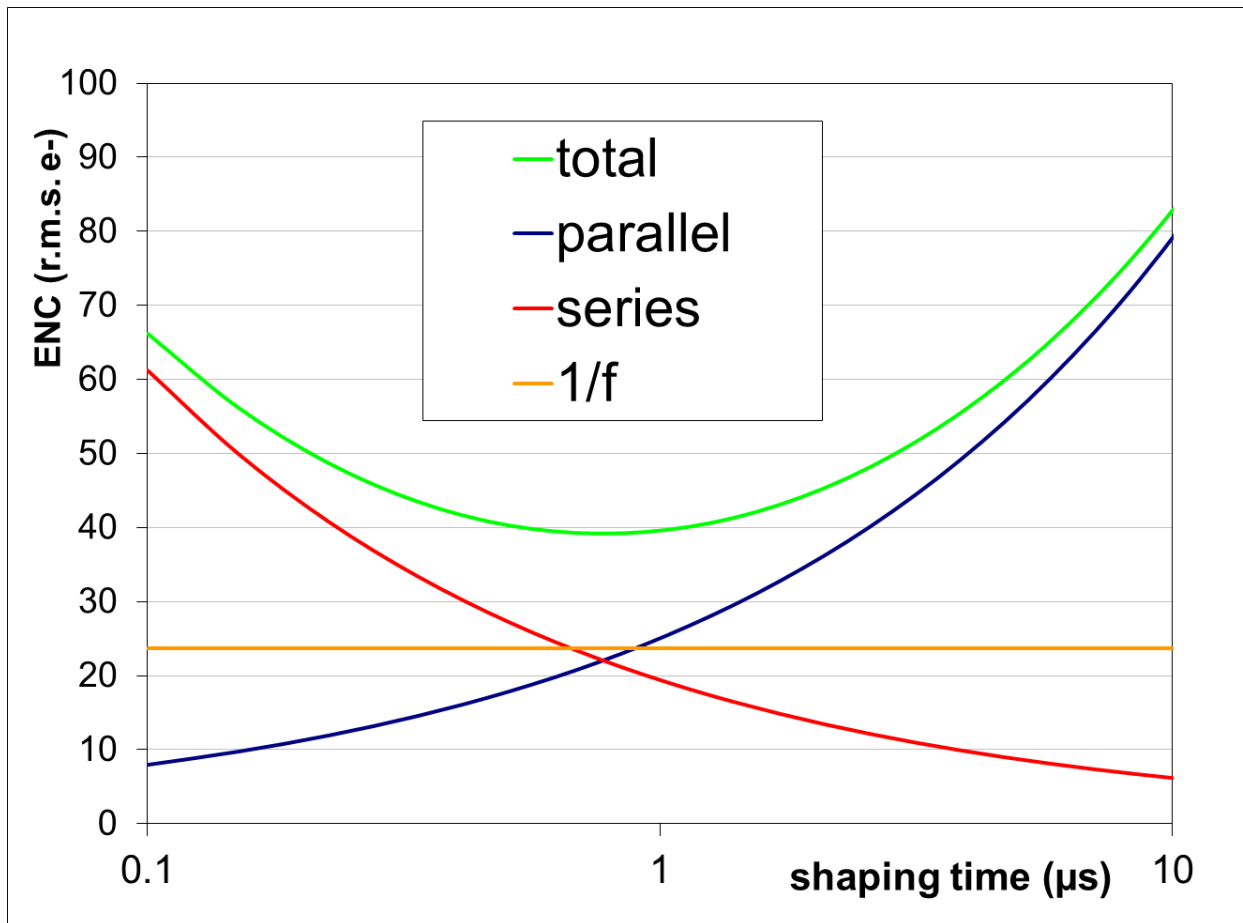
Low-activity X-ray-emitting radioactive materials are used as calibration sources

# Noise in a detection system

Intrinsic (physical) properties of sensor/detection system introduce noise in the read-out.

Equivalent Noise Charge (ENC) is the charge for which Signal-to-Noise ratio is 1.

Can be optimized, never eliminated, by wisely minimizing Capacitance (C) and sensor leakage current (as much as possible), designing good read-out (peaking time  $\tau$ ), etc.



$$ENC_{\text{parallel}}^2 \sim I_{\text{leakage}} \tau$$

$$ENC_{\text{series}}^2 \sim C^2 / \tau$$

$$ENC_{\text{flicker}}^2 \sim C^2$$

$$ENC_{\text{total}}^2 = ENC_{\text{parallel}}^2 + ENC_{\text{series}}^2 + ENC_{\text{flicker}}^2$$