Brookhaven National Laboratory

U.S. DEPARTMENT OF ENERGY

Data Acquisition in ASIC testing

Piotr Maj on behalf of ASIC group

Date 10/19/2023

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Data Acquisition

For ASIC testing

DAQ System Overview

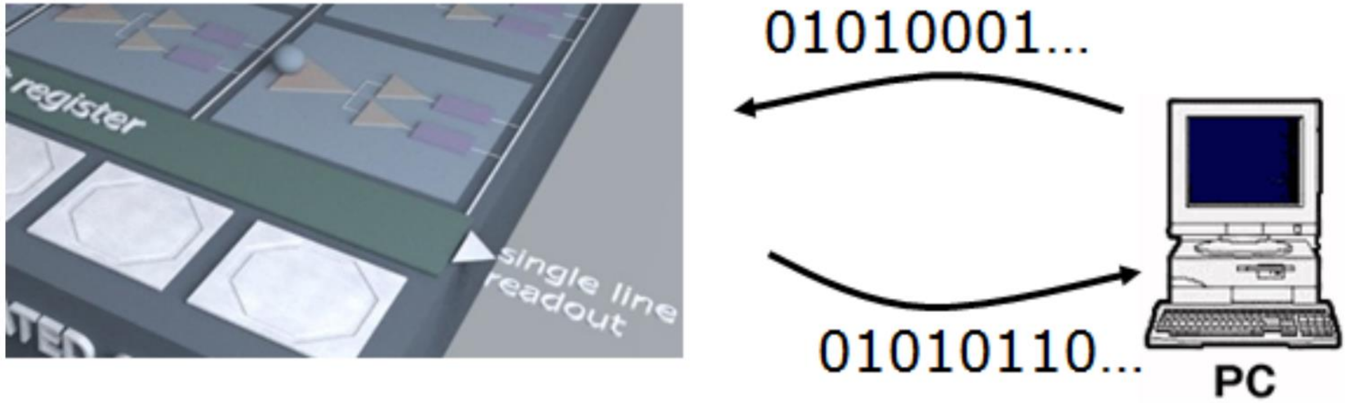
Data Acquisition (DAQ)

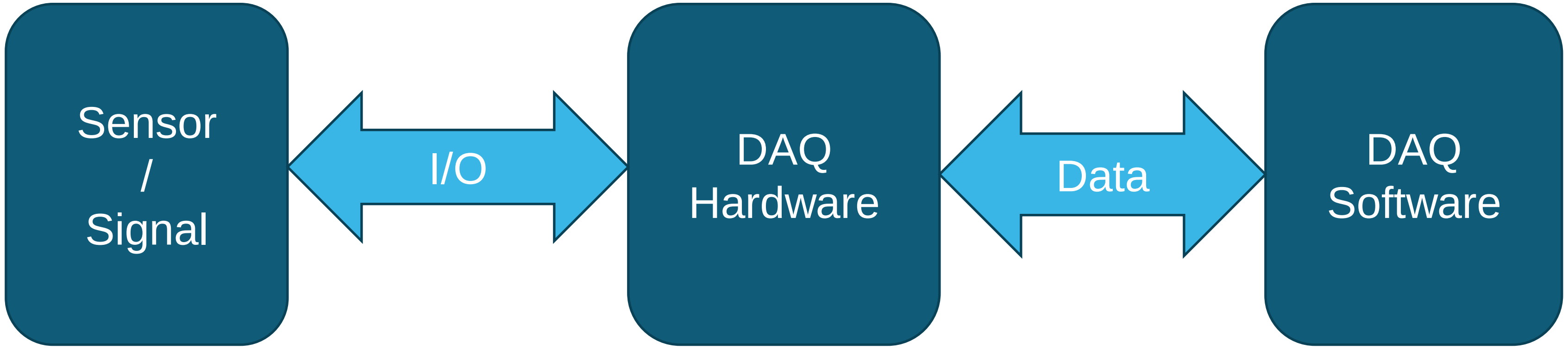
the automatic collection of data from sensors, instruments, and devices in a factory, laboratory, or in the field.

Purpose

To measure an electrical or physical phenomenon such as voltage, current, temperature, pressure, or sound

DAQ System Overview




Sensor / Signal

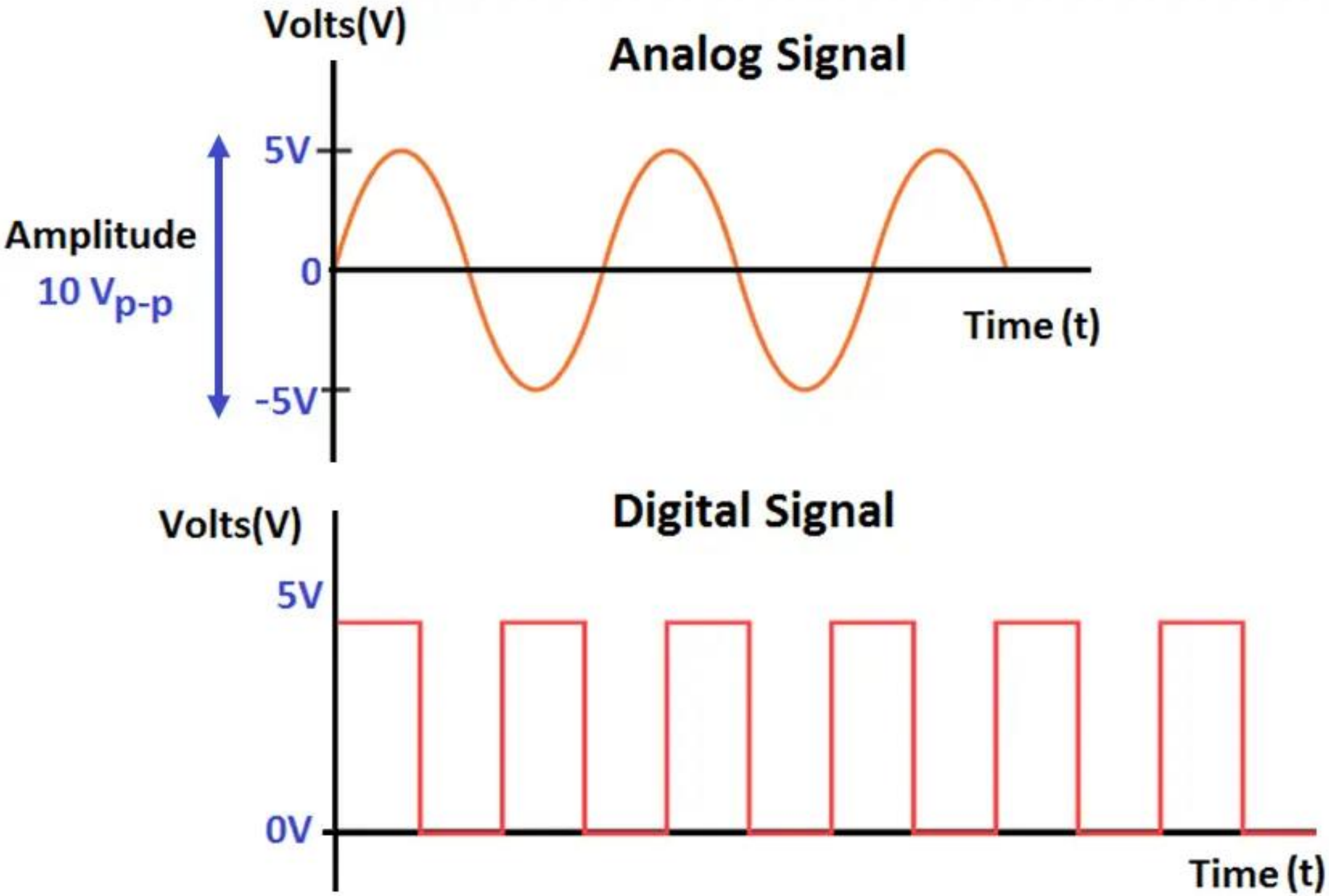
I/O

DAQ Hardware

Data

DAQ Software

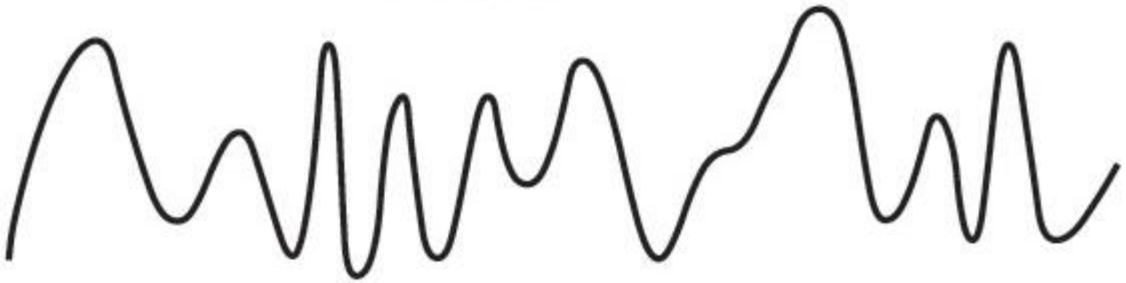
Signal Classification



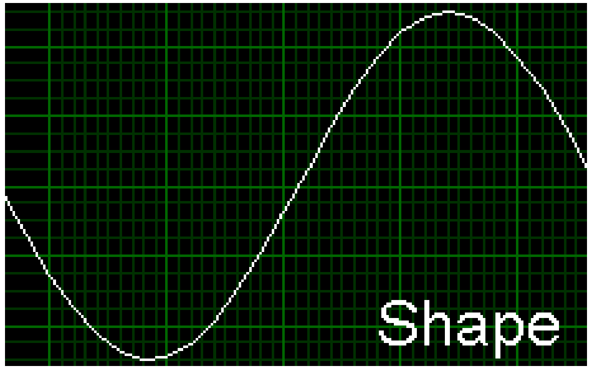
Analog Signals

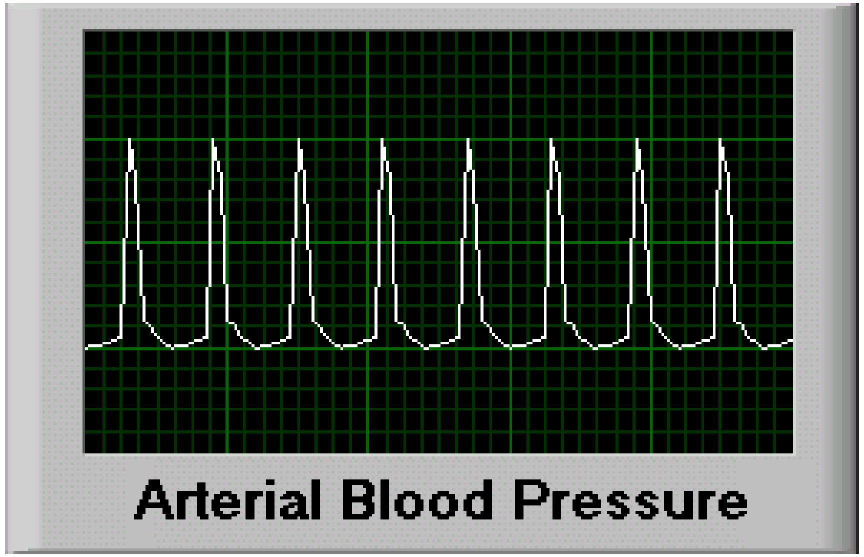
- Continuous signal
  - Can be at any value with respect to time
- Three types of information
  - Level
  - Shape
  - Frequency

Analog

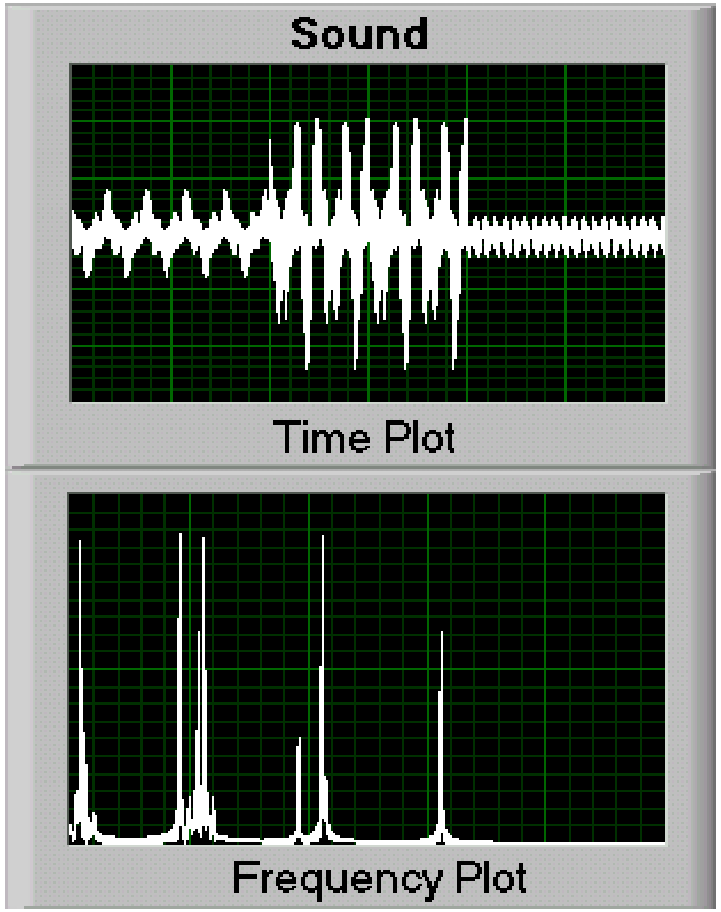


Analog Signals

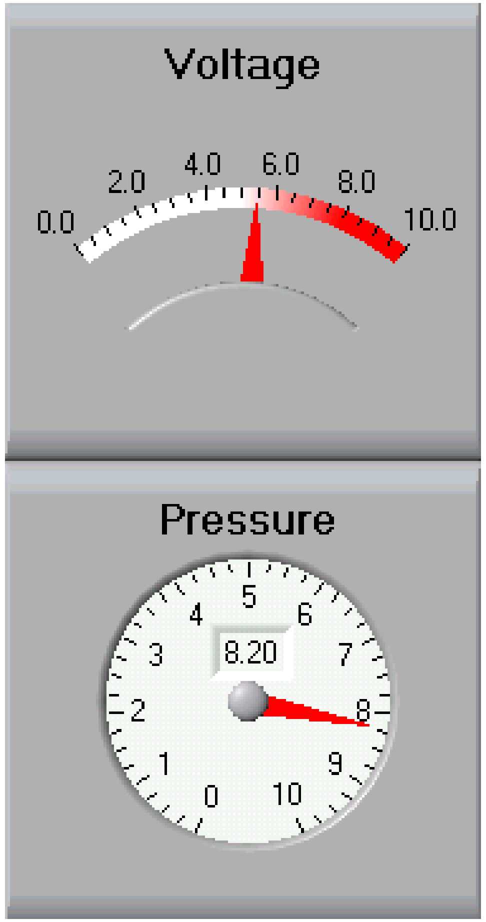




Frequency



level



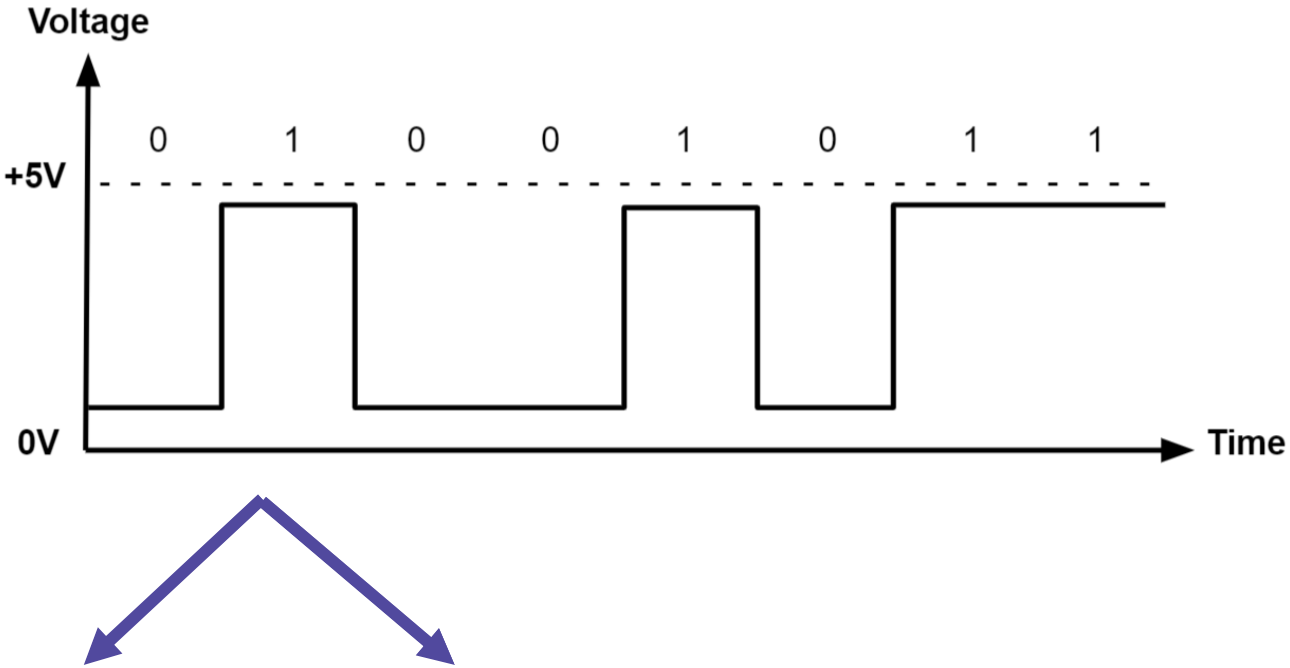
Digital Signals

Two possible levels:

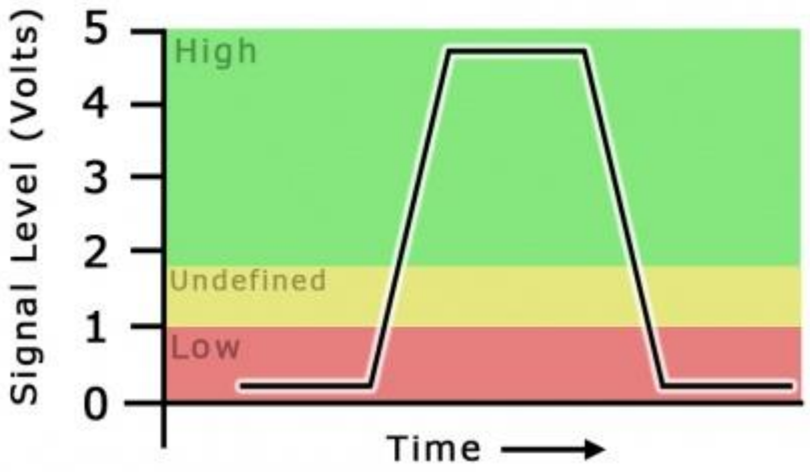
- High/On
- Low/Off

Two types of information:

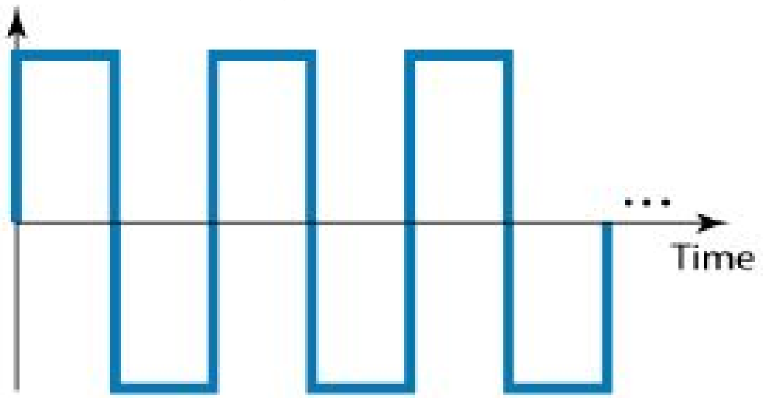
- State
- Rate



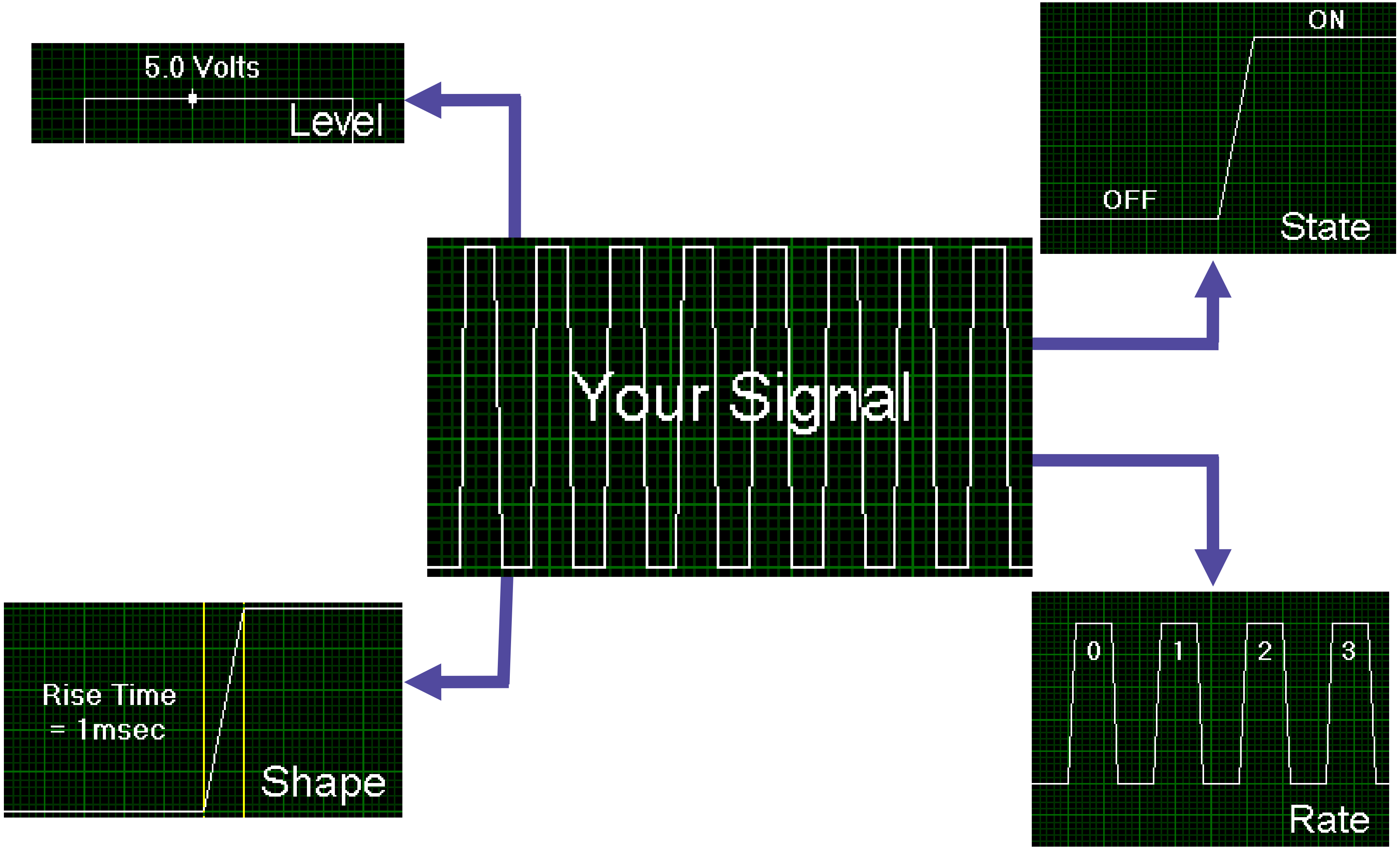
State



Rate

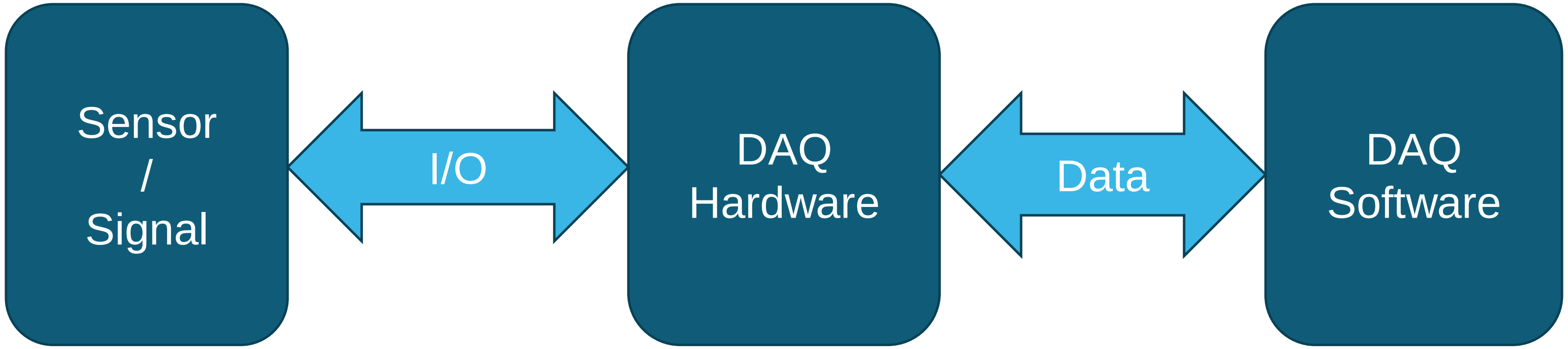


5 Ways to Measure the Same Signal

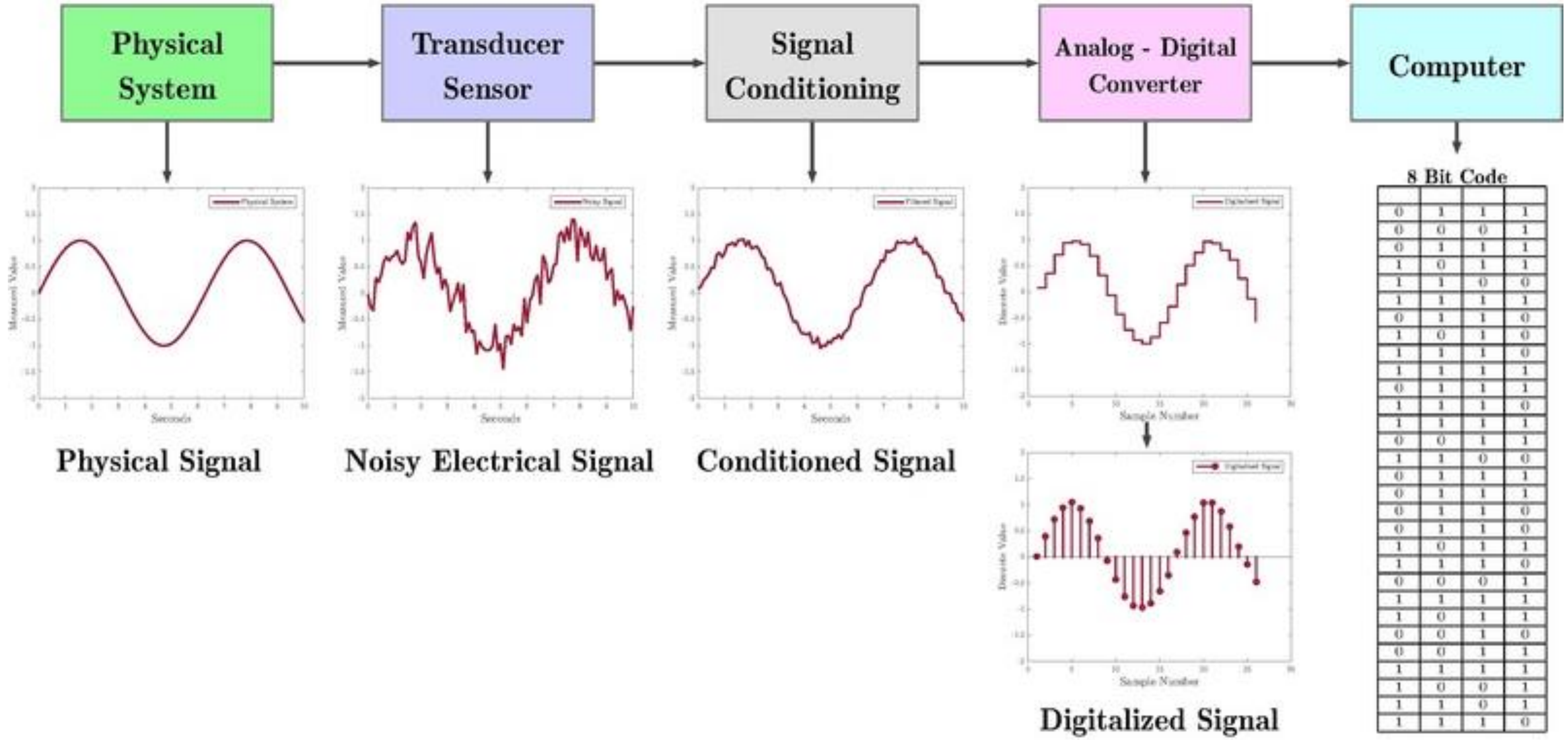


DAQ Hardware Overview

- DAQ hardware
  - Can acquire and generate analog and digital signals
  - Transfers signals to and from DAQ software through a bus (e.g. PCIe, USB)



Data Acquisition Hardware



Physical Signal

Noisy Electrical Signal

Conditioned Signal

Digitalized Signal

8 Bit Code

0	1	1	1
0	0	0	1
0	1	1	1
1	0	1	1
1	1	0	0
1	1	1	1
0	1	1	0
1	0	1	0
1	1	1	0
1	1	1	1
0	1	1	1
1	1	1	0
1	1	1	1
0	0	1	1
1	1	0	0
0	1	1	1
0	1	1	1
0	1	1	0
0	1	1	0
1	0	1	1
1	1	1	0
0	0	0	1
1	1	1	1
1	0	1	1
0	0	1	0
0	0	1	1
1	1	1	1
1	0	0	1
1	1	0	1
1	1	1	0

DAQ Device

st DAQ devices have:

- Analog Input
- Analog Output
- Digital I/O
- Counters

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Specialty devices exist for specific applications

- High speed digital I/O
- High speed waveform generation
- Dynamic Signal Acquisition (vibration, sonar)

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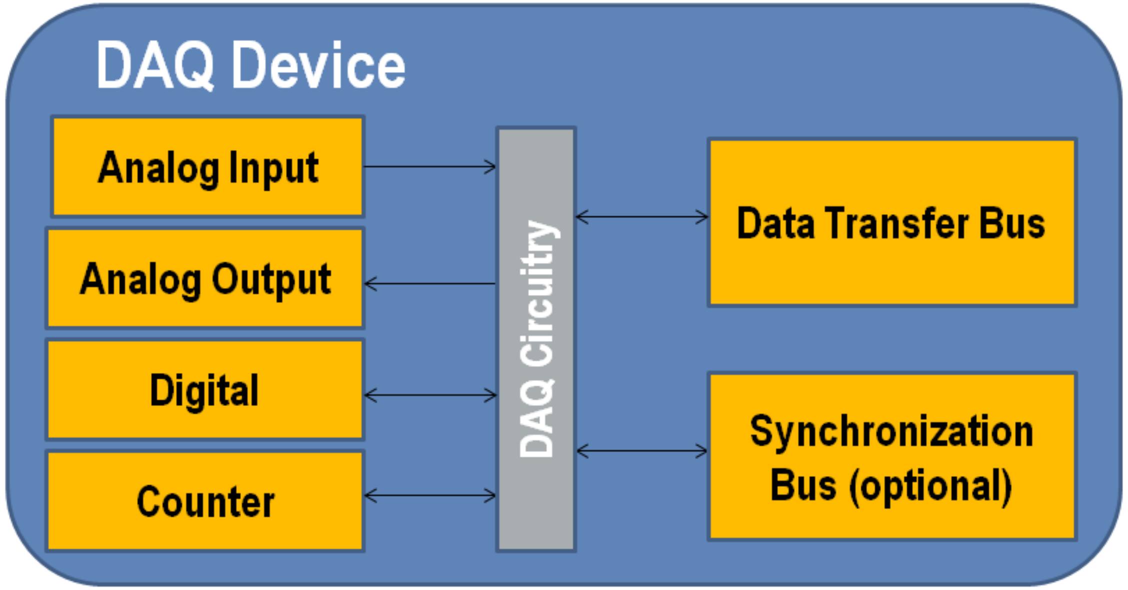
B. Components of a DAQ Device

- Data Transfer Bus
  - Connects the DAQ device to the computer
  - Can be a variety of bus structures
    - USB, PCI Express,



- Synchronization Bus
  - Used to synchronize multiple DAQ devices
  - Allows sharing of timing and trigger signals between devices

C. Choosing Appropriate DAQ Hardware

- Bus Considerations
- Signal Considerations
- Accuracy Considerations

Bus Considerations

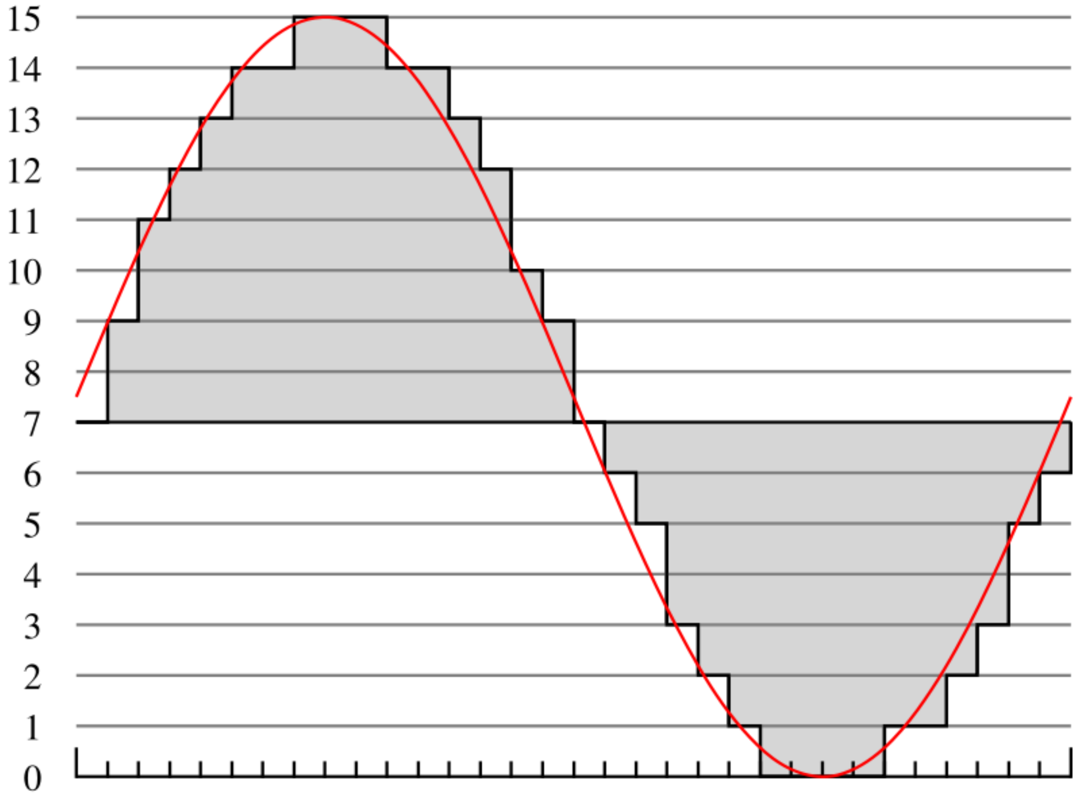
- How much data will I be streaming across this bus?
  - Bus bandwidth
- What are my single-point I/O requirements?
  - Bus latency and determinism
- Do I need to synchronize multiple devices?
  - Bus synchronization options
- How portable should this system be?
- How far will my measurements be from my computer?

Signal Considerations

- How many channels?
  - Choose DAQ device(s) with enough channels
- How quickly do you need to acquire/generate samples of the signal?
  - Choose DAQ device with fast enough sampling rate
- What are the expected minimum and maximum measurements?
  - Choose DAQ device with appropriate range
- What is the smallest change in your signal that you need to detect?
  - Choose DAQ device with a small enough code width
  - To calculate the code width, you must know:
    - Resolution
    - Device input range

Calculating Code Width – Resolution Example

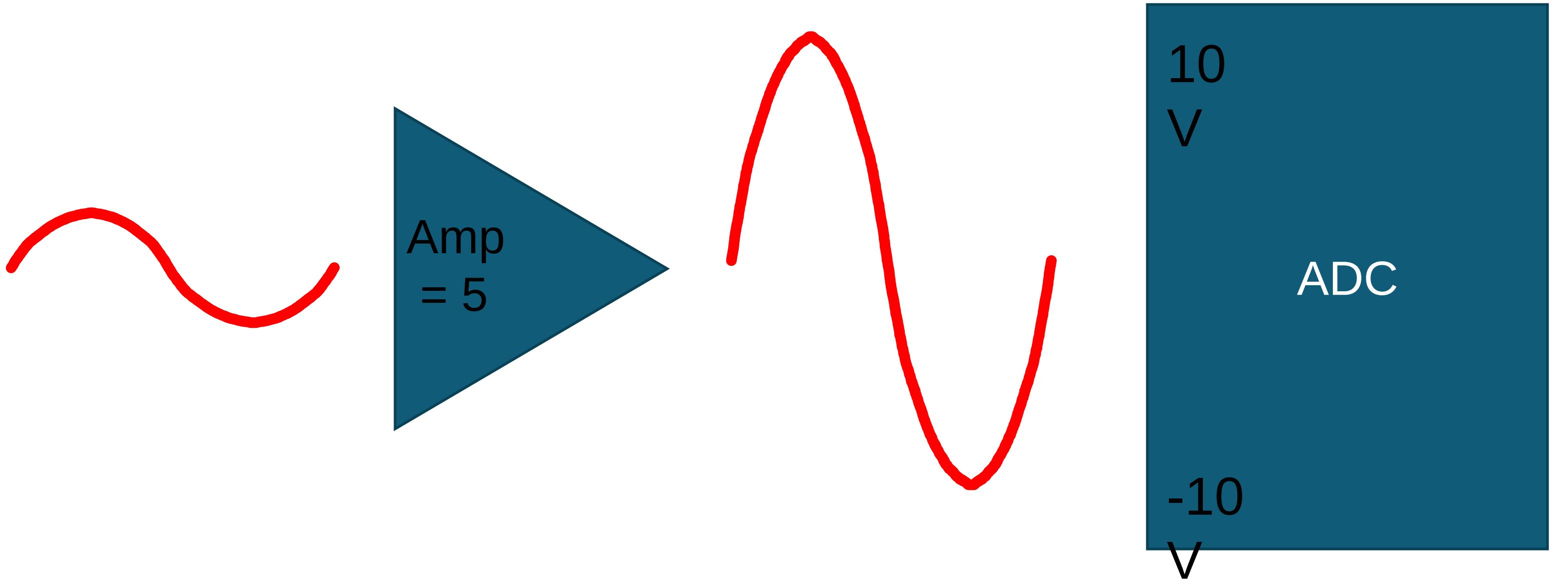
- 4-bit resolution can represent 16 voltage levels
- 16-bit resolution can represent 65,536 voltage levels



Calculating Code Width – Amplification and Device Input Range

DAQ devices have a built-in amplifier

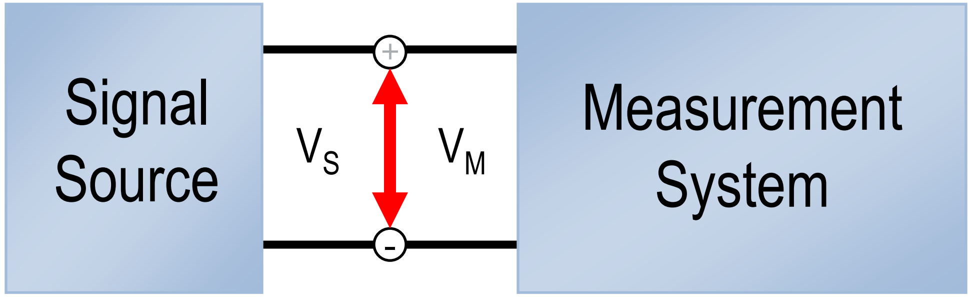
- Amplifies the signal to better fit the range of the ADC
- Better utilizes the ADC resolution



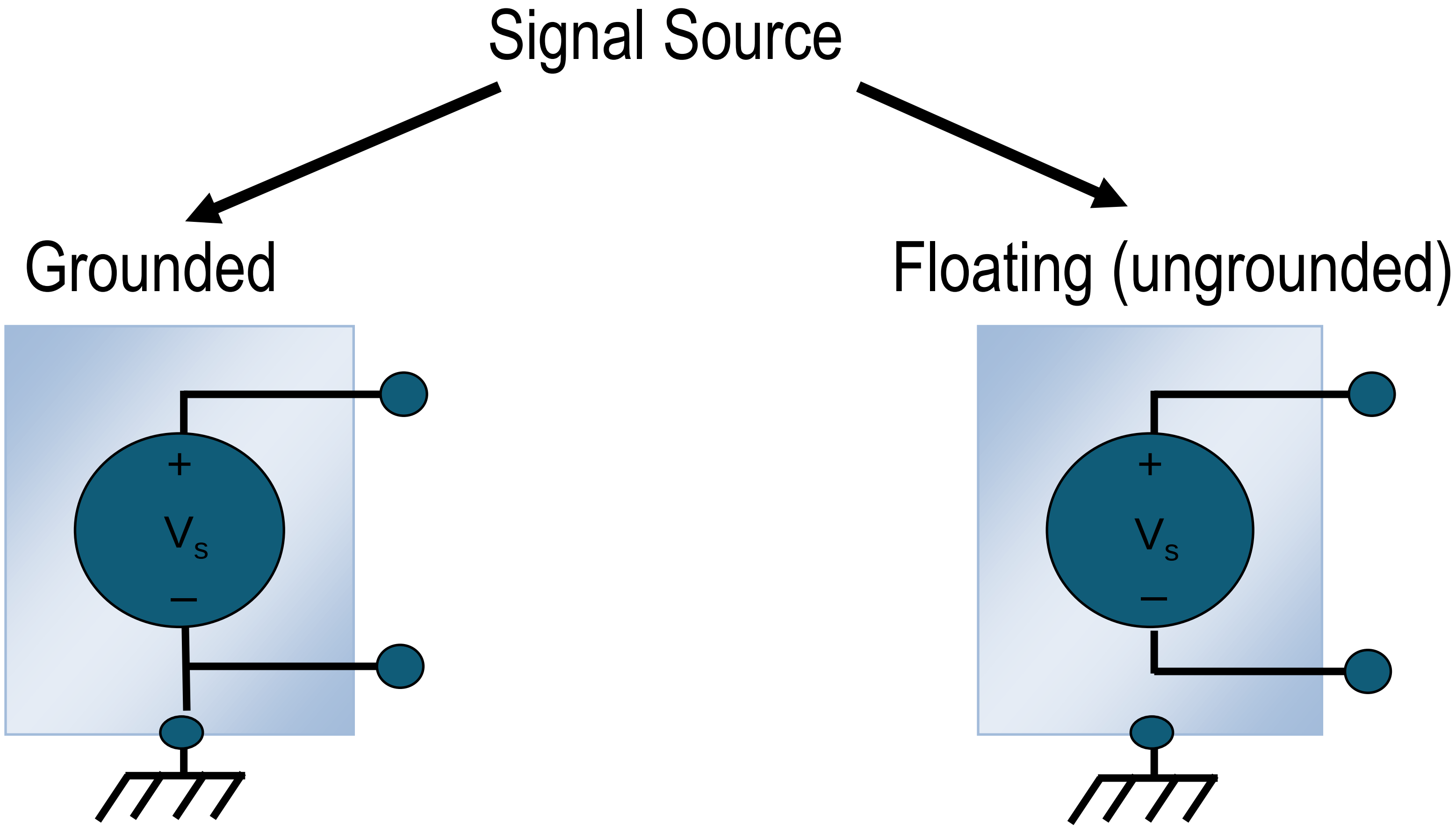
Grounding Issues

- To get correct analog input measurements, you must properly ground your system
- How the signal is grounded affects how you should ground the instrumentation amplifier on the DAQ device
- Steps to proper grounding of your system:

1. Determine how your signal is grounded
2. Choose a grounding mode for your Measurement System



Signal Source Categories



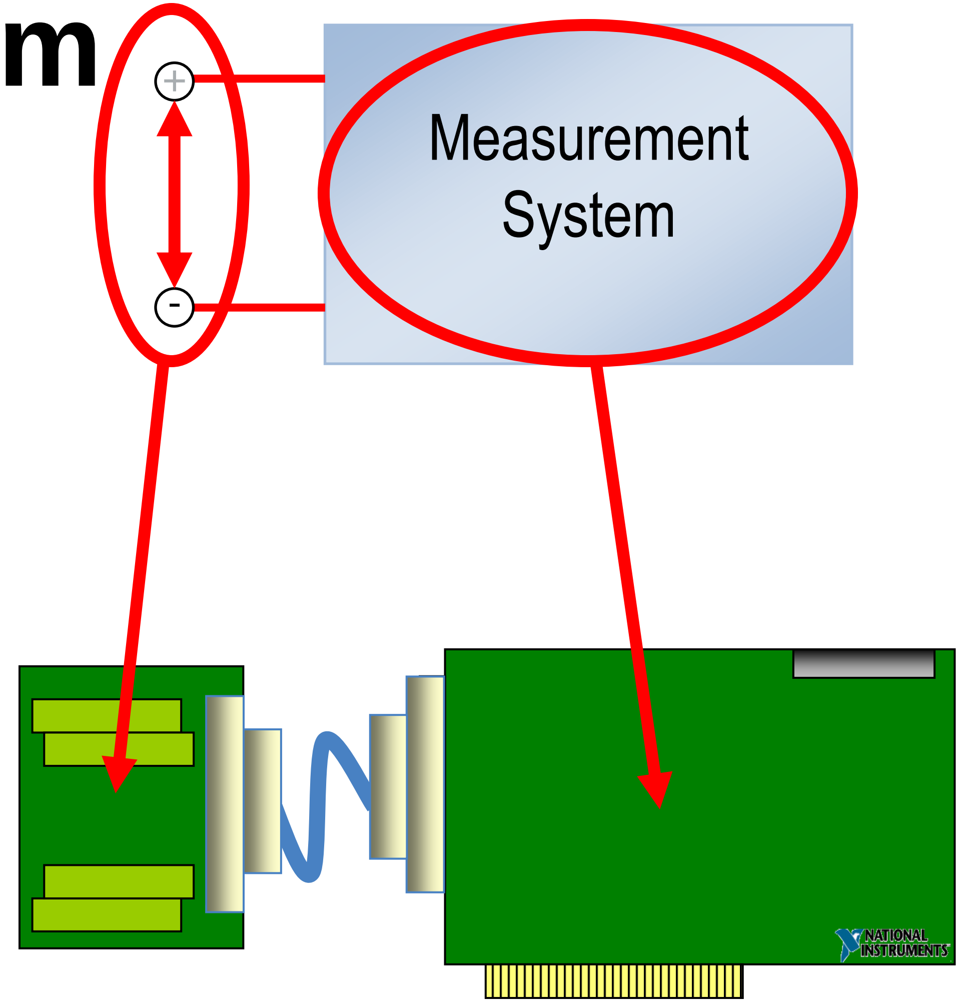
Signal Source

Grounded

Floating (ungrounded)

Measurement System

- Three modes of grounding for your Measurement System
  - Differential
  - Referenced Single-Ended (RSE)
  - Non-Referenced Single-Ended (NRSE)
- Mode you choose will depend on how your signal is grounded



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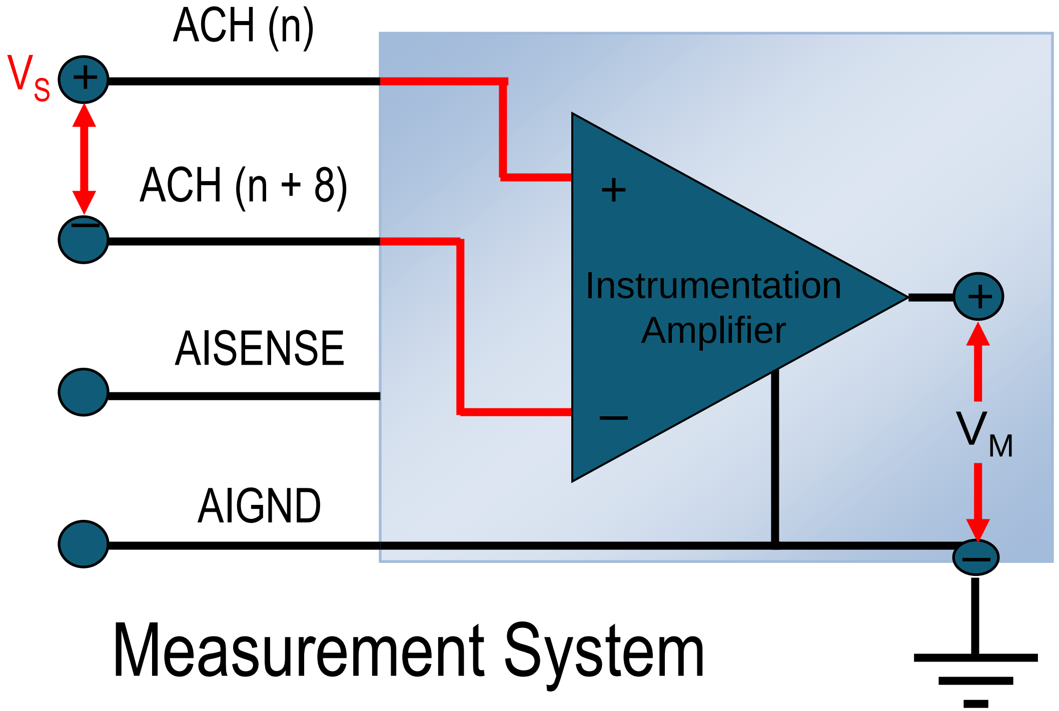
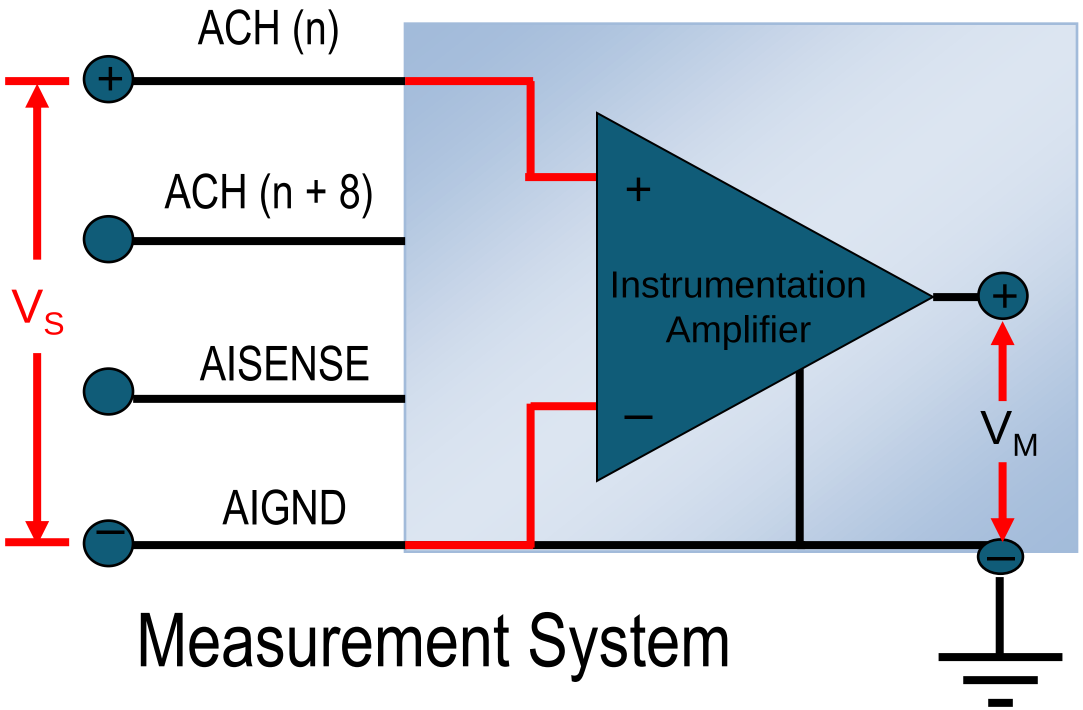
Differential Mode

- Two channels used for each signal
- Rejects common-mode voltage and common-mode noise



Referenced Single-Ended (RSE) Mode

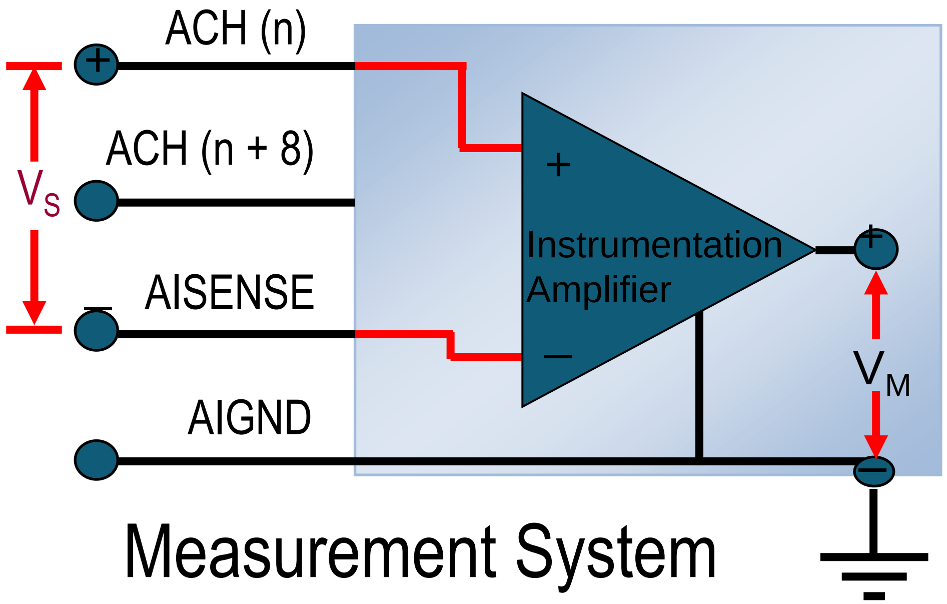
- Measurement made with respect to system ground
- One channel used for each signal
- Does not reject common mode voltage



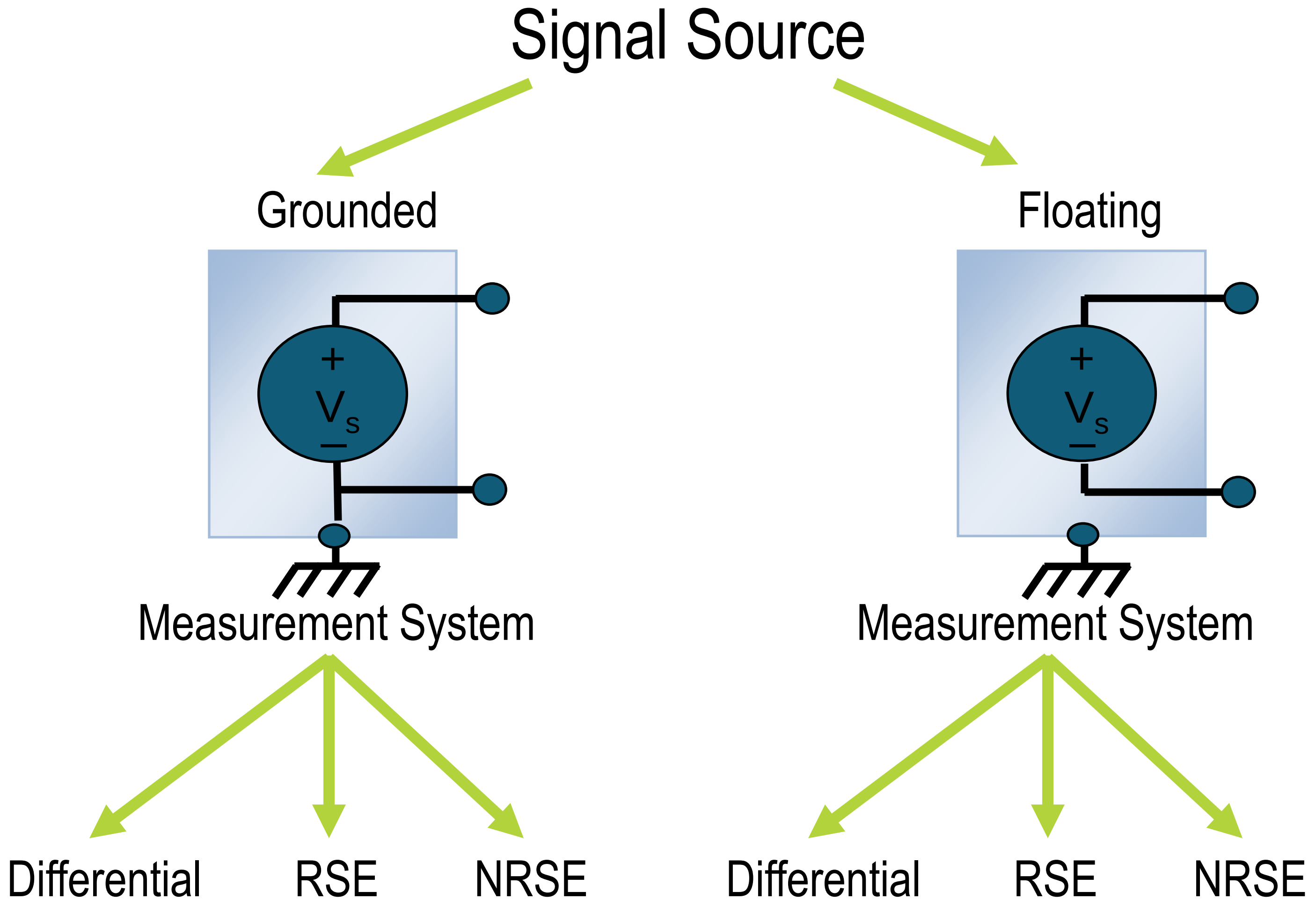
Measurement System

Non-Referenced Single-Ended (NRSE) Mode

- One channel used for each signal
- Measurement made with respect to AISENSE not system ground
- AISENSE is floating



Choosing Your Measurement System



Signal Source

Grounded

Floating

Measurement System

Measurement System

Differential

RSE

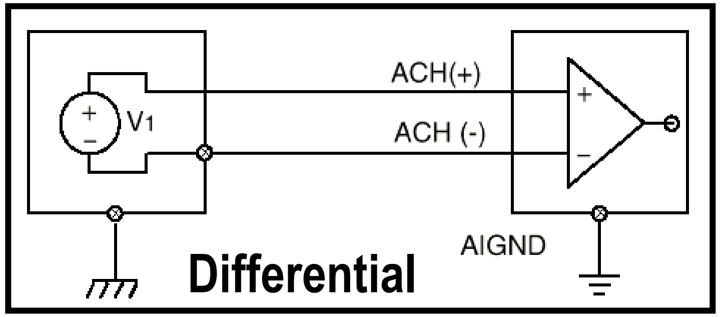
NRSE

Differential

RSE

NRSE

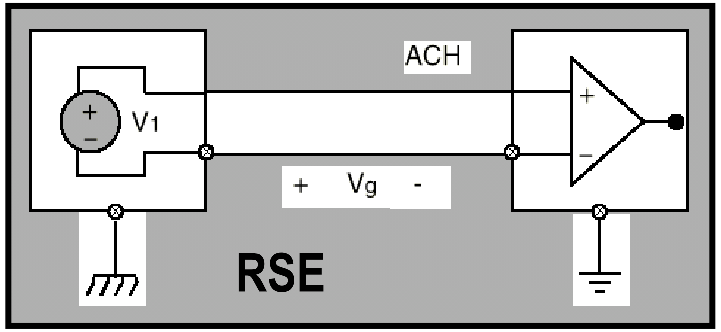
Options for Grounded Signal Sources



Better

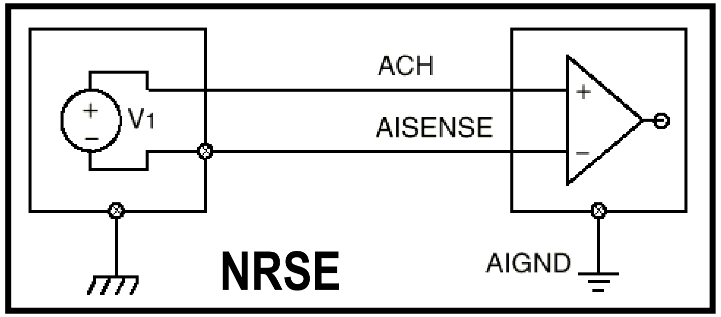
+ Rejects common-mode voltage

– Cuts channel count in half



Not Recommended

– Voltage difference (Vg) between the two grounds makes a ground loop that could damage the device

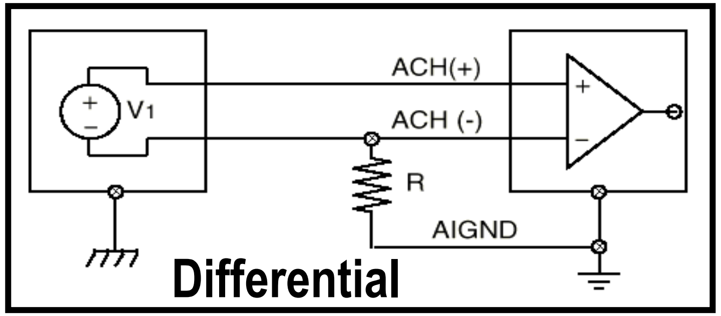


Good

+ Allows use of entire channel count

– Does not reject common-mode voltage

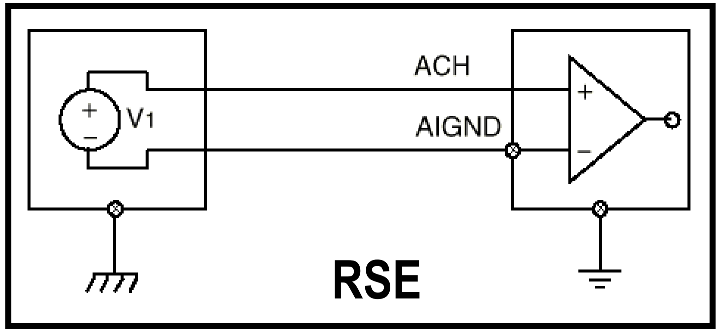
Options for Floating Signal Sources



Differential

Best

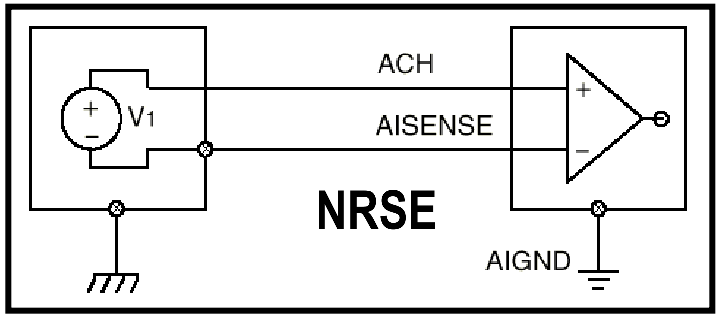
+ Rejects common-mode voltage
– Cuts channel count in half
– Needs bias resistors



RSE

Better

+ Allows use of entire channel count
+ Do not need bias resistors
– Does not reject common-mode voltage

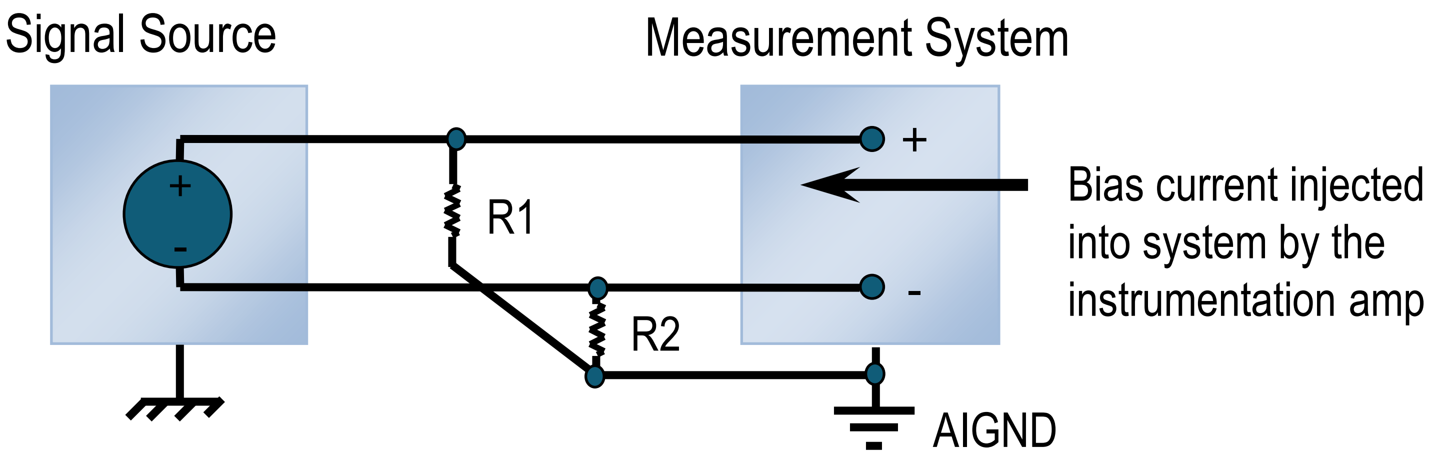


NRSE

Good

+ Allows use of entire channel count
– Needs bias resistors

Bias Resistors

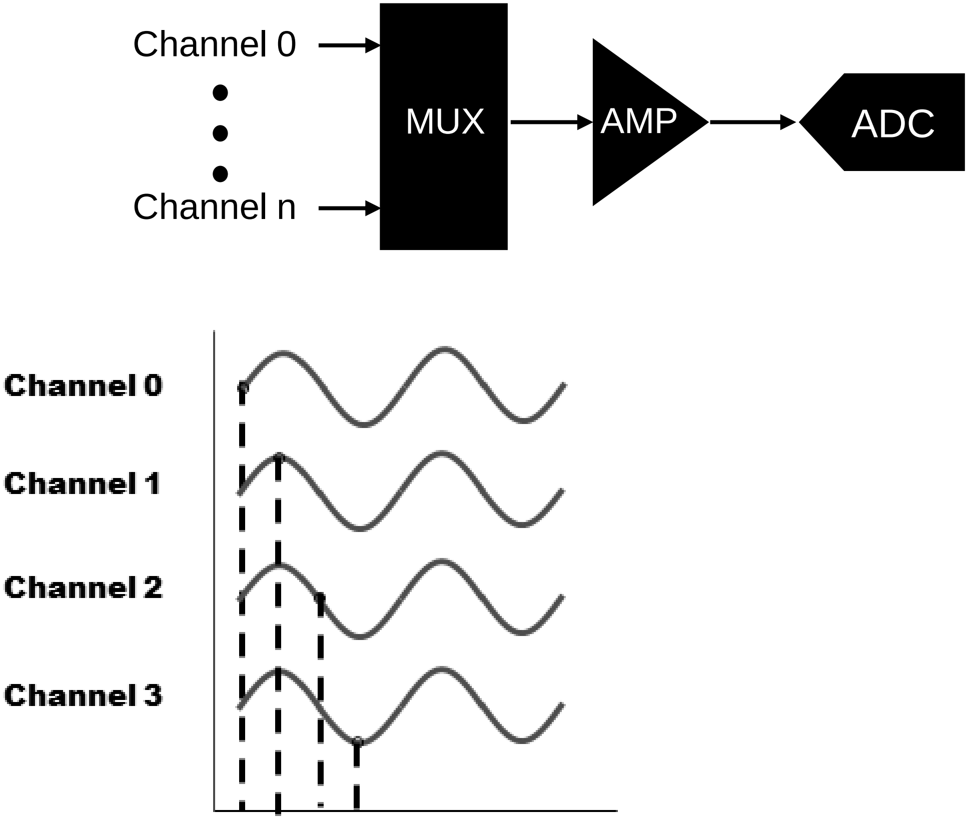


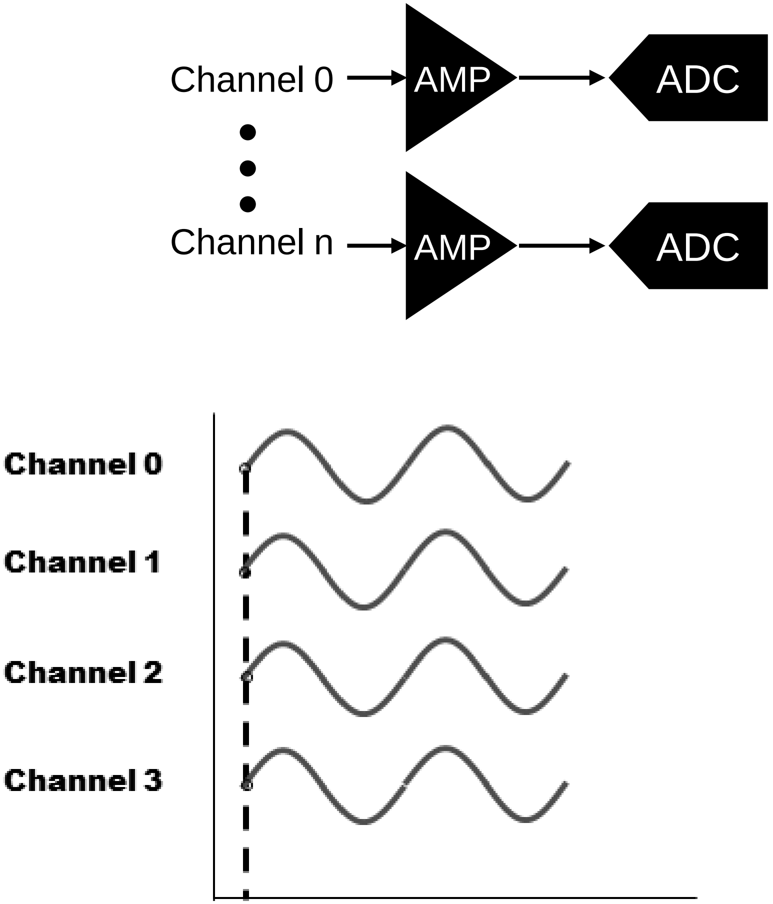
Bias current injected into system by the instrumentation amp

- Needed with floating signal source and floating measurement system (Differential or NRSE)
- Bias resistors provide a return path to ground for instrumentation amplifier bias currents
- Recommended value is between 10 kΩ and 100 kΩ

Parallel sampling

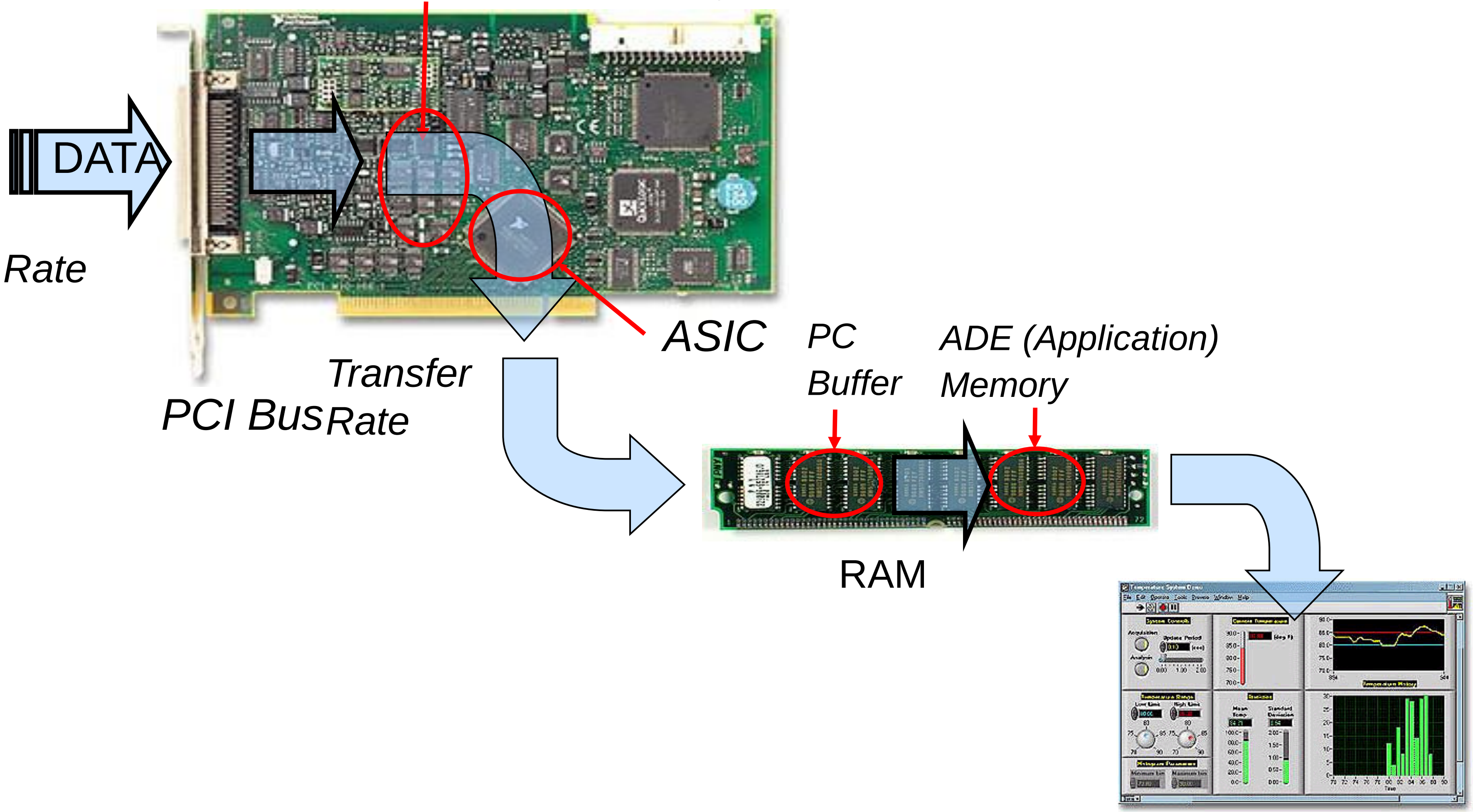
- Used when time relationship between signals is important
- to synchronize the taking of samples





Data Transfer for an Input Operation

Onboard FIFO Memory



DATA

Input Rate

ASIC

PC
Buffer

ADE (Application)
Memory

Transfer
Rate

PCI Bus

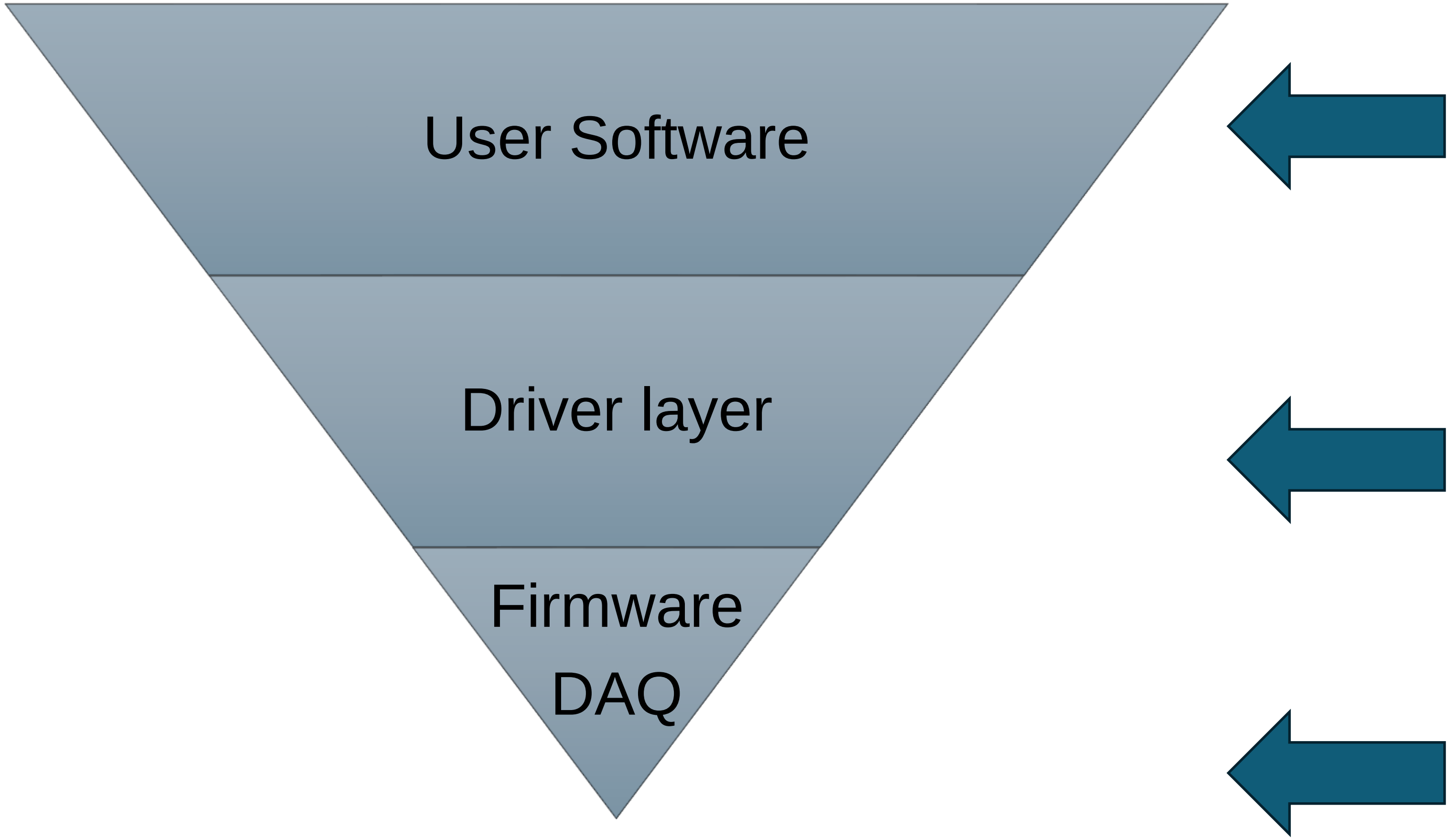
RAM

Software

Software for DAQ

Short introduction to graphical programming

Software Architecture



High level software / data storage / data analysis

General purpose input/output – interface to the firmware

Low-level software for high-speed input/output operations

High-level software

Data acquisition

Instrument control

Offline analysis

Data presentation

Data Storage

Ethernet Sync.

Extensible functionality

Classical design patterns

LabVIEW for DAQ

DEMO 1 – Program Structure

DEMO 2 – Data Acquisition

DEMO 3 – State Machine

Embedded systems programming

with LabVIEW Real-Time and FPGA

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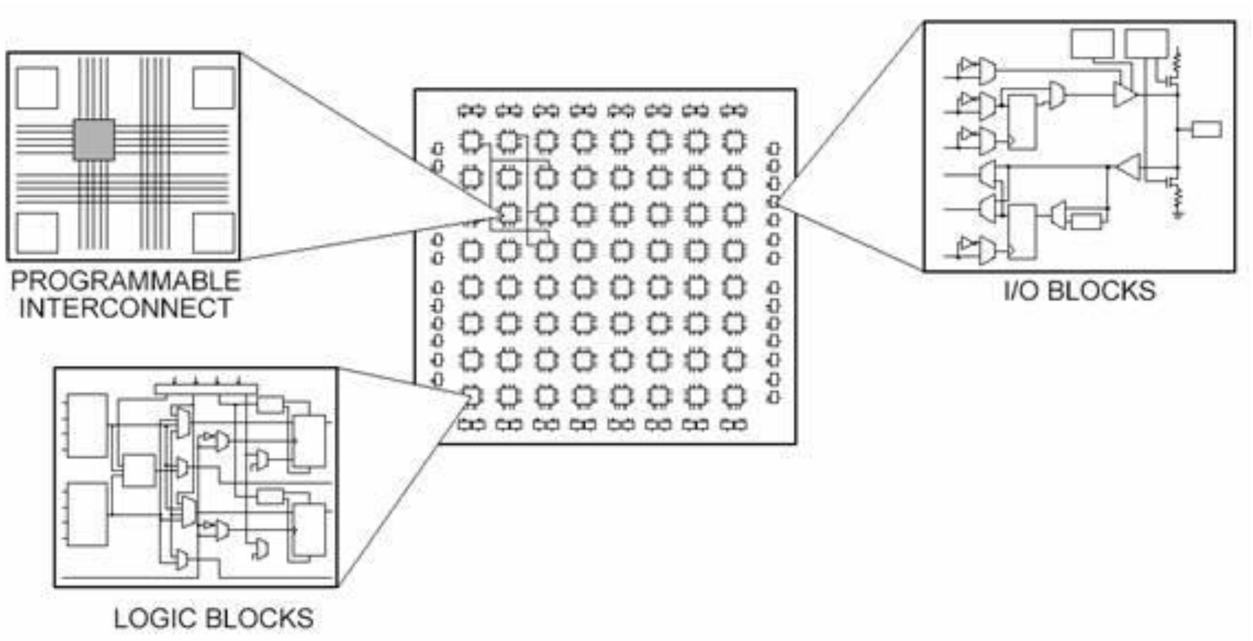
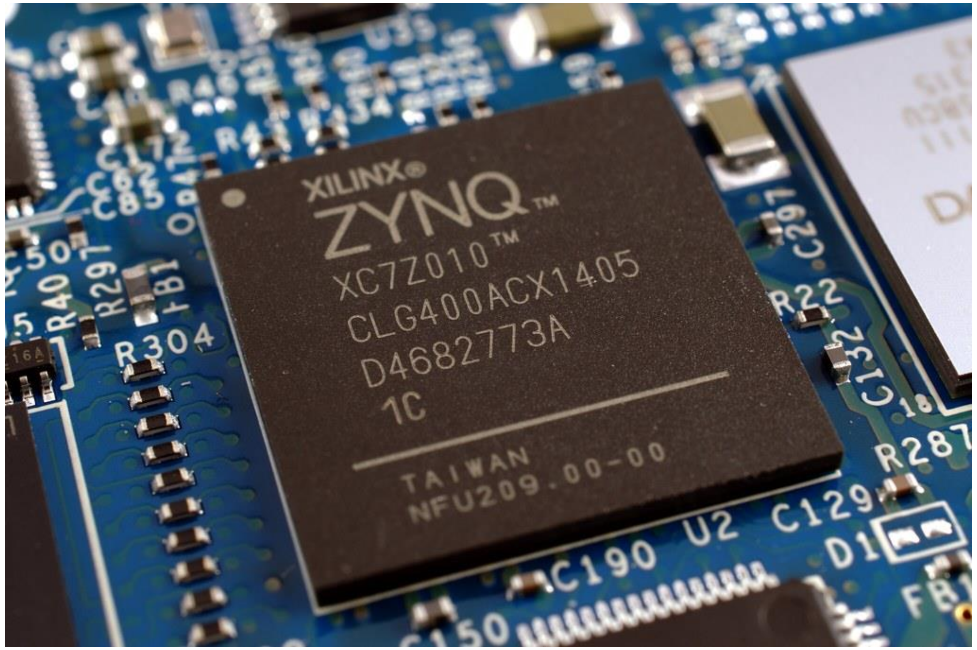
FPGA

FPGA (ang. *Field Programmable Gate Arrays*)



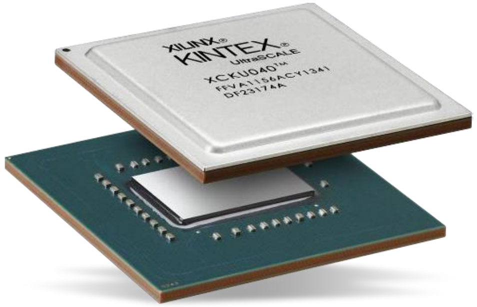


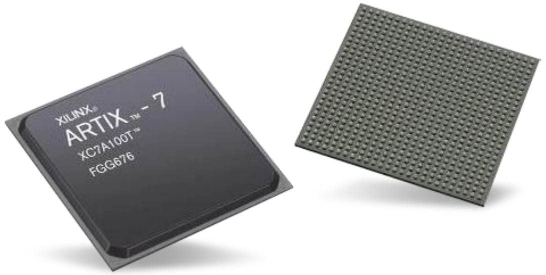
https://atadiat.com/wp-content/uploads/2020/03/fpga-chip.jpg

CPU vs FPGA vs ASIC

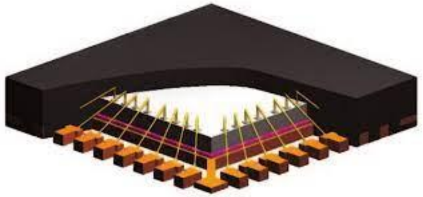
CPU / GPU

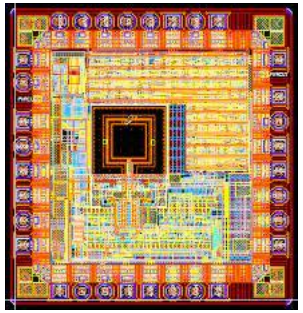
FPGA



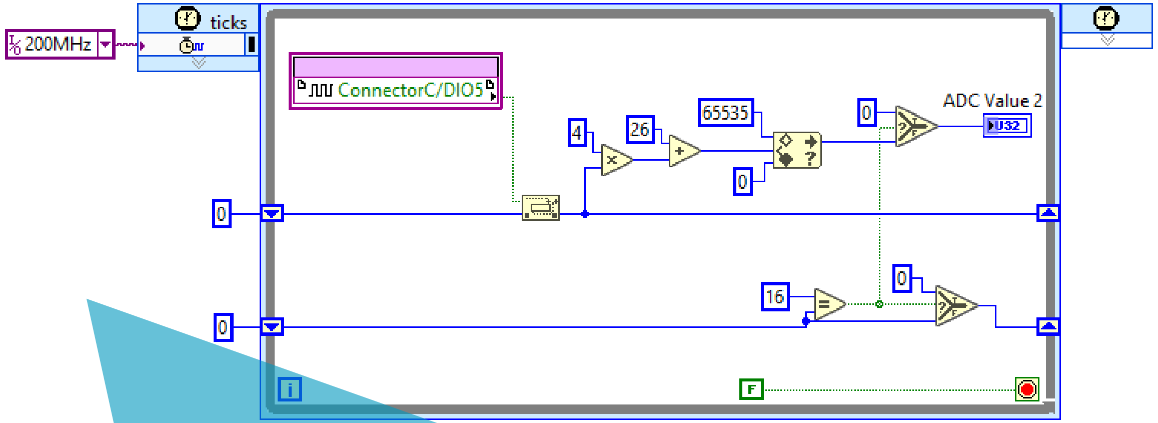


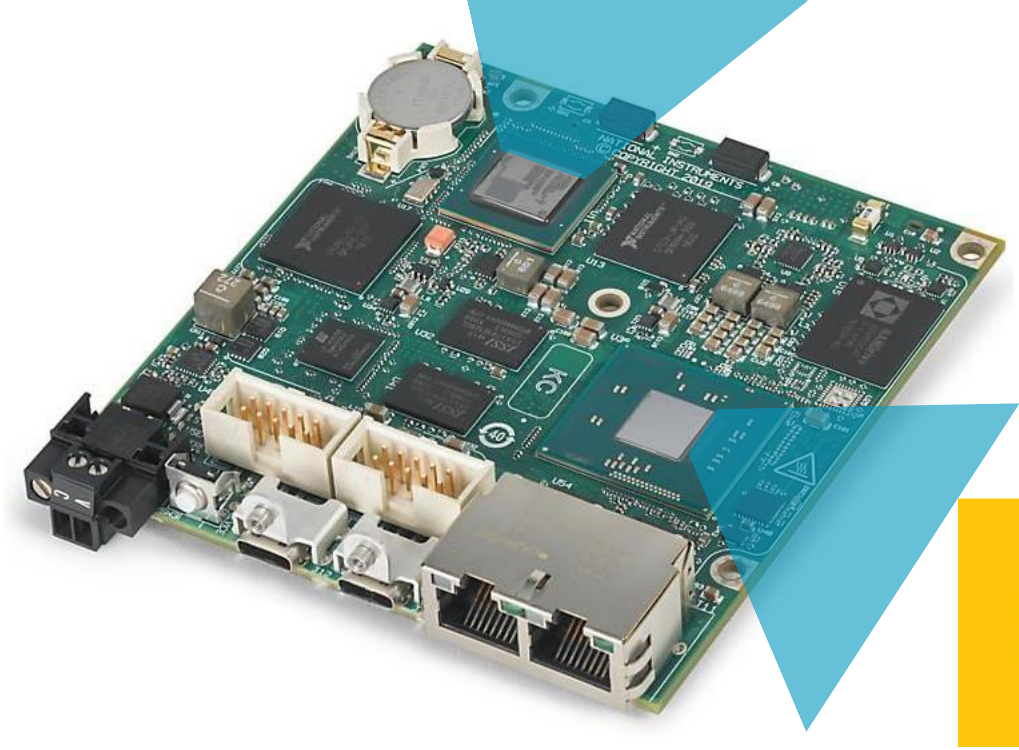
ASIC

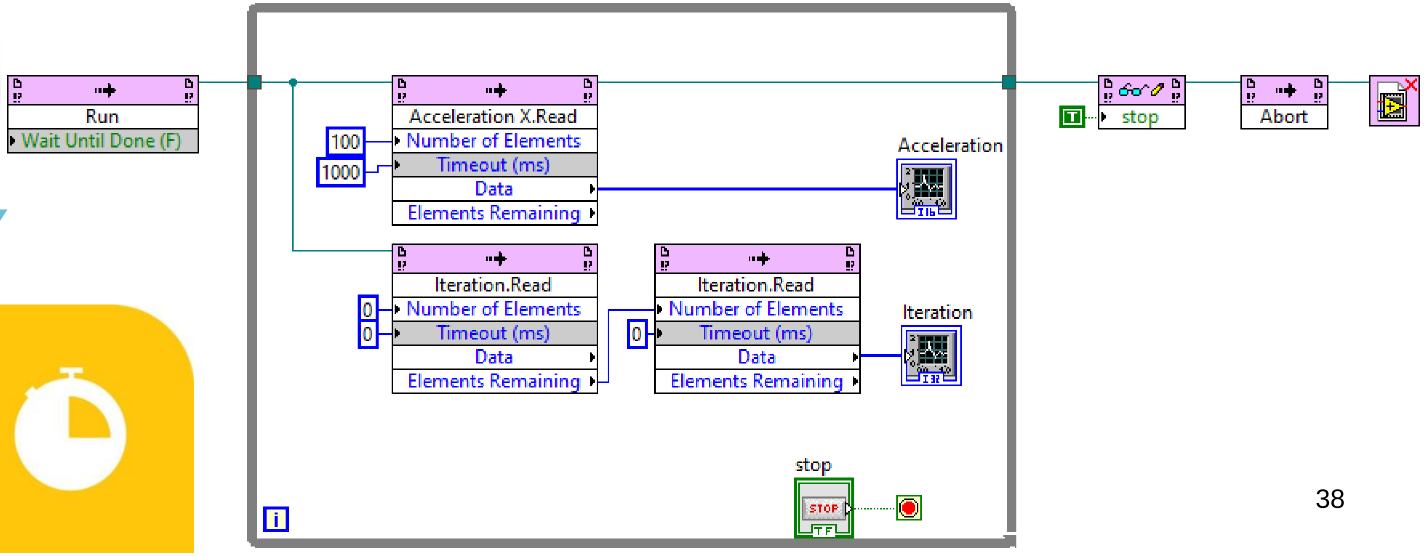




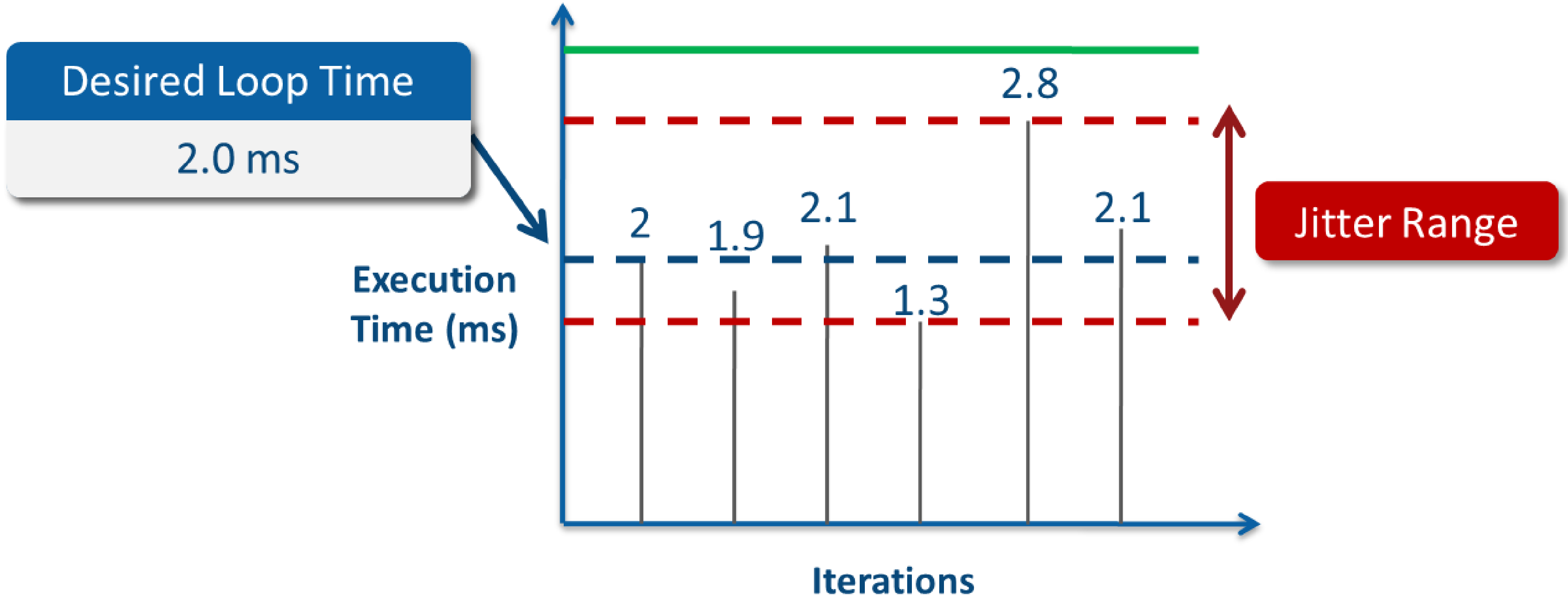
Embedded system



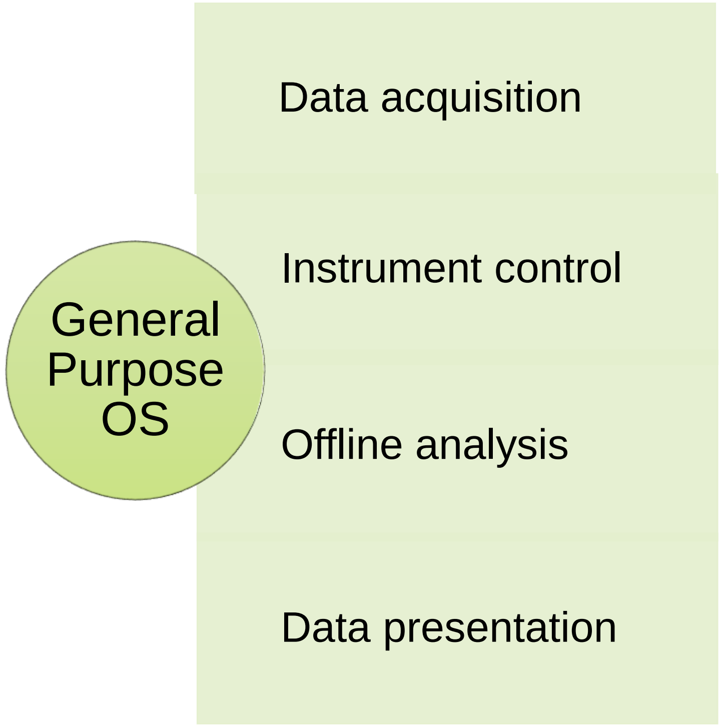


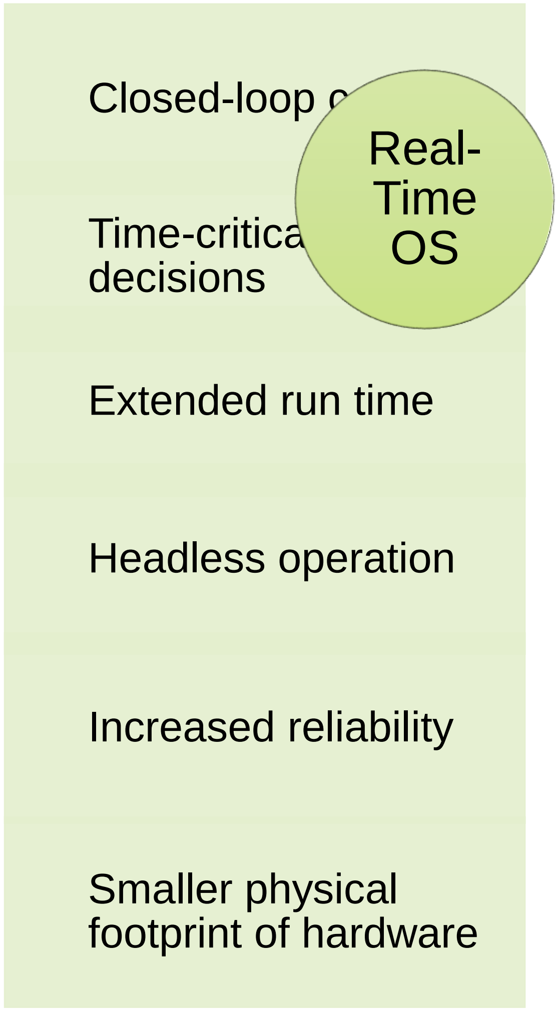


RT-OS

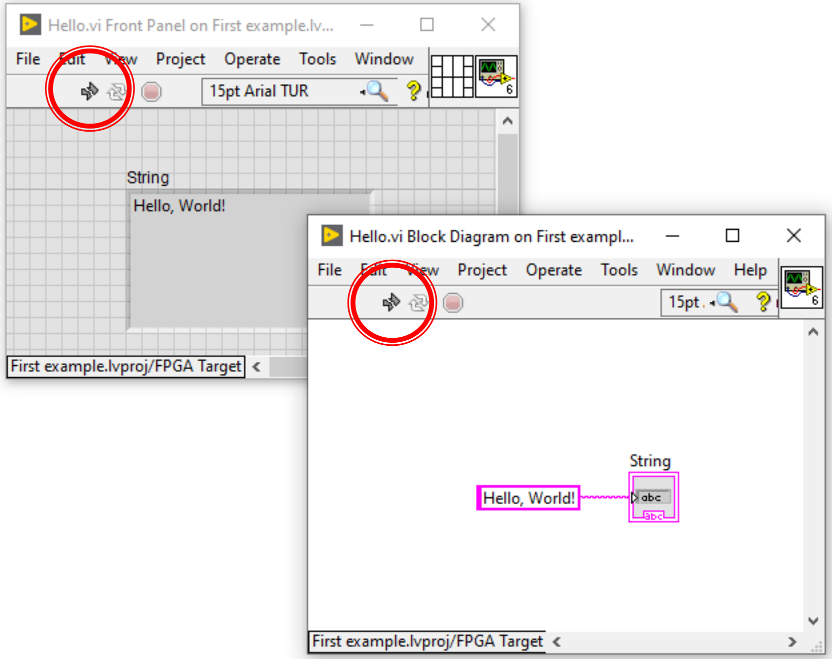

Desired Loop Time
2.0 ms
Execution Time (ms)
2
1.9
2.1
1.3
2.8
2.1
Jitter Range
Iterations

RT-OS

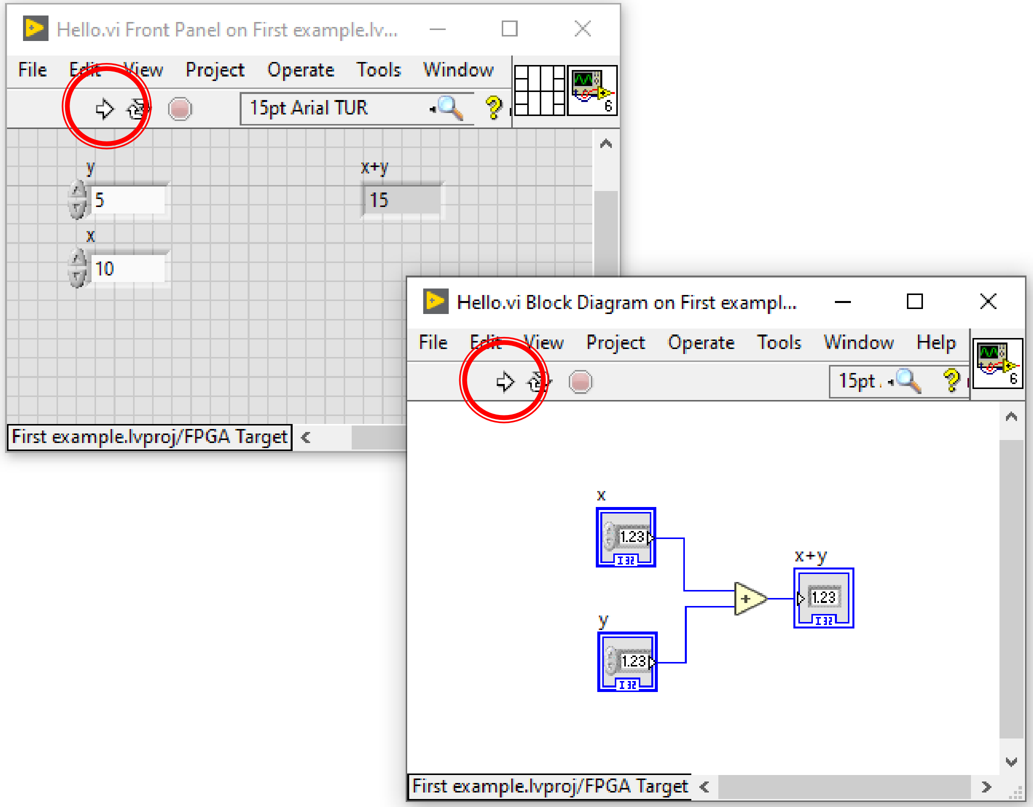

General Purpose OS
Data acquisition
Instrument control
Offline analysis
Data presentation


Real-Time OS
Closed-loop c
Time-critica decisions
Extended run time
Headless operation
Increased reliability
Smaller physical footprint of hardware

Hello World in FPGA


Hello.vi Front Panel on First example.lv...
File Edit View Project Operate Tools Window
15pt Arial TUR
Hello.vi Block Diagram on First exampl...
File Edit View Project Operate Tools Window Help
15pt
abc
First example.lvproj/FPGA Target

String: Hello, World!


Hello.vi Front Panel on First example.lv...
File Edit View Project Operate Tools Window
15pt Arial TUR
Hello.vi Block Diagram on First exampl...
File Edit View Project Operate Tools Window Help
15pt
x
y
x+y
1.23
I32
+
First example.lvproj/FPGA Target

y: 5

x: 10

x+y: 15

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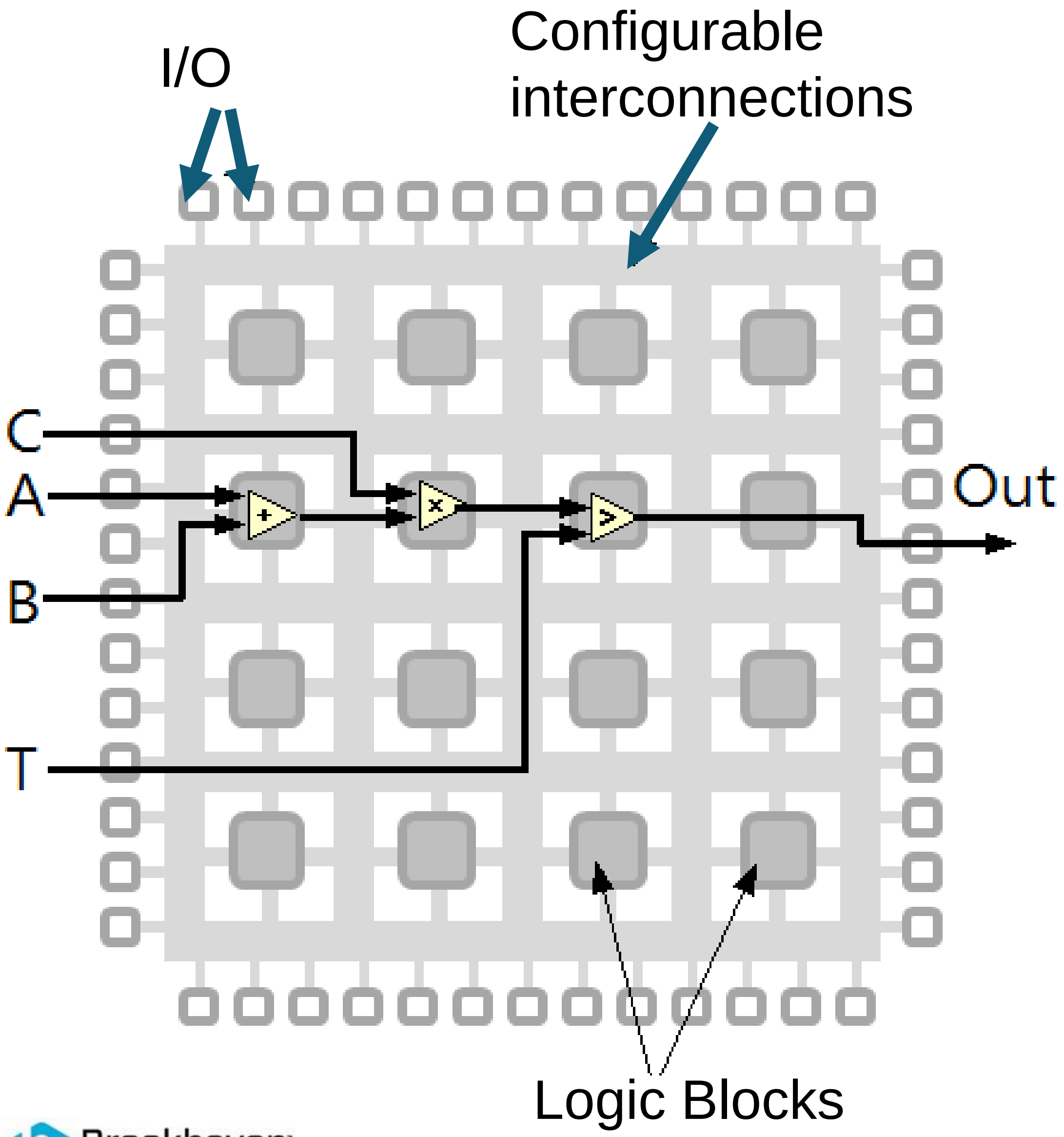
FPGA I/O

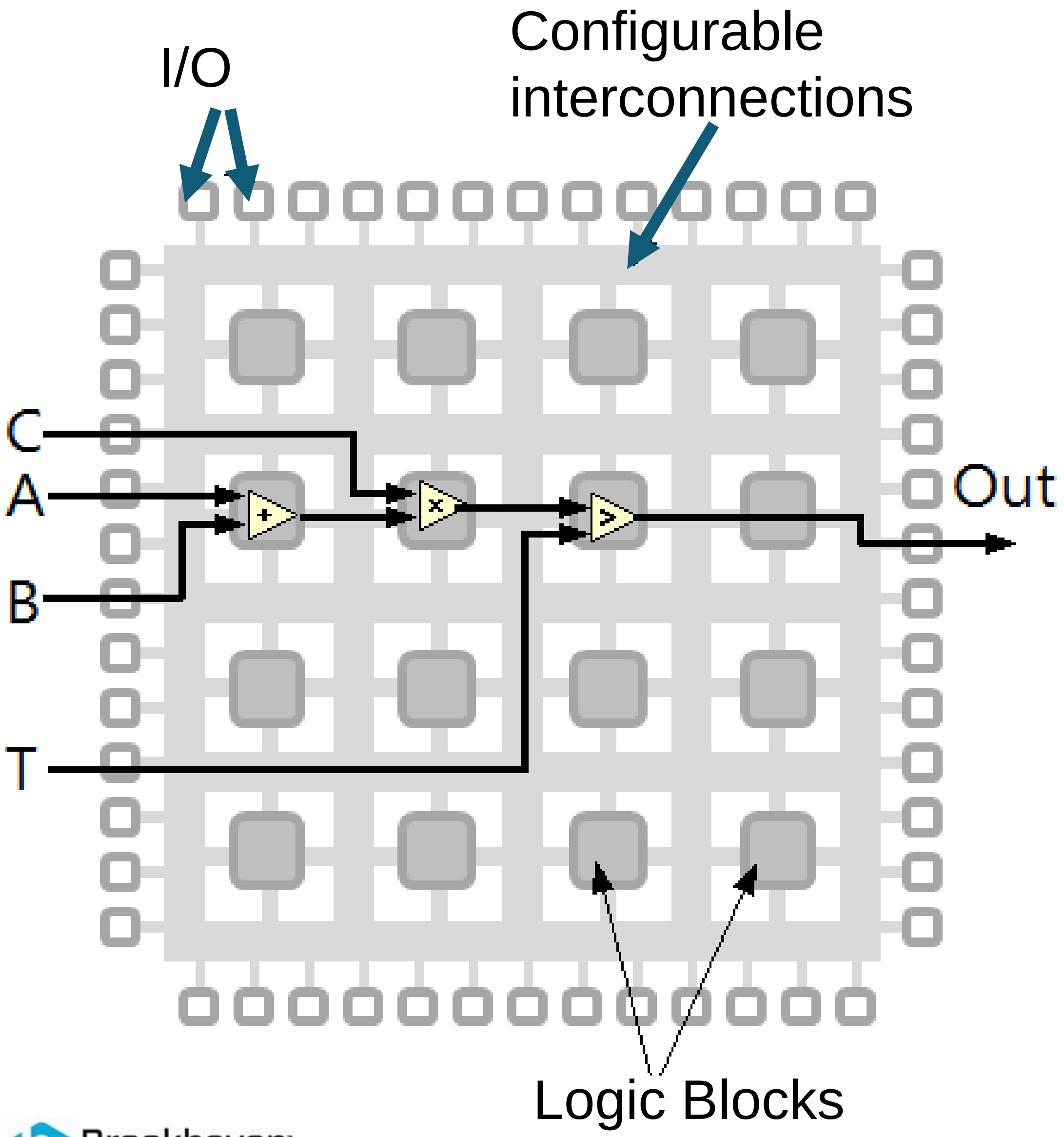


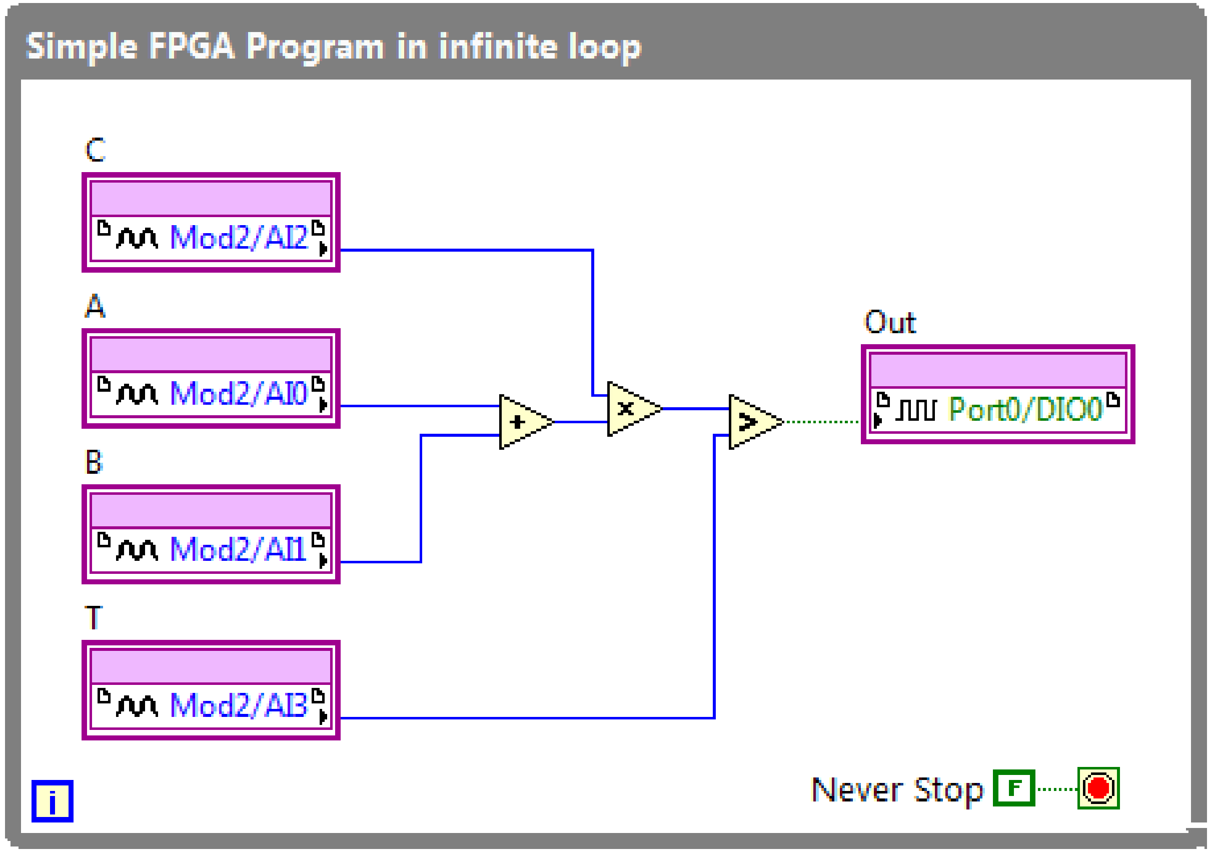
I/O

Configurable interconnections

Logic Blocks

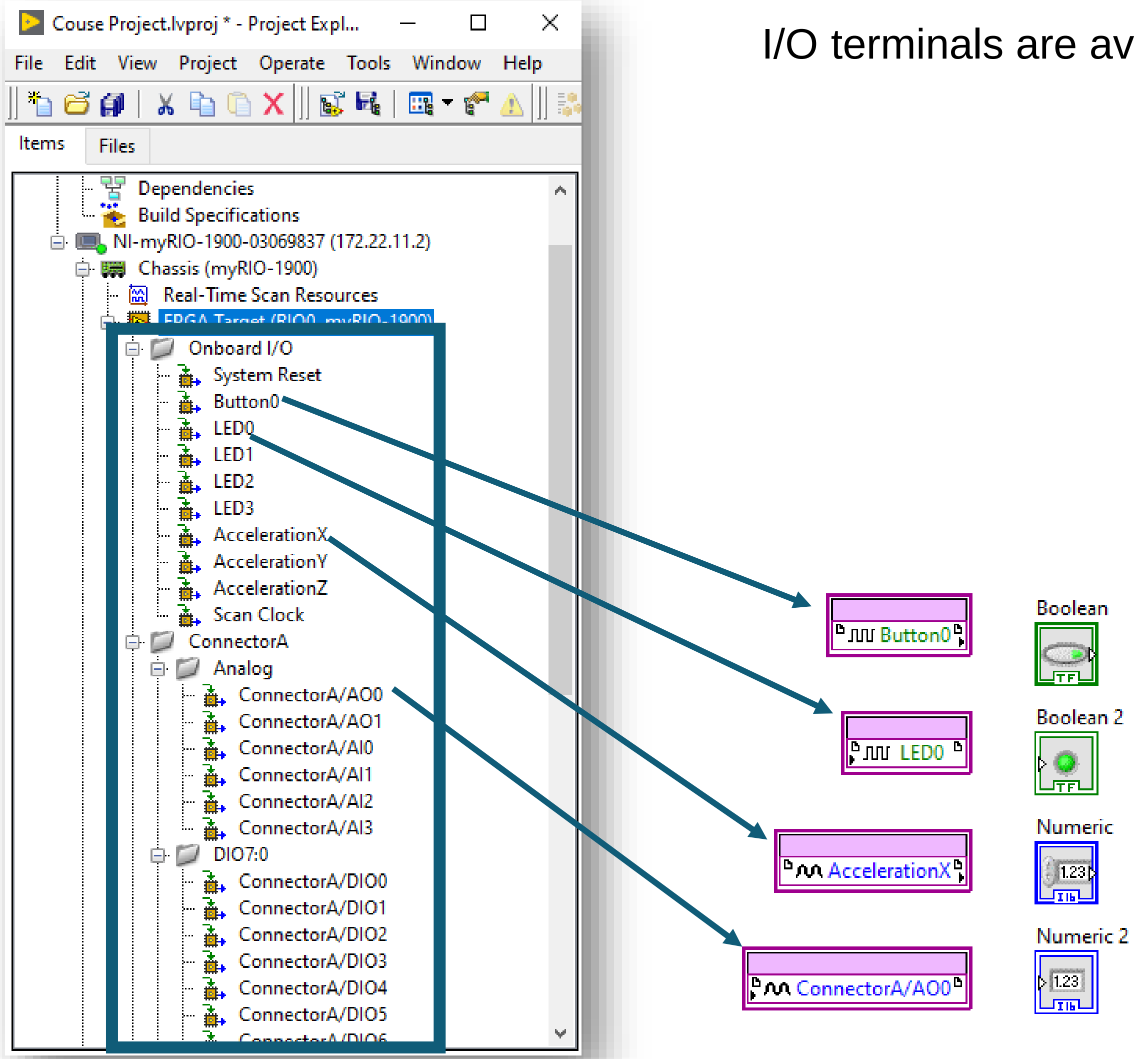
FPGA I/O

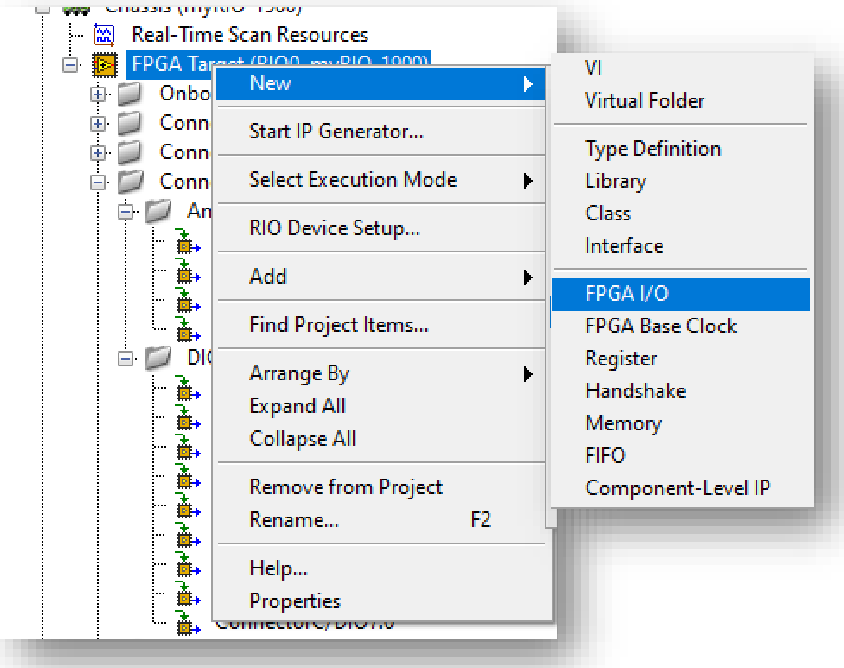

I/O
Configurable interconnections
C
A
B
T
+
×
>
Out
Logic Blocks


Simple FPGA Program in infinite loop
C
Mod2/AI2
A
Mod2/AI0
B
Mod2/AI1
T
Mod2/AI3
+
×
>
Out
Port0/DIO0
Never Stop
F
i

FPGA – I/O

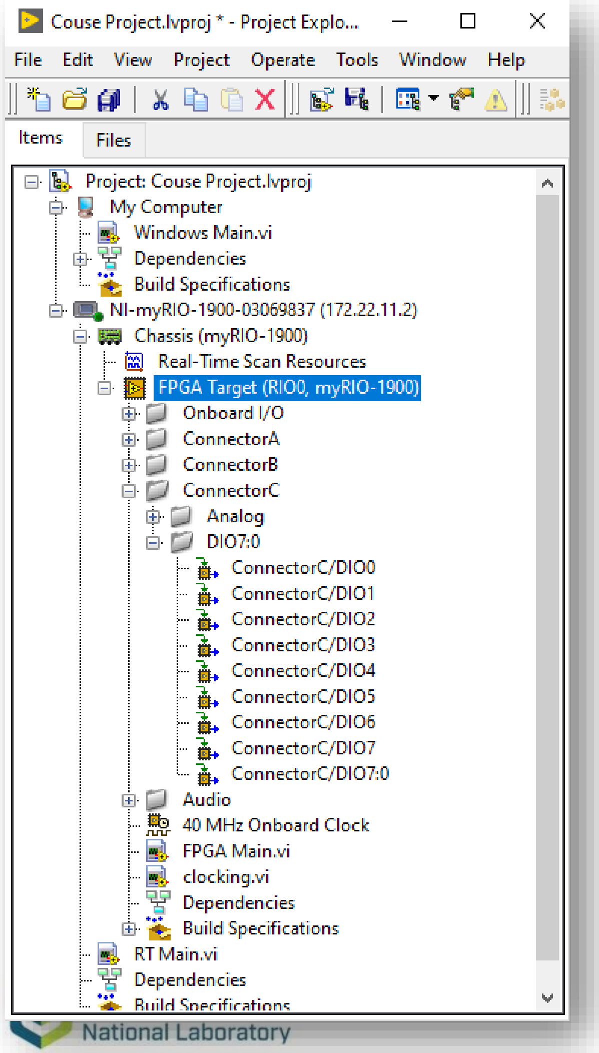
I/O terminals are available in a project window



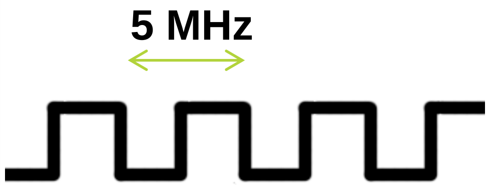


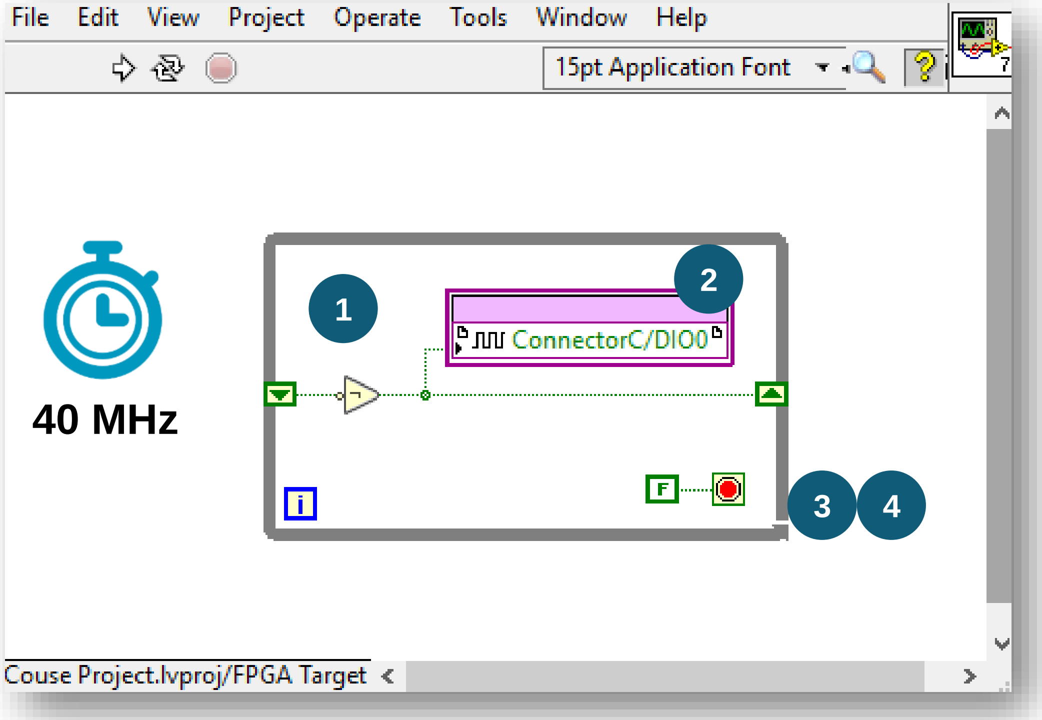
Single Operation Time

What’s the program speed?


Couse Project.lvproj * - Project Explo...
File Edit View Project Operate Tools Window Help
Items
Files

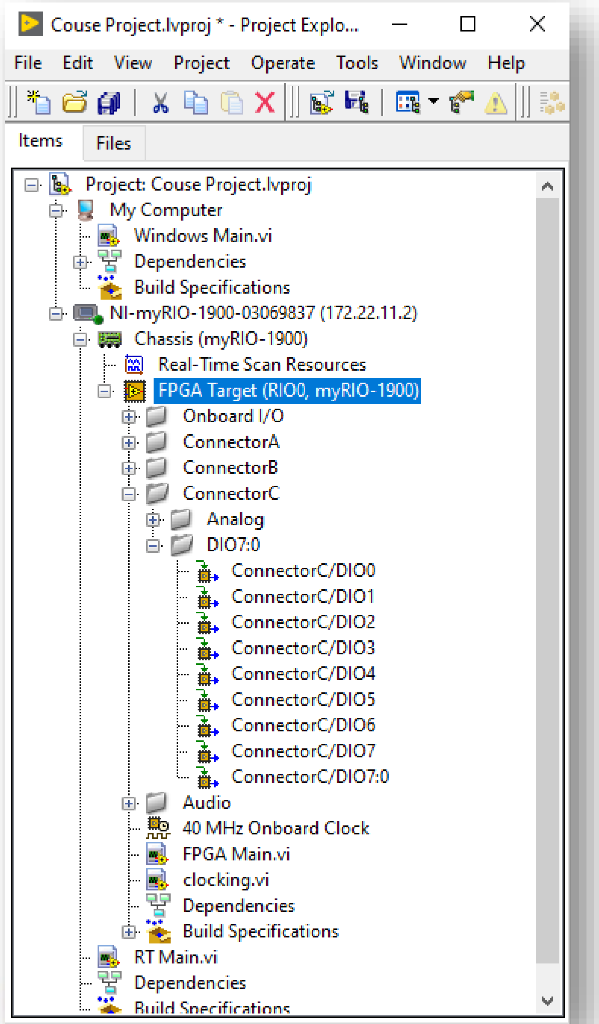
```
Project: Couse Project.lvproj
  My Computer
    Windows Main.vi
    Dependencies
    Build Specifications
  NI-myRIO-1900-03069837 (172.22.11.2)
    Chassis (myRIO-1900)
      Real-Time Scan Resources
      FPGA Target (RIO0, myRIO-1900)
        Onboard I/O
        ConnectorA
        ConnectorB
        ConnectorC
          Analog
          DIO7:0
            ConnectorC/DIO0
            ConnectorC/DIO1
            ConnectorC/DIO2
            ConnectorC/DIO3
            ConnectorC/DIO4
            ConnectorC/DIO5
            ConnectorC/DIO6
            ConnectorC/DIO7
            ConnectorC/DIO7:0
        Audio
        40 MHz Onboard Clock
        FPGA Main.vi
        clocking.vi
        Dependencies
        Build Specifications
    RT Main.vi
    Dependencies
    Build Specifications
```




File Edit View Project Operate Tools Window Help
15pt Application Font
40 MHz
1
2
ConnectorC/DIO0
F
i
3
4
Couse Project.lvproj/FPGA Target

1. “Not” functions requires one clk cycle to execute
2. Outputing a value to physical pin takes one clk cycle
3. While Loop requires two clk cycles to execute

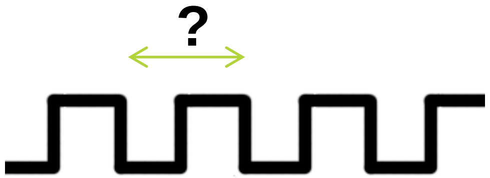
What’s the program speed ?

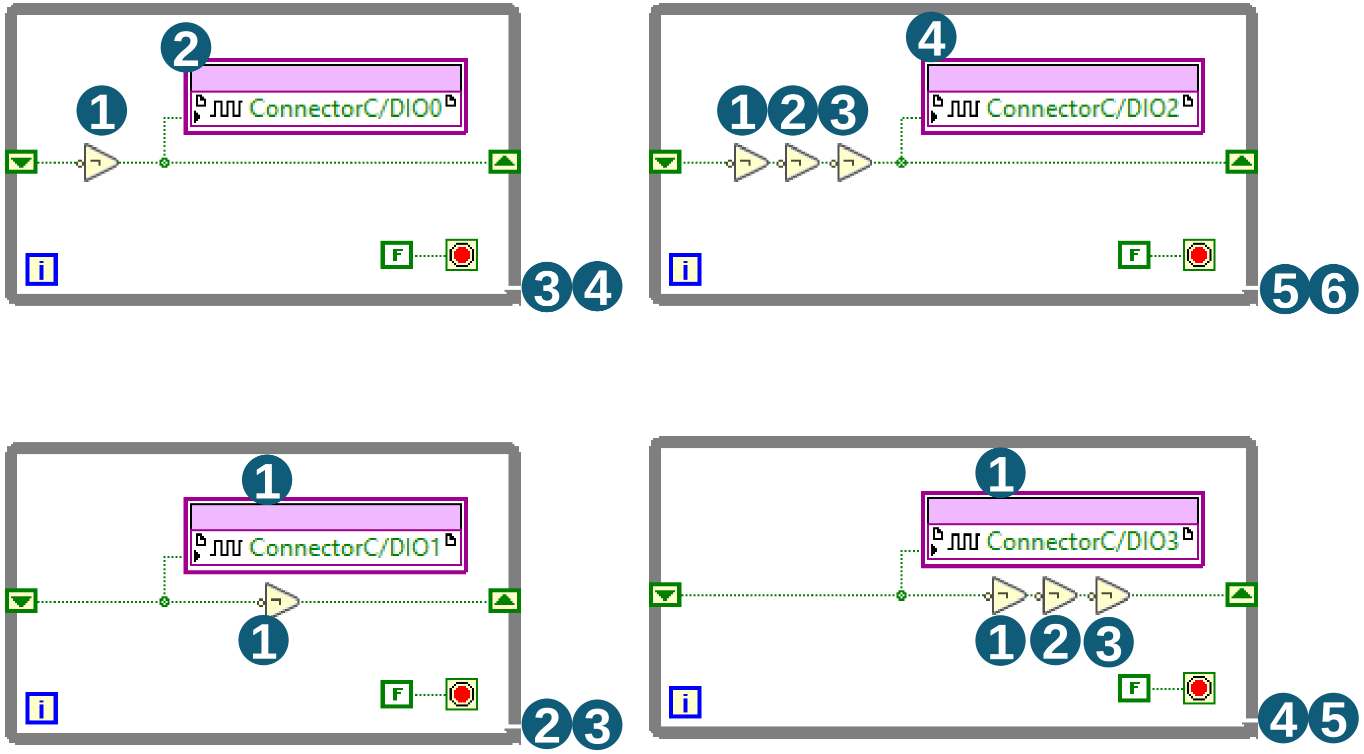


Couse Project.lvproj * - Project Explo...

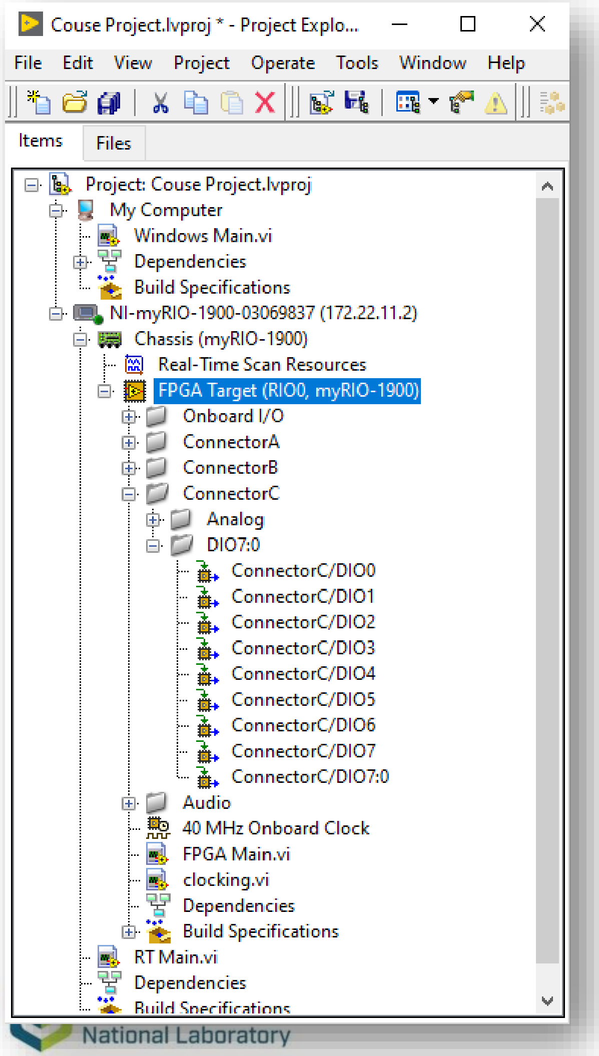
- Project: Couse Project.lvproj
  - My Computer
    - Windows Main.vi
    - Dependencies
    - Build Specifications
  - NI-myRIO-1900-03069837 (172.22.11.2)
    - Chassis (myRIO-1900)
      - Real-Time Scan Resources
      - FPGA Target (RIO0, myRIO-1900)
        - Onboard I/O
        - ConnectorA
        - ConnectorB
        - ConnectorC
          - Analog
          - DIO7:0
            - ConnectorC/DIO0
            - ConnectorC/DIO1
            - ConnectorC/DIO2
            - ConnectorC/DIO3
            - ConnectorC/DIO4
            - ConnectorC/DIO5
            - ConnectorC/DIO6
            - ConnectorC/DIO7
            - ConnectorC/DIO7:0
        - Audio
        - 40 MHz Onboard Clock
        - FPGA Main.vi
        - clocking.vi
        - Dependencies
        - Build Specifications
    - RT Main.vi
    - Dependencies
    - Build Specifications

Top-Level Clock = 40 MHz





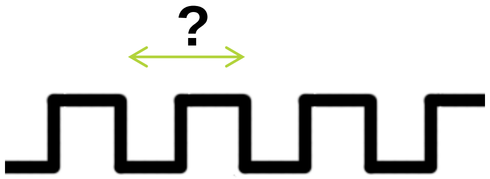
What’s the program speed ?

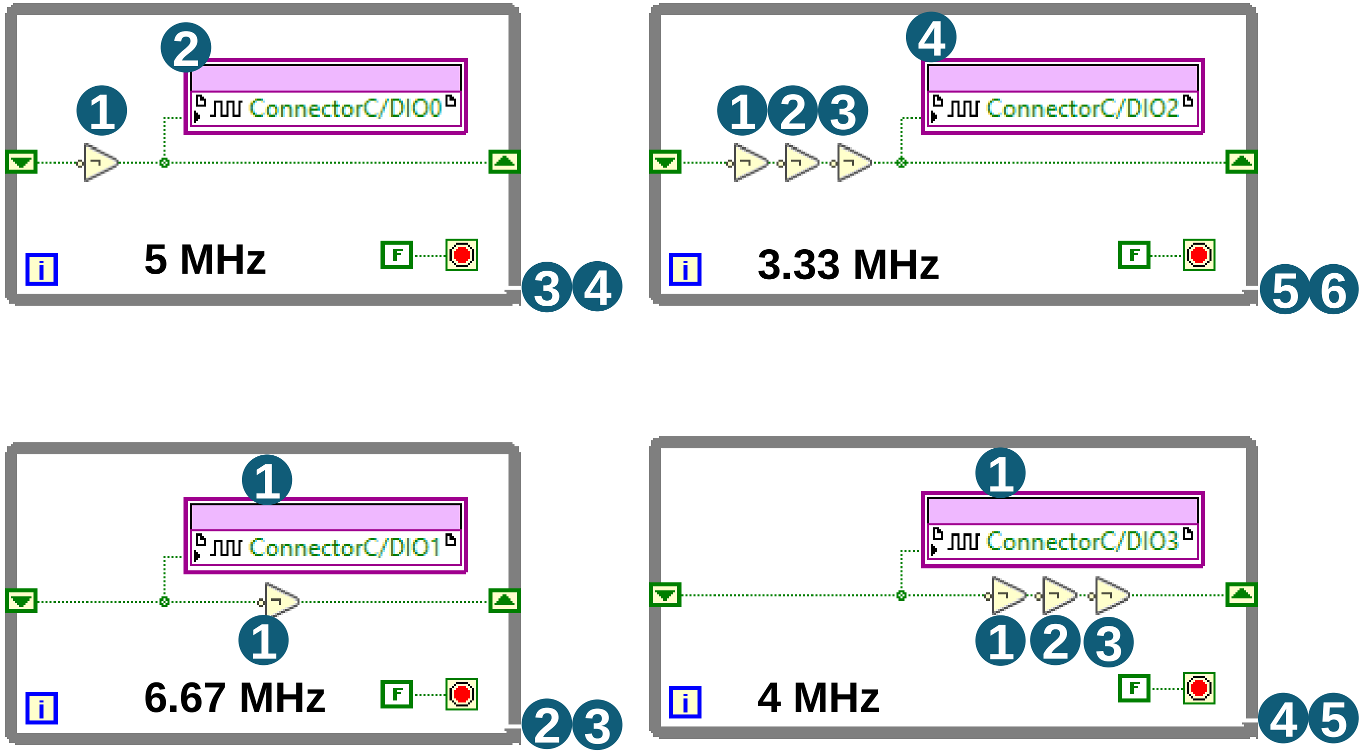


Couse Project.lvproj * - Project Explo...

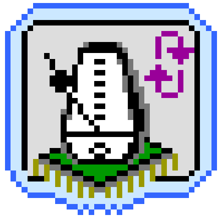
- Project: Couse Project.lvproj
  - My Computer
    - Windows Main.vi
    - Dependencies
    - Build Specifications
  - NI-myRIO-1900-03069837 (172.22.11.2)
    - Chassis (myRIO-1900)
      - Real-Time Scan Resources
      - FPGA Target (RIO0, myRIO-1900)
        - Onboard I/O
        - ConnectorA
        - ConnectorB
        - ConnectorC
          - Analog
          - DIO7:0
            - ConnectorC/DIO0
            - ConnectorC/DIO1
            - ConnectorC/DIO2
            - ConnectorC/DIO3
            - ConnectorC/DIO4
            - ConnectorC/DIO5
            - ConnectorC/DIO6
            - ConnectorC/DIO7
            - ConnectorC/DIO7:0
        - Audio
        - 40 MHz Onboard Clock
        - FPGA Main.vi
        - clocking.vi
        - Dependencies
        - Build Specifications
    - RT Main.vi
    - Dependencies
    - Build Specifications

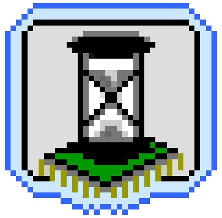
Top-Level Clock = 40 MHz

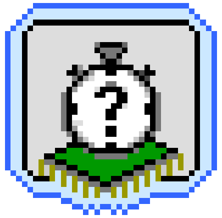


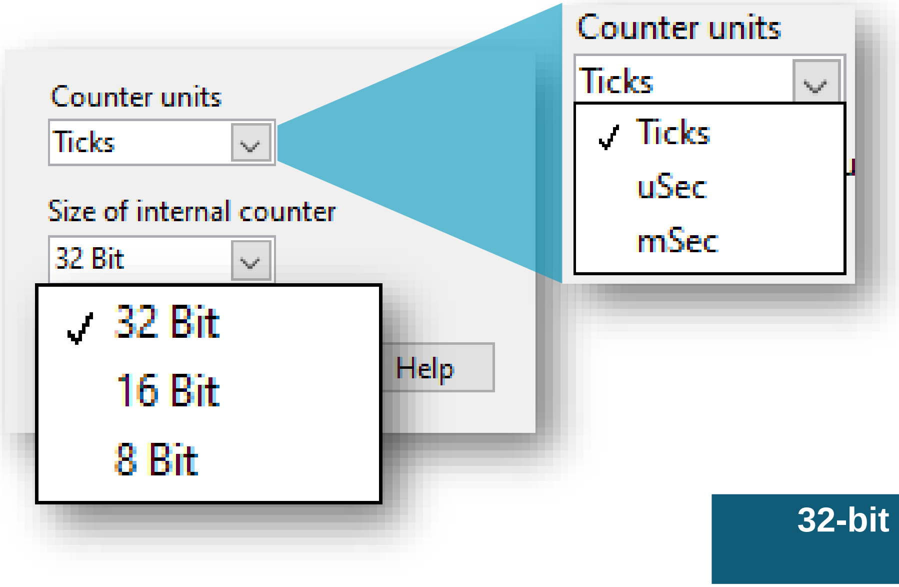


TIMING in FPGA









Counter units

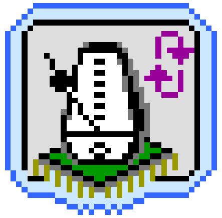
Ticks

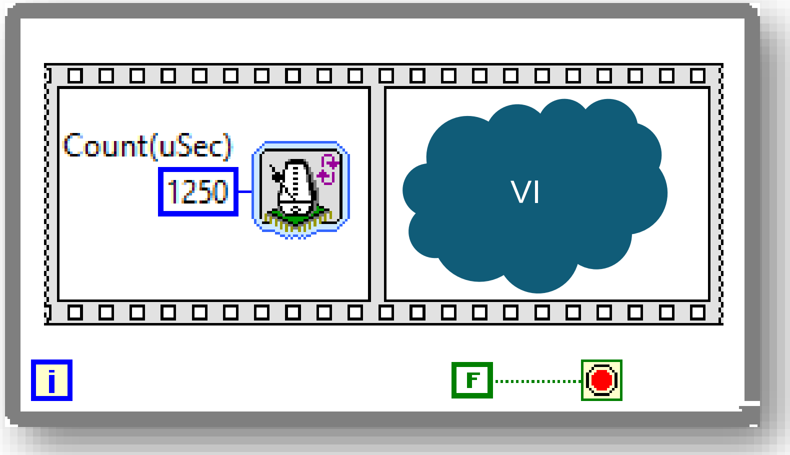
Size of internal counter

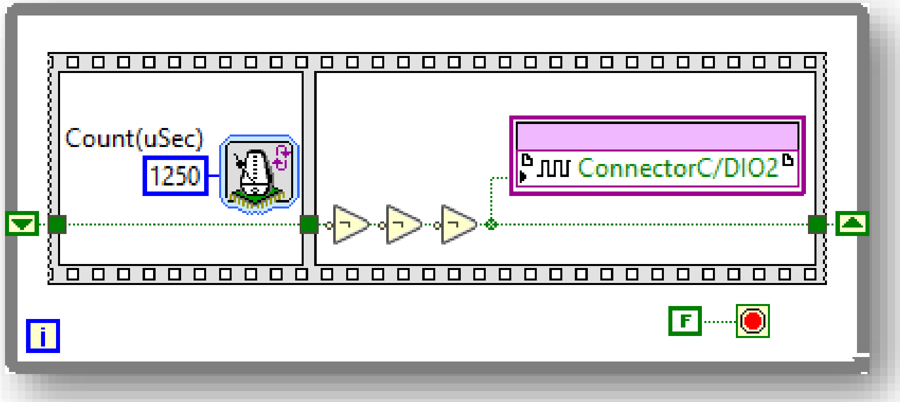
32 Bit

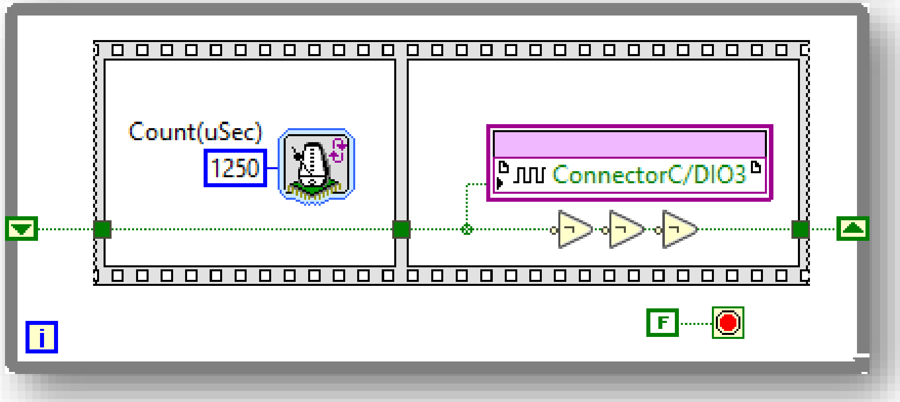
32-bit	1 do 4,294,967,296 tików	1 µs do 71 minut	1 ms do 49 dni
16-bit	1 do 65,536 tików	1 µs do 65 ms	1 ms do 65 s
8-bit	1 do 256 tików	1 µs do 256 µs	1 ms to 256 ms

TIMING IN FPGA - example

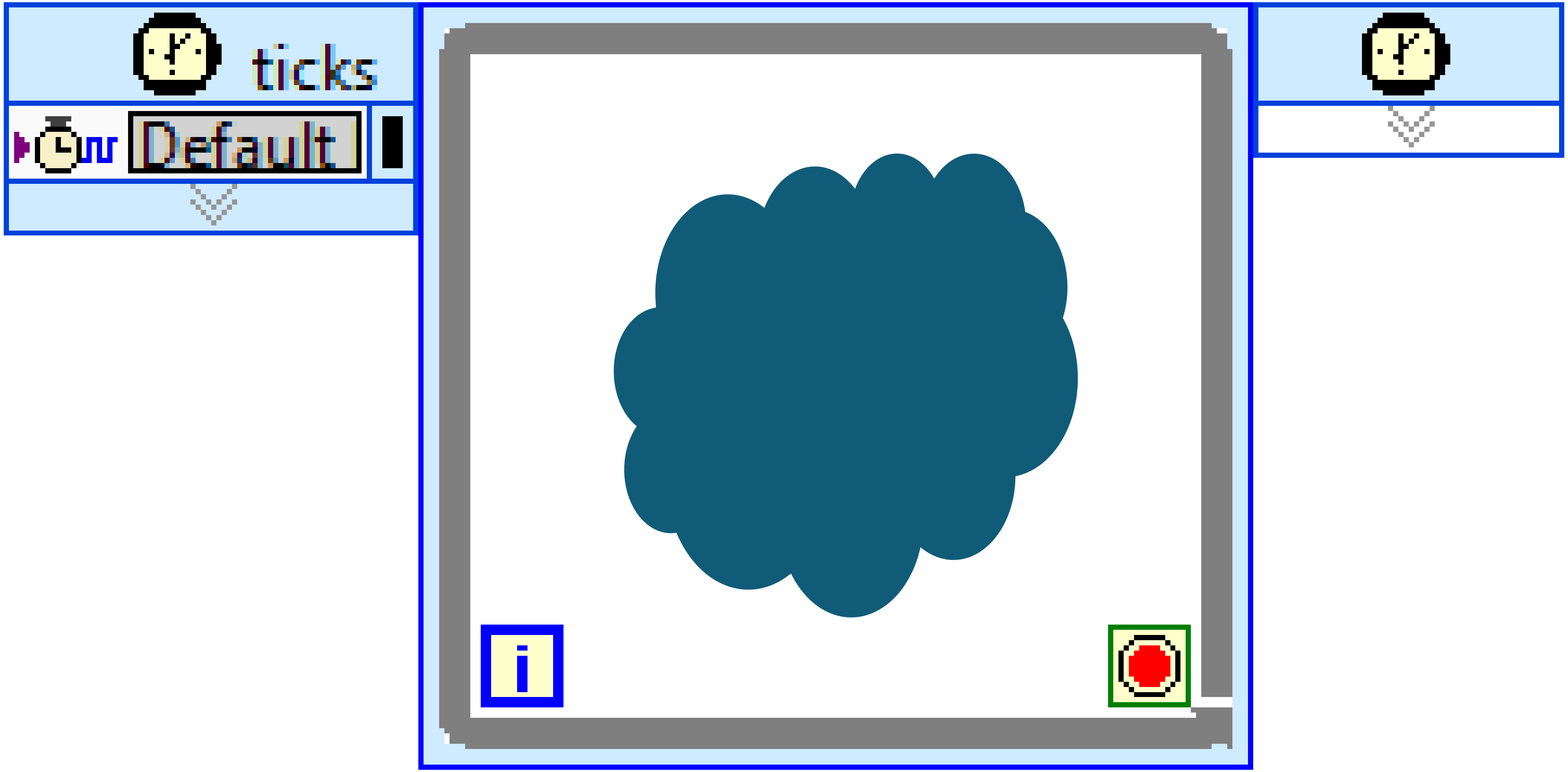




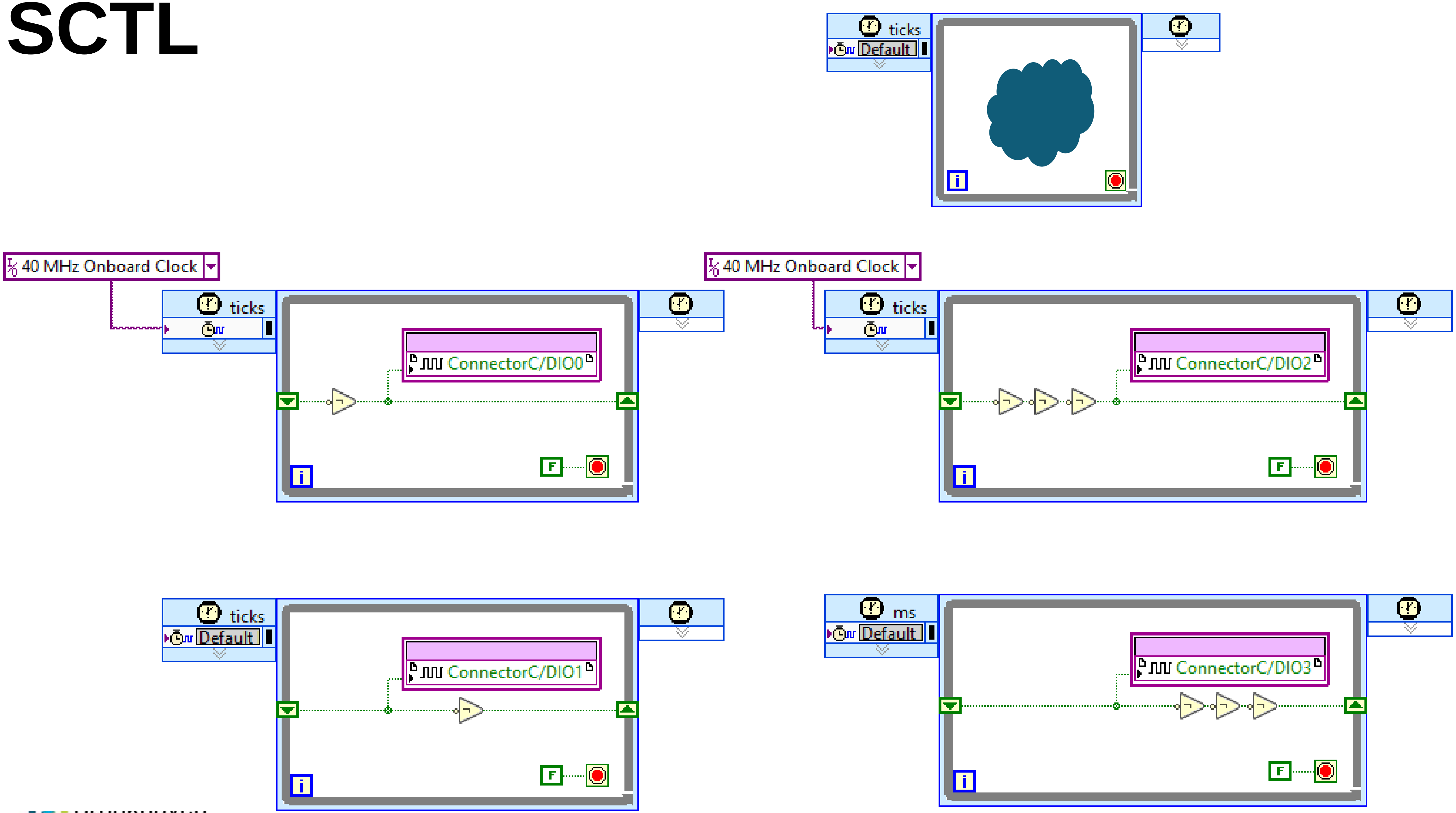




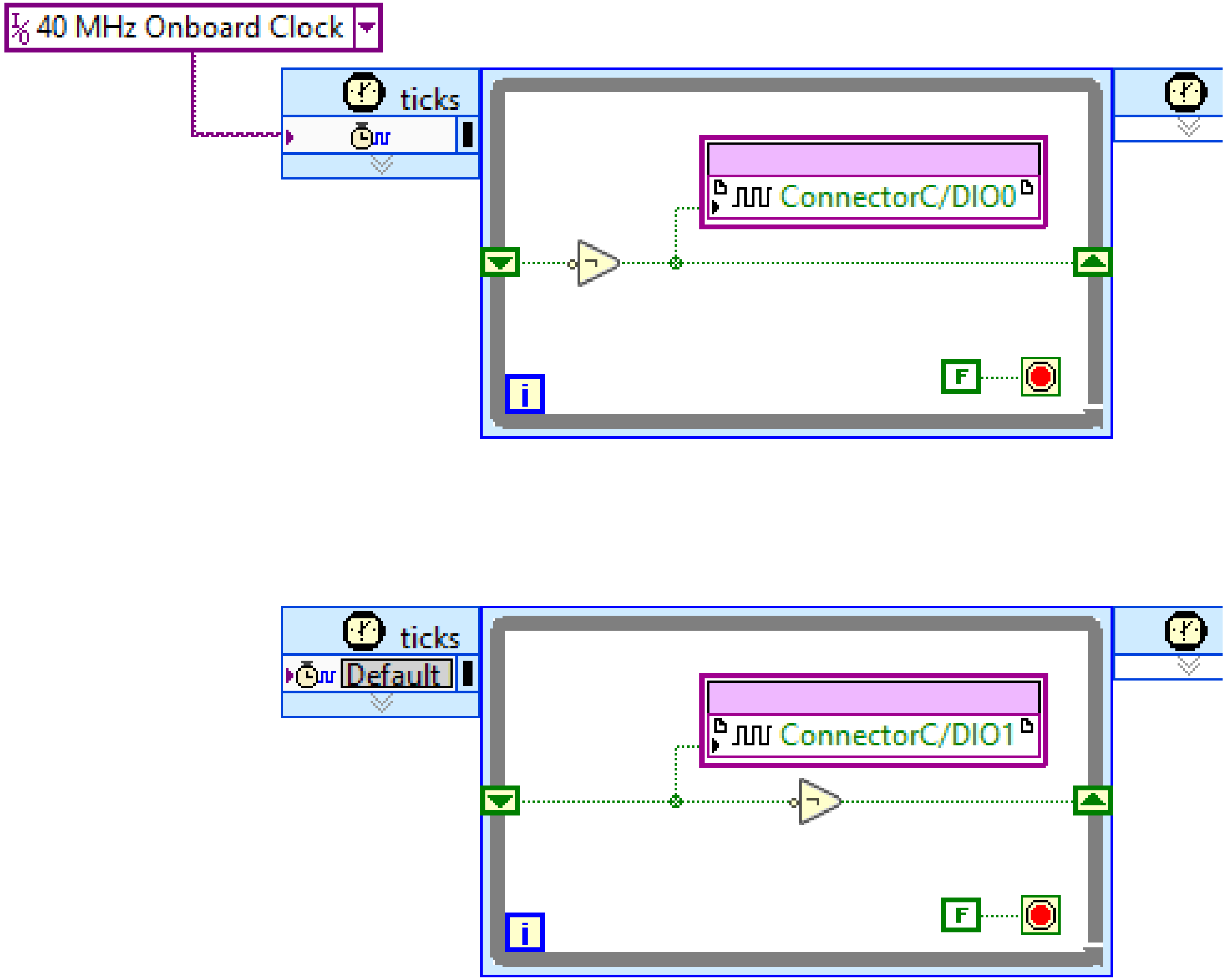
SINGLE-CYCLE TIMED LOOP



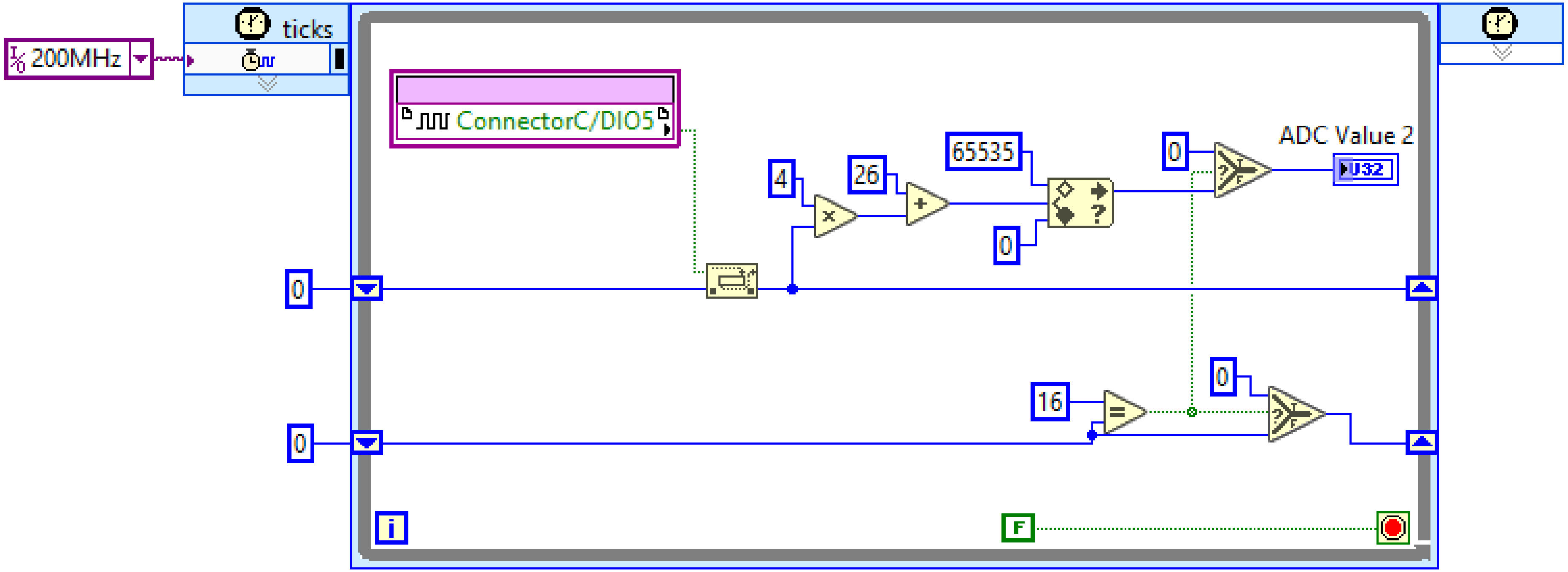
SCTL


ticks
Default
40 MHz Onboard Clock
ticks
ConnectorC/DIO0
F
40 MHz Onboard Clock
ticks
ConnectorC/DIO2
F
ticks
Default
ConnectorC/DIO1
F
ms
Default
ConnectorC/DIO3
F

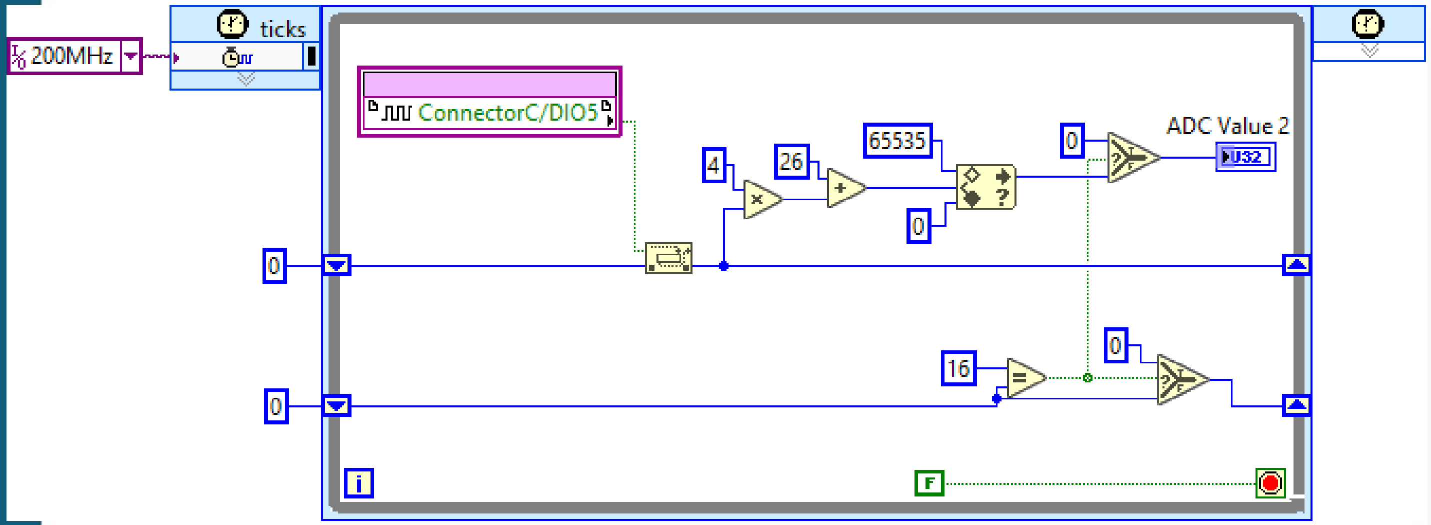
SCTL

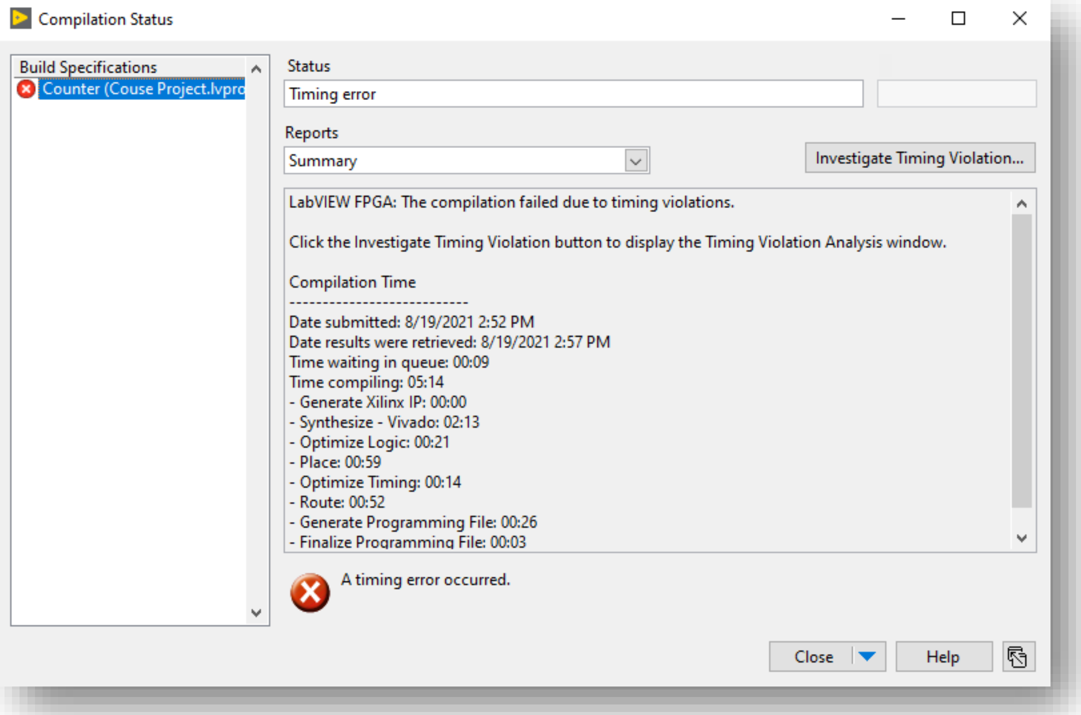

40 MHz Onboard Clock
ticks
ConnectorC/DIO0
F
i
ticks
Default
ConnectorC/DIO1
F
i

SCTL


200MHz
ticks
ConnectorC/DIO5
4
26
65535
0
ADC Value 2
U32
0
0
16
0
0
F
i

SCTL





Counter (Couse Project.lvpro

Status: Timing error

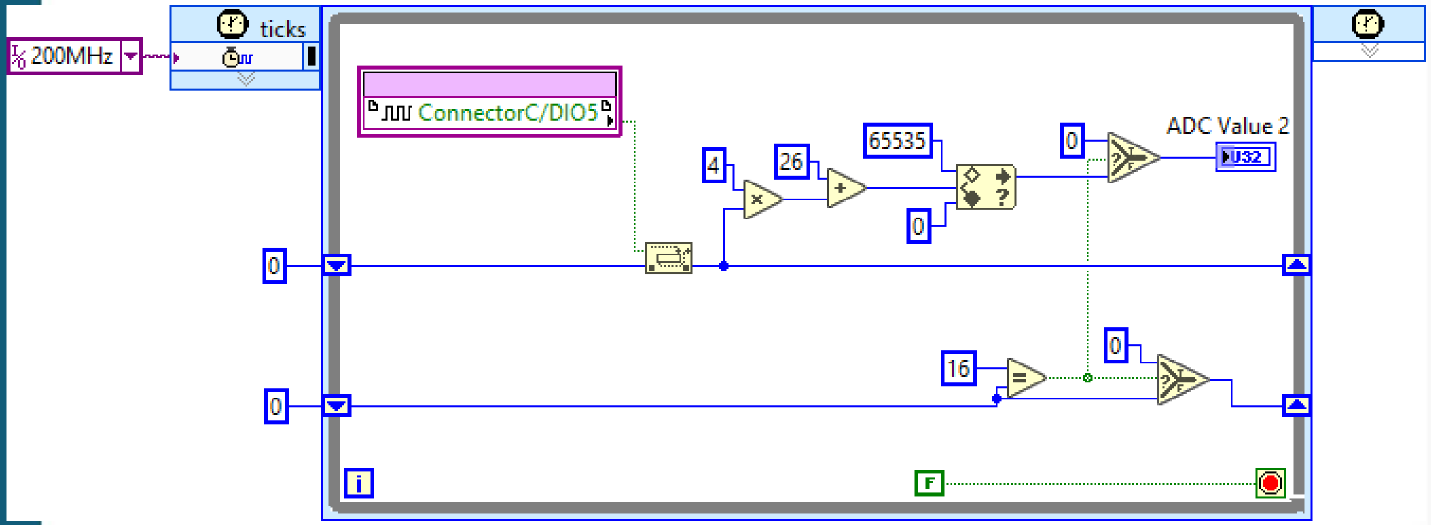
Reports: Summary

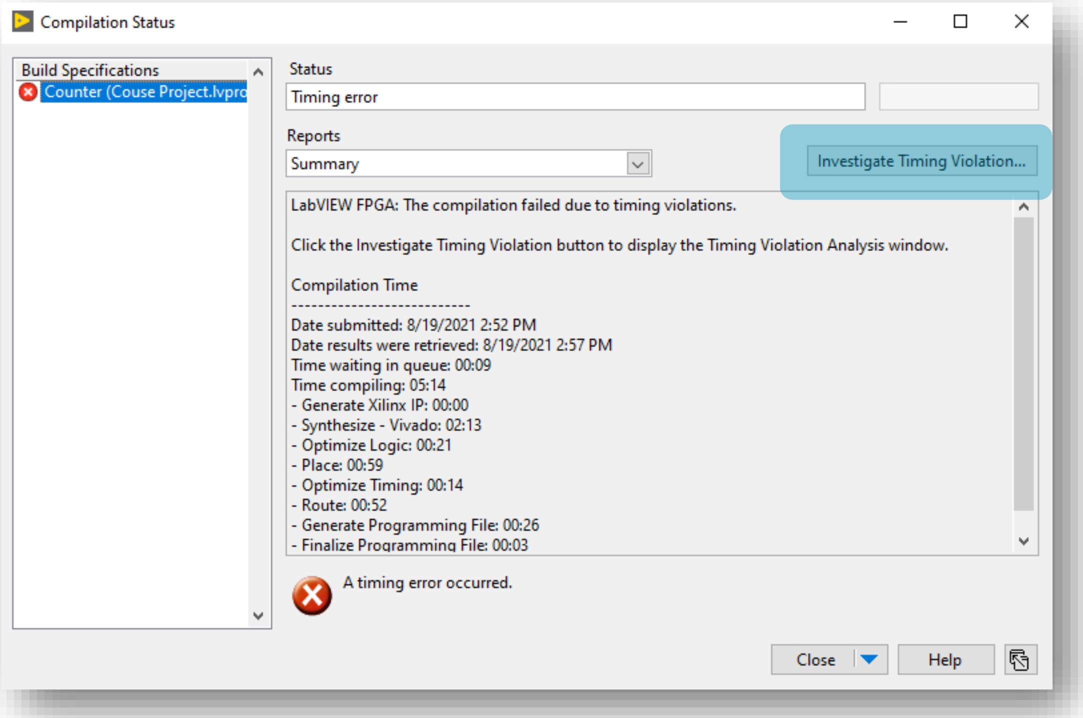
Investigate Timing Violation...

```
LabVIEW FPGA: The compilation failed due to timing violations.

Click the Investigate Timing Violation button to display the Timing Violation Analysis window.

Compilation Time
---------------------------
Date submitted: 8/19/2021 2:52 PM
Date results were retrieved: 8/19/2021 2:57 PM
Time waiting in queue: 00:09
Time compiling: 05:14
- Generate Xilinx IP: 00:00
- Synthesize - Vivado: 02:13
- Optimize Logic: 00:21
- Place: 00:59
- Optimize Timing: 00:14
- Route: 00:52
- Generate Programming File: 00:26
- Finalize Programming File: 00:03
```

A timing error occurred.

SCTL





Status

Timing error

Reports

Summary

LabVIEW FPGA: The compilation failed due to timing violations.

Click the Investigate Timing Violation button to display the Timing Violation Analysis window.

```
Compilation Time
---------------------------
Date submitted: 8/19/2021 2:52 PM
Date results were retrieved: 8/19/2021 2:57 PM
Time waiting in queue: 00:09
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- Generate Xilinx IP: 00:00
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- Optimize Logic: 00:21
- Place: 00:59
- Optimize Timing: 00:14
- Route: 00:52
- Generate Programming File: 00:26
- Finalize Programming File: 00:03
```
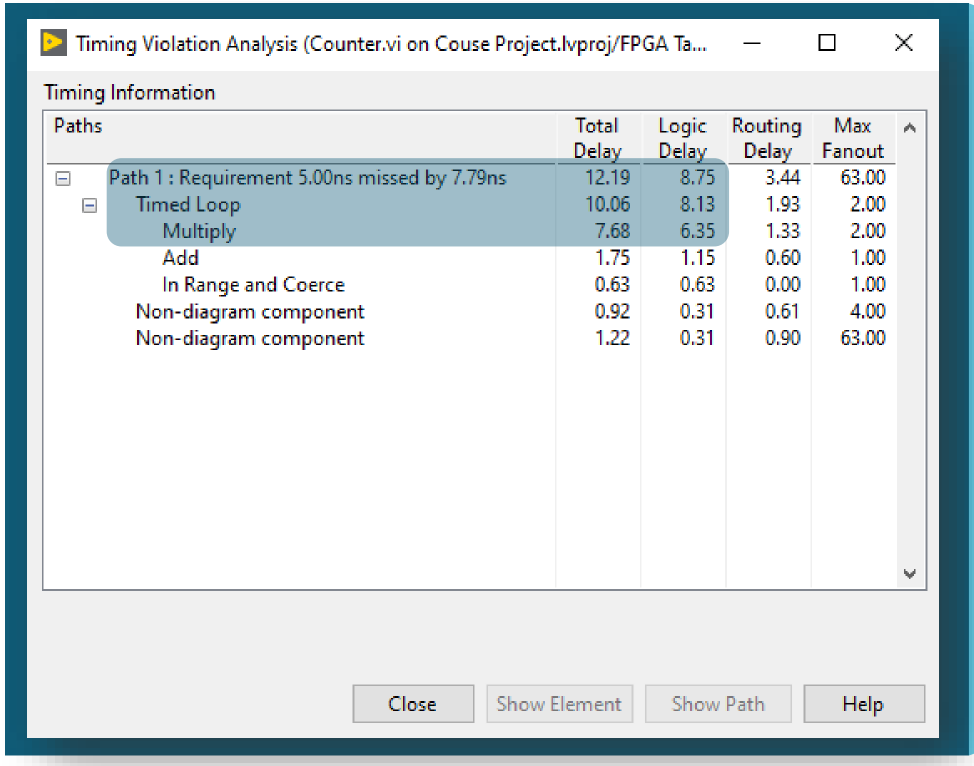
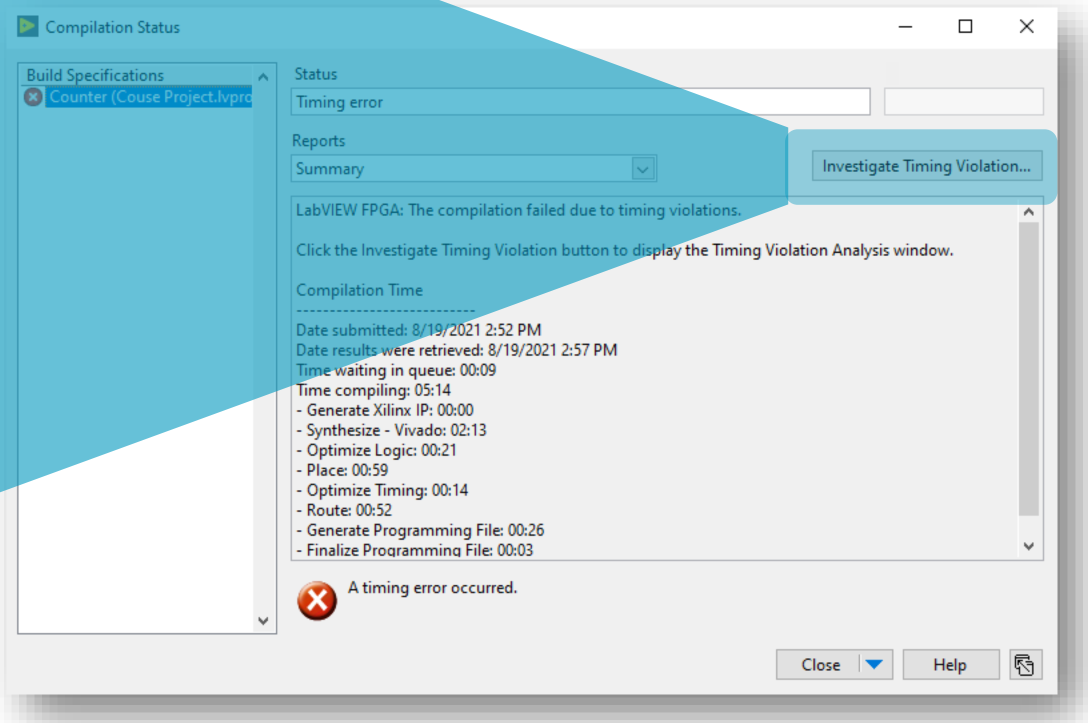

A timing error occurred.

SCTL


Timing Violation Analysis (Counter.vi on Couse Project.lvproj/FPGA Ta...
Close
Show Element
Show Path
Help

Timing Information

Paths	Total Delay	Logic Delay	Routing Delay	Max Fanout
⊟ Path 1 : Requirement 5.00ns missed by 7.79ns	12.19	8.75	3.44	63.00
⊟ Timed Loop	10.06	8.13	1.93	2.00
Multiply	7.68	6.35	1.33	2.00
Add	1.75	1.15	0.60	1.00
In Range and Coerce	0.63	0.63	0.00	1.00
Non-diagram component	0.92	0.31	0.61	4.00
Non-diagram component	1.22	0.31	0.90	63.00



Status: Timing error

Reports: Summary

```
LabVIEW FPGA: The compilation failed due to timing violations.

Click the Investigate Timing Violation button to display the Timing Violation Analysis window.

Compilation Time
---------------------------
Date submitted: 8/19/2021 2:52 PM
Date results were retrieved: 8/19/2021 2:57 PM
Time waiting in queue: 00:09
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- Optimize Logic: 00:21
- Place: 00:59
- Optimize Timing: 00:14
- Route: 00:52
- Generate Programming File: 00:26
- Finalize Programming File: 00:03
```
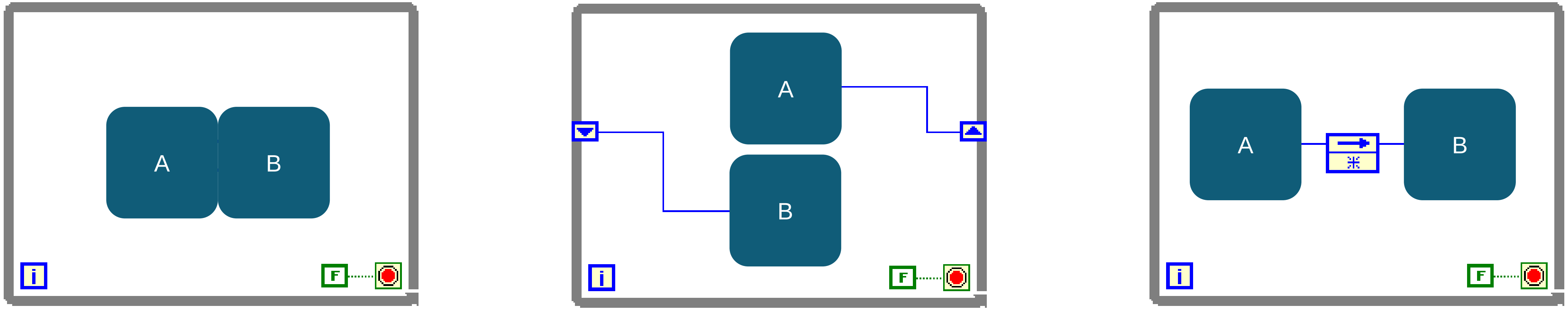
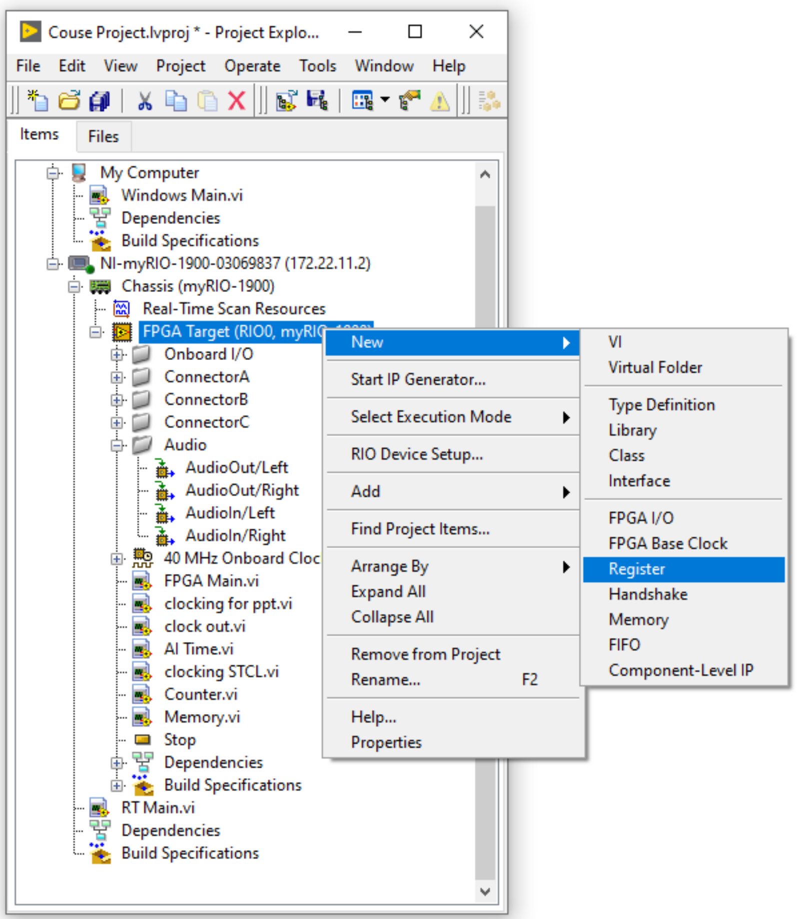
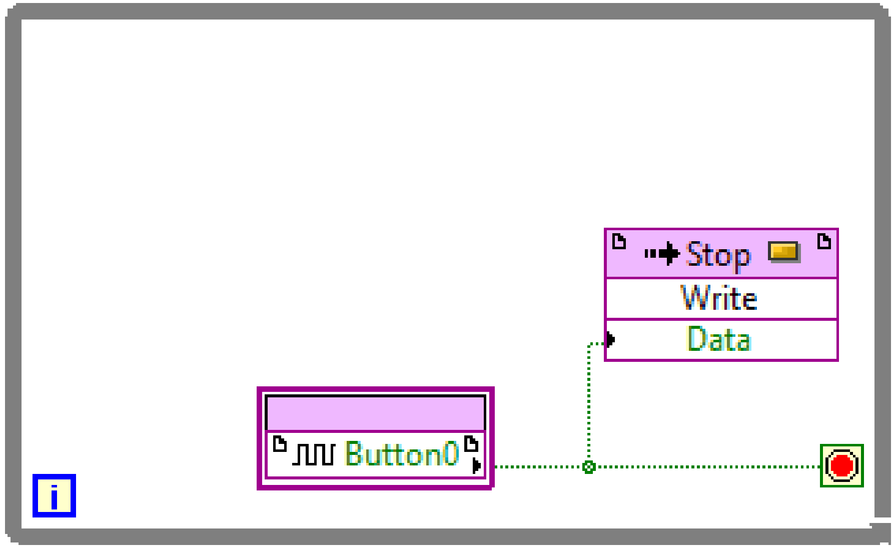

A timing error occurred.

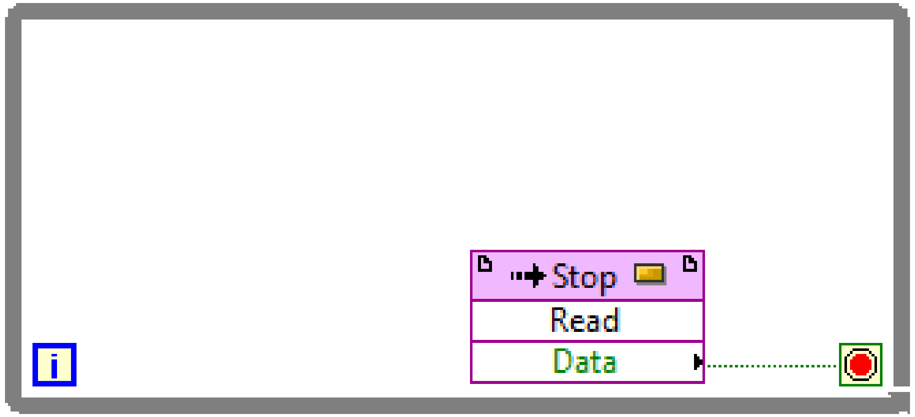
PIPELINE



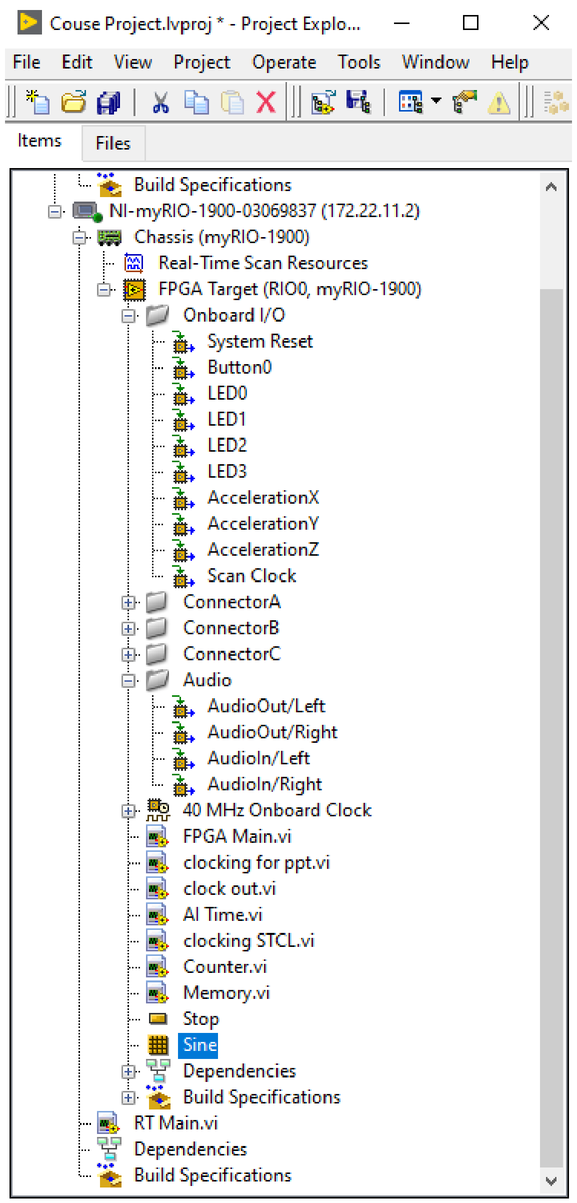
Register


Couse Project.lvproj * - Project Explo...
File Edit View Project Operate Tools Window Help
Items Files
My Computer
Windows Main.vi
Dependencies
Build Specifications
NI-myRIO-1900-03069837 (172.22.11.2)
Chassis (myRIO-1900)
Real-Time Scan Resources
FPGA Target (RIO0, myRIO-1900)
Onboard I/O
ConnectorA
ConnectorB
ConnectorC
Audio
AudioOut/Left
AudioOut/Right
AudioIn/Left
AudioIn/Right
40 MHz Onboard Cloc
FPGA Main.vi
clocking for ppt.vi
clock out.vi
AI Time.vi
clocking STCL.vi
Counter.vi
Memory.vi
Stop
Dependencies
Build Specifications
RT Main.vi
Dependencies
Build Specifications
New
Start IP Generator...
Select Execution Mode
RIO Device Setup...
Add
Find Project Items...
Arrange By
Expand All
Collapse All
Remove from Project
Rename... F2
Help...
Properties
VI
Virtual Folder
Type Definition
Library
Class
Interface
FPGA I/O
FPGA Base Clock
Register
Handshake
Memory
FIFO
Component-Level IP

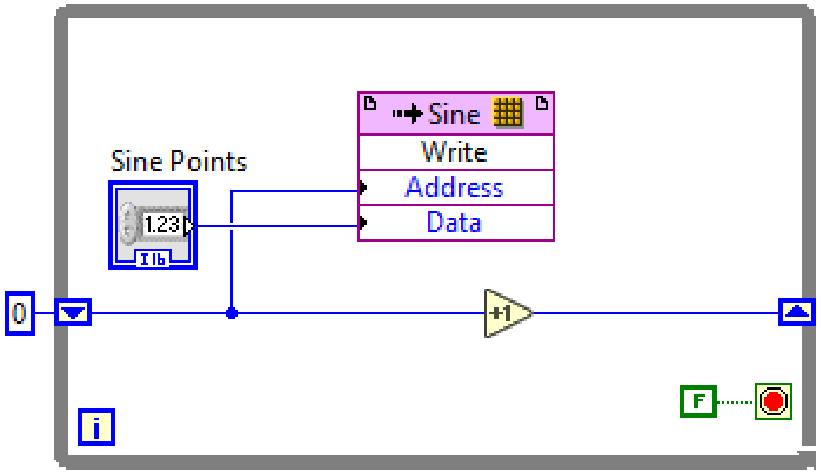

Stop
Write
Data
Button0
i

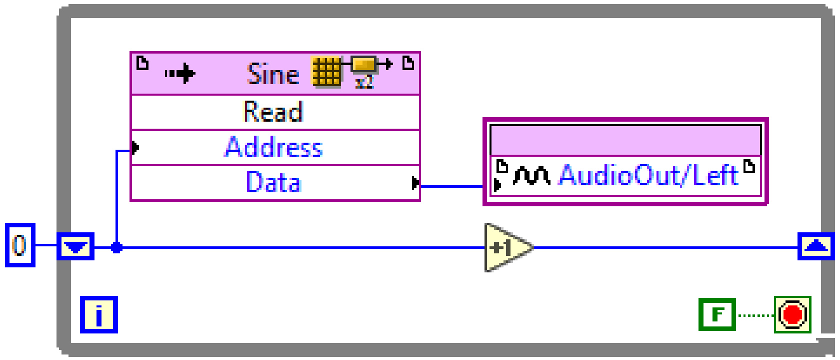

Stop
Read
Data
i

Memory


Couse Project.lvproj * - Project Explo...
File Edit View Project Operate Tools Window Help
Items Files

- Build Specifications
- NI-myRIO-1900-03069837 (172.22.11.2)
  - Chassis (myRIO-1900)
    - Real-Time Scan Resources
    - FPGA Target (RIO0, myRIO-1900)
      - Onboard I/O
        - System Reset
        - Button0
        - LED0
        - LED1
        - LED2
        - LED3
        - AccelerationX
        - AccelerationY
        - AccelerationZ
        - Scan Clock
      - ConnectorA
      - ConnectorB
      - ConnectorC
      - Audio
        - AudioOut/Left
        - AudioOut/Right
        - AudioIn/Left
        - AudioIn/Right
      - 40 MHz Onboard Clock
      - FPGA Main.vi
      - clocking for ppt.vi
      - clock out.vi
      - AI Time.vi
      - clocking STCL.vi
      - Counter.vi
      - Memory.vi
      - Stop
      - Sine
      - Dependencies
      - Build Specifications
  - RT Main.vi
  - Dependencies
  - Build Specifications





+ easy to configure

+ similar to an array

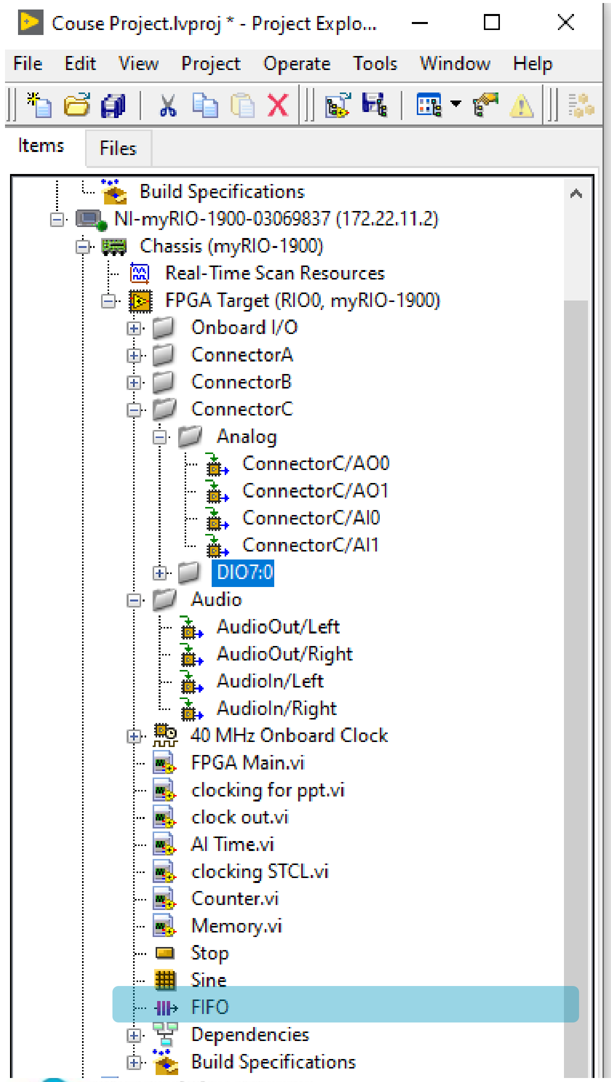
+ doesn’t require contro/indicator

+ no data copies

+ can be a type defined

- no synchronization methods

FIFO


Couse Project.lvproj * - Project Explo...
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Items Files

Build Specifications
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ConnectorC/AO1
ConnectorC/AI0
ConnectorC/AI1
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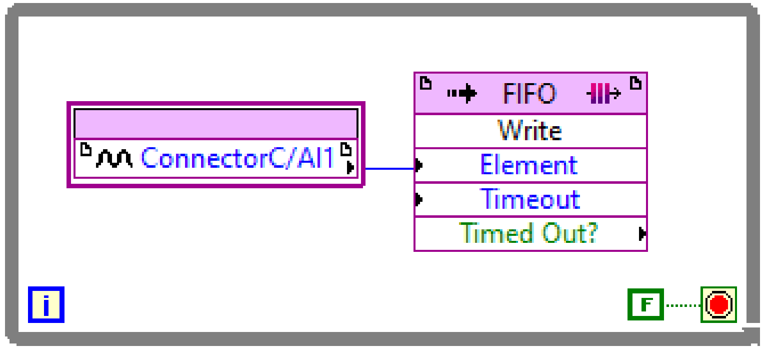
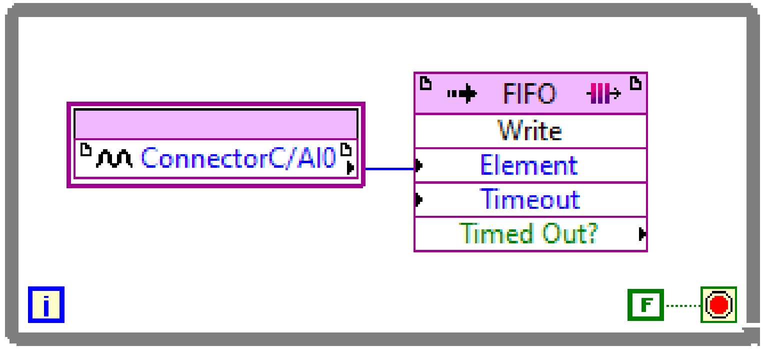
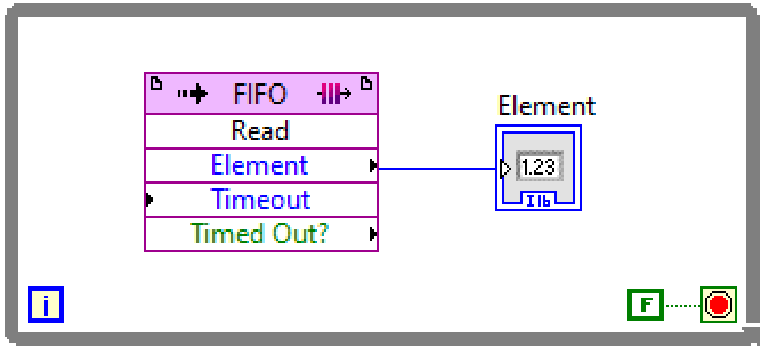
clocking for ppt.vi
clock out.vi
AI Time.vi
clocking STCL.vi
Counter.vi
Memory.vi
Stop
Sine
FIFO
Dependencies
Build Specifications







+ easy to configure

+ similar to standard FIFOs

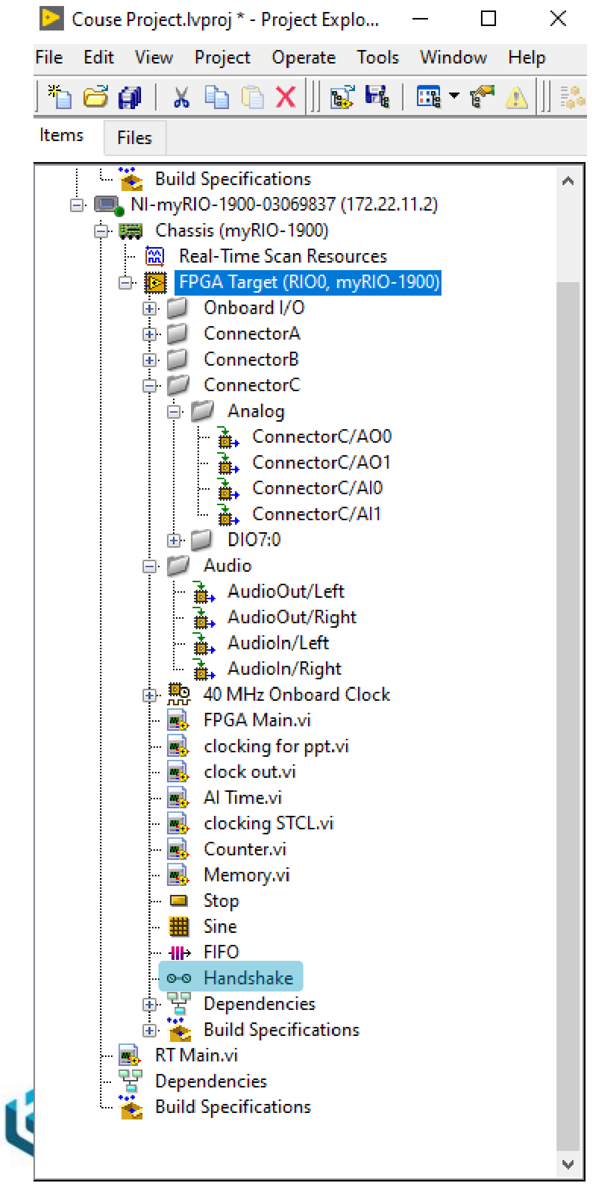
+ no control/indicator needed

+ no data copies

+ may be a typedef

- Arbitration needs to be considered

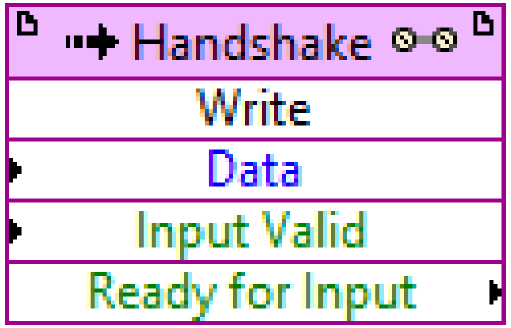
HANDSHAKE

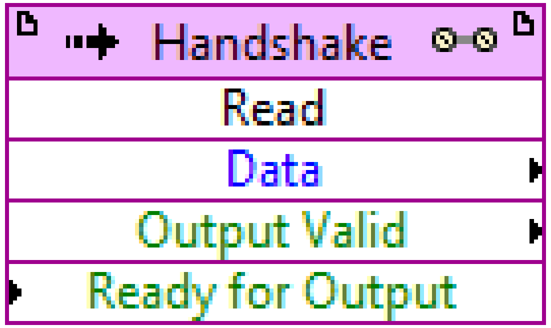

Couse Project.lvproj * - Project Explo...

File Edit View Project Operate Tools Window Help

Items Files

- Build Specifications
- NI-myRIO-1900-03069837 (172.22.11.2)
  - Chassis (myRIO-1900)
    - Real-Time Scan Resources
    - FPGA Target (RIO0, myRIO-1900)
      - Onboard I/O
      - ConnectorA
      - ConnectorB
      - ConnectorC
        - Analog
          - ConnectorC/AO0
          - ConnectorC/AO1
          - ConnectorC/AI0
          - ConnectorC/AI1
        - DIO7:0
      - Audio
        - AudioOut/Left
        - AudioOut/Right
        - AudioIn/Left
        - AudioIn/Right
      - 40 MHz Onboard Clock
      - FPGA Main.vi
      - clocking for ppt.vi
      - clock out.vi
      - AI Time.vi
      - clocking STCL.vi
      - Counter.vi
      - Memory.vi
      - Stop
      - Sine
      - FIFO
      - Handshake
      - Dependencies
      - Build Specifications
  - RT Main.vi
  - Dependencies
  - Build Specifications





+ easy to configure

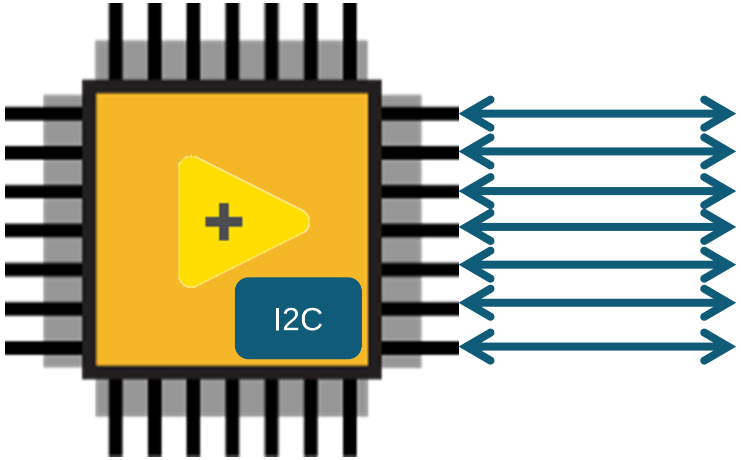
+ use as single-element FIFO

+ no control required

+ no data copy

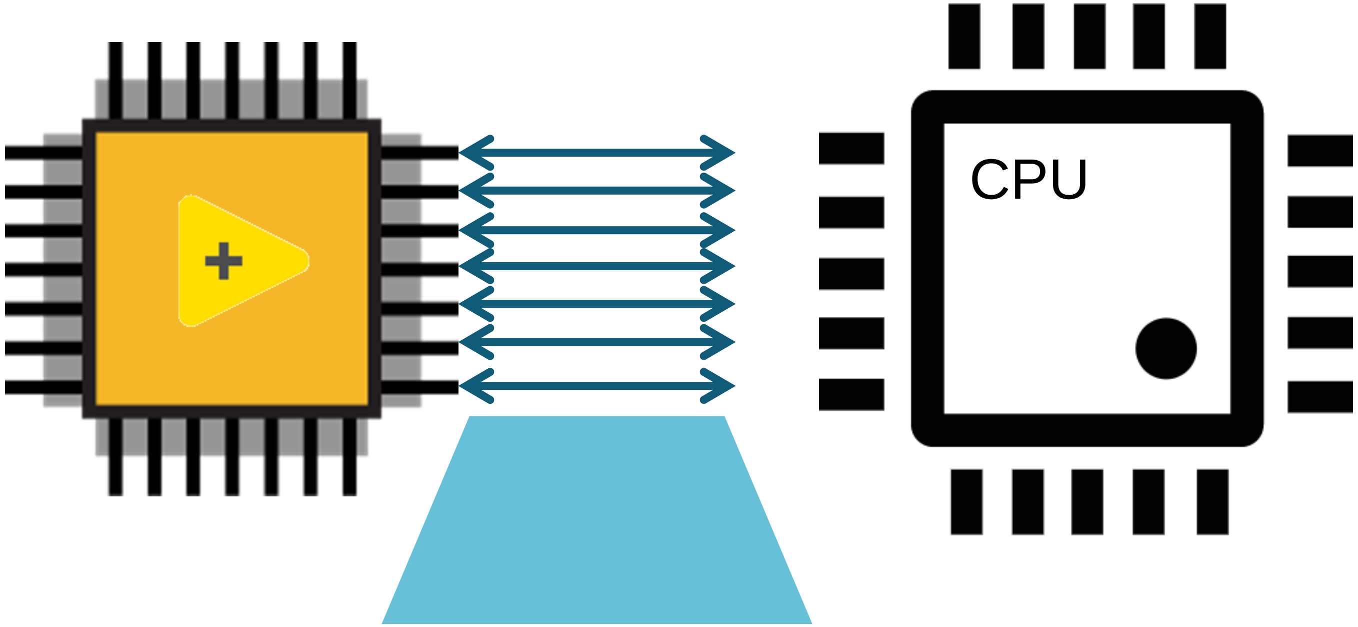
+ may be a typedef

FPGA communication



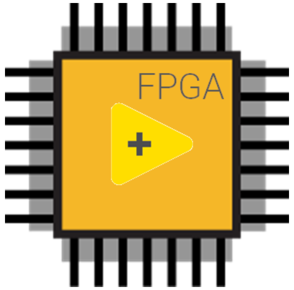
FPGA ←→ CPU

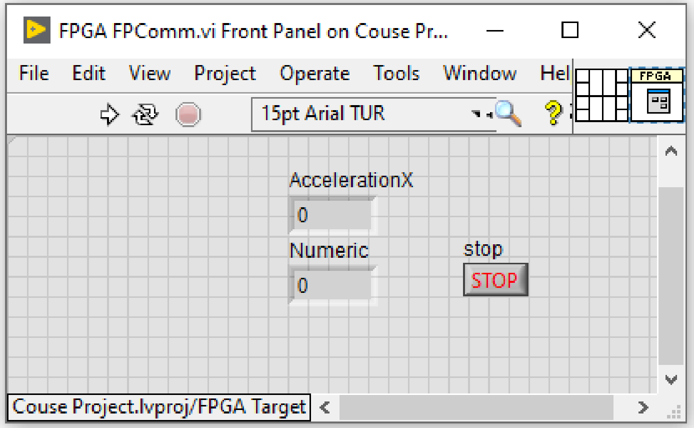
+ IP components delivered

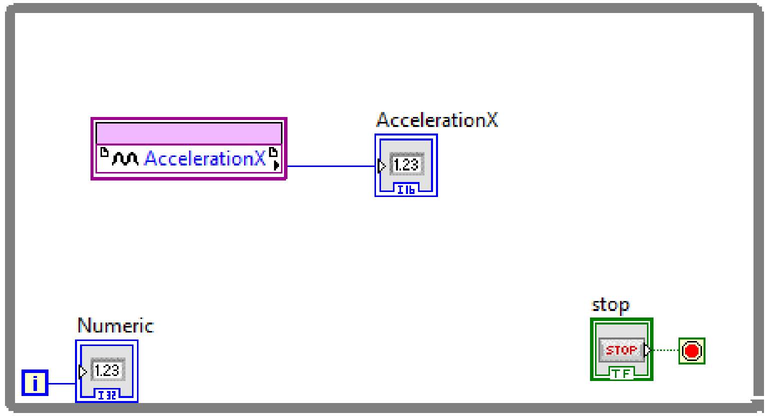


- ○ Front Panel Communication
- ○ DMA
- ○ Interruptions

FPGA interface







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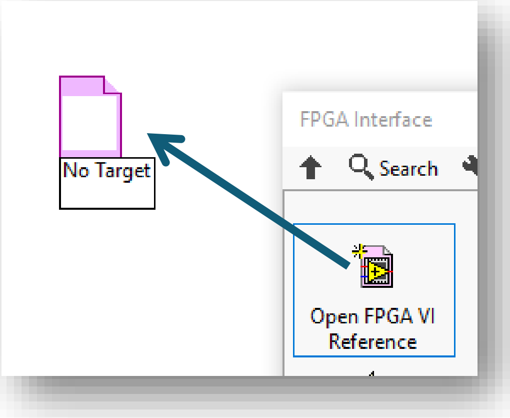

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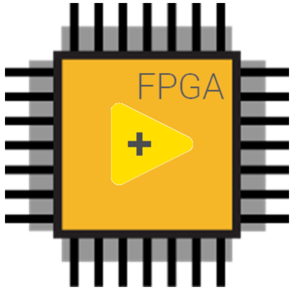
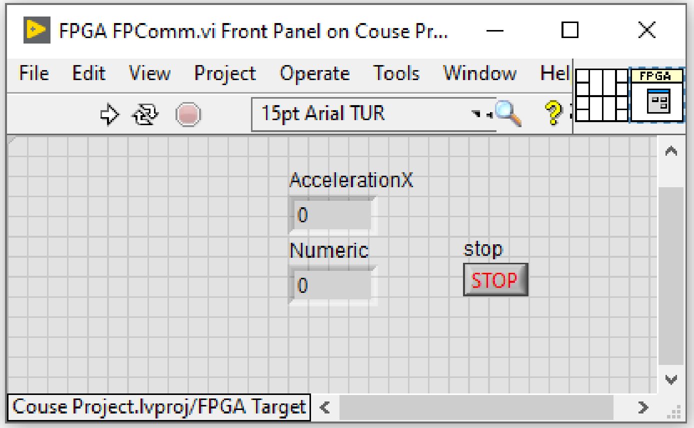
FPGA interface



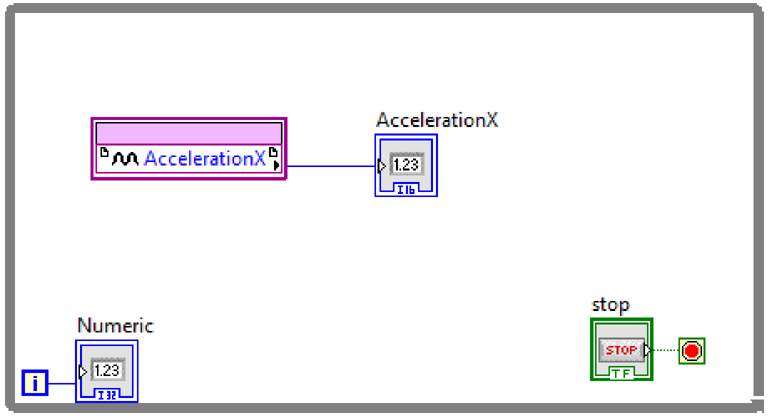

FPGA FPComm.vi Front Panel on Couse Pr...
File Edit View Project Operate Tools Window Hel
15pt Arial TUR
FPGA

AccelerationX: 0

Numeric: 0

stop: STOP

Couse Project.lvproj/FPGA Target



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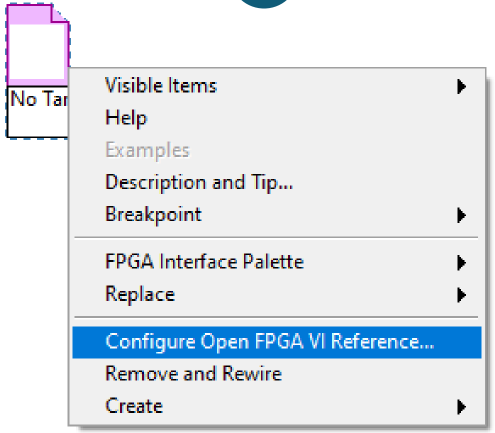
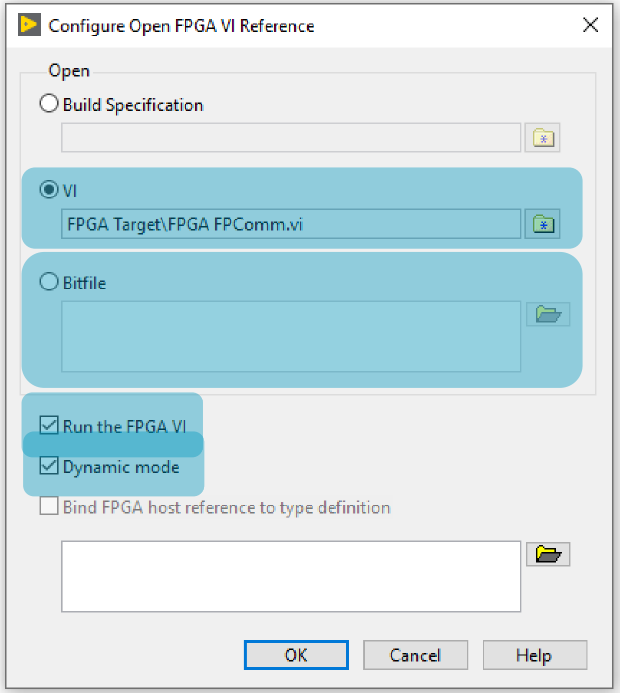




Configure Open FPGA VI Reference

Open

○ Build Specification

● VI

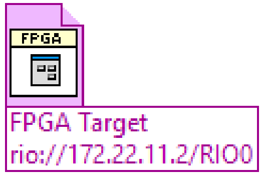
FPGA Target\FPGA FPComm.vi

○ Bitfile

☑ Run the FPGA VI

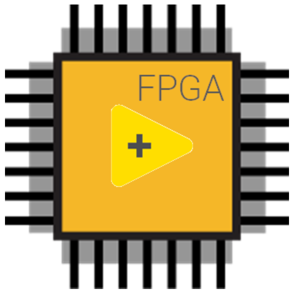
☑ Dynamic mode

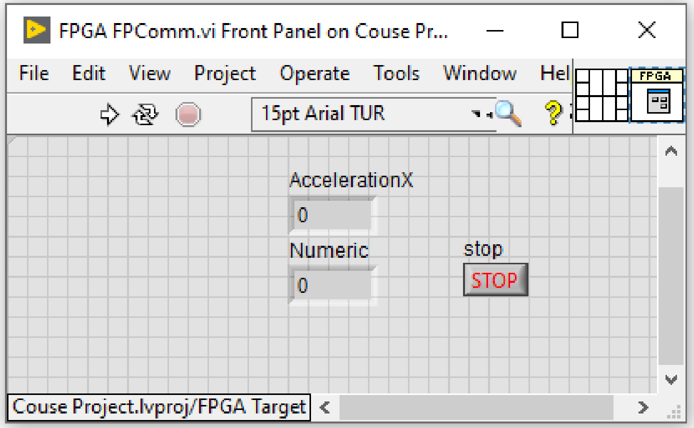
□ Bind FPGA host reference to type definition



FPGA Target
rio://172.22.11.2/RIO0

FPGA interface



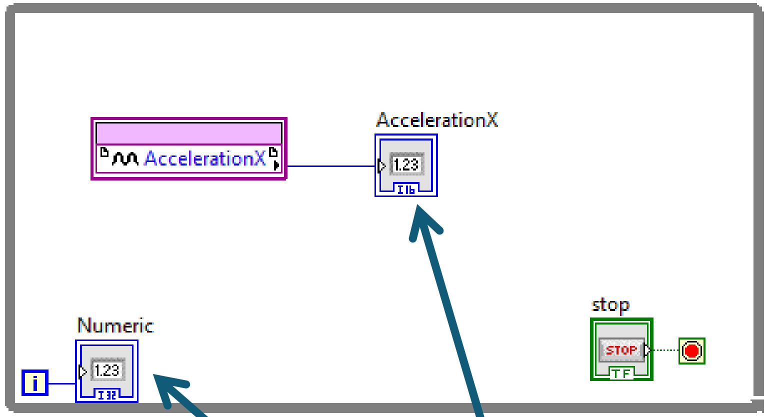

FPGA FPComm.vi Front Panel on Couse Pr...

File Edit View Project Operate Tools Window Hel

15pt Arial TUR

AccelerationX
0
Numeric
0
stop
STOP

Couse Project.lvproj/FPGA Target



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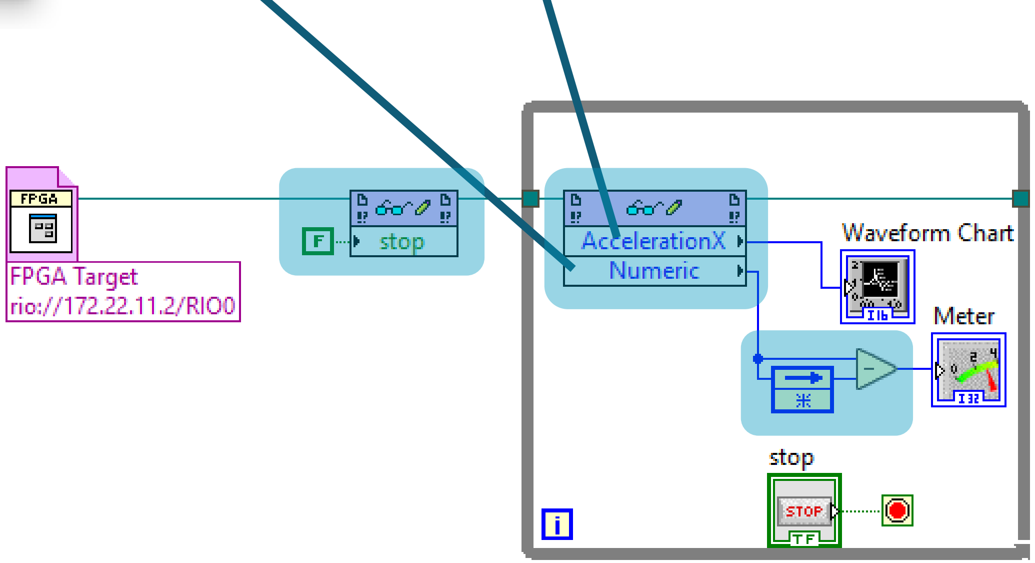

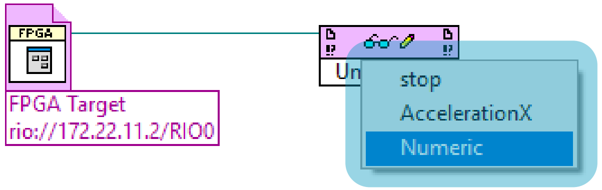

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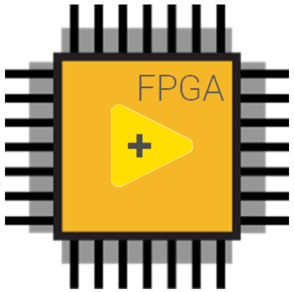
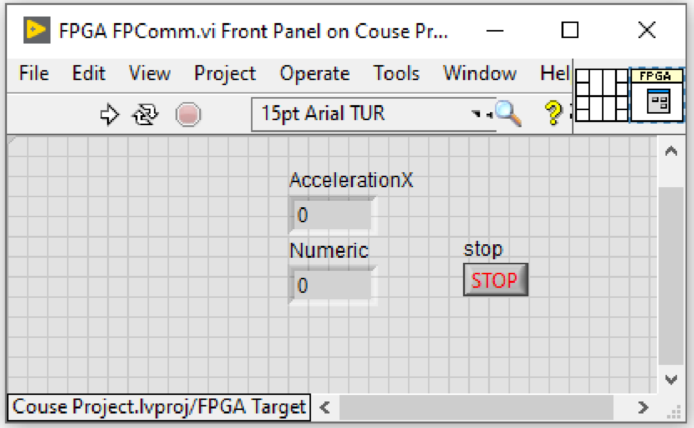
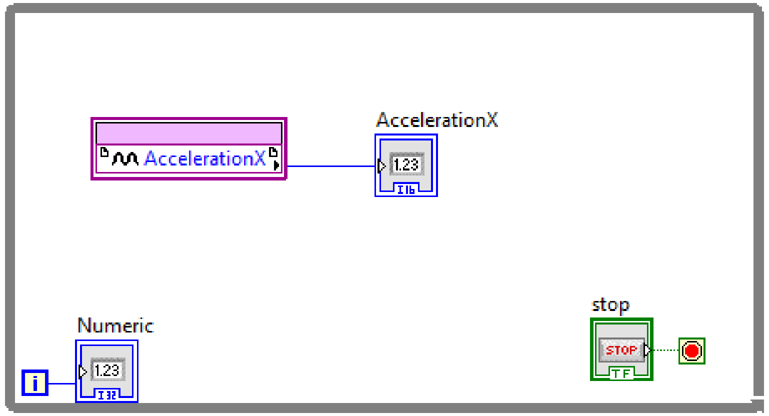
FPGA interface







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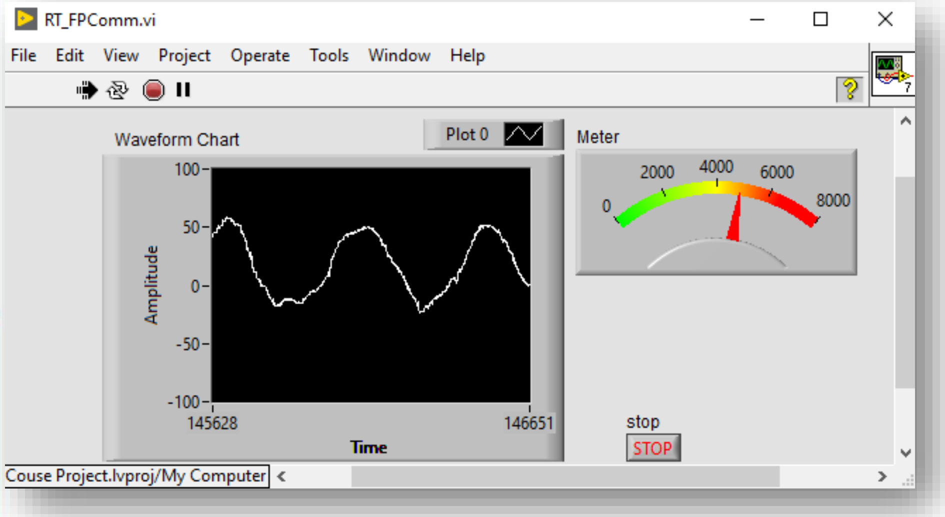
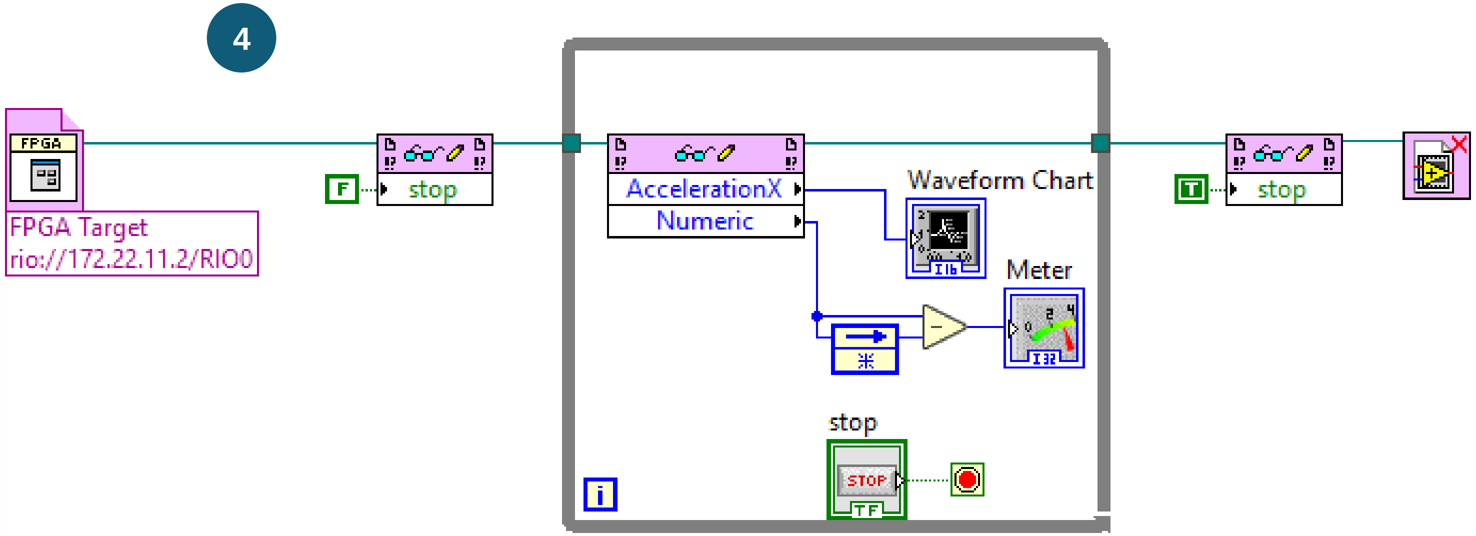
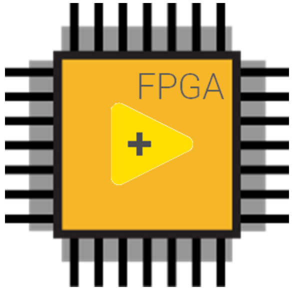
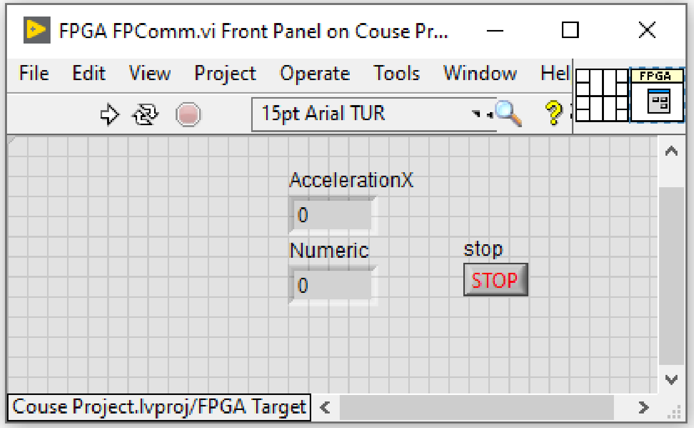




DMA – FPGA-HOST



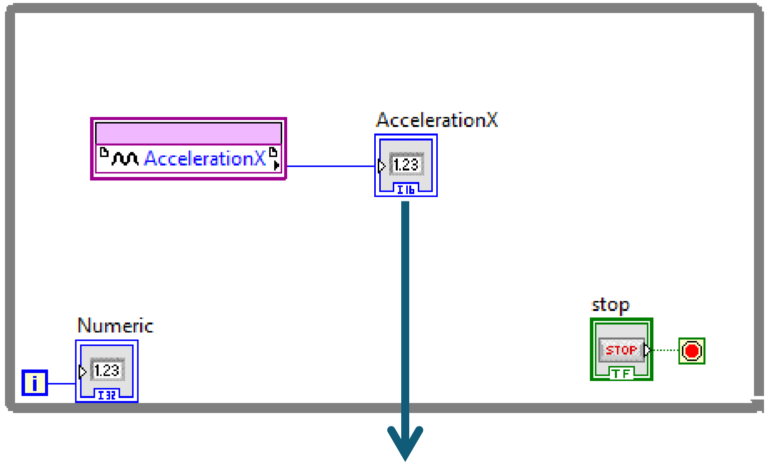

FPGA FPComm.vi Front Panel on Couse Pr...

AccelerationX: 0

Numeric: 0

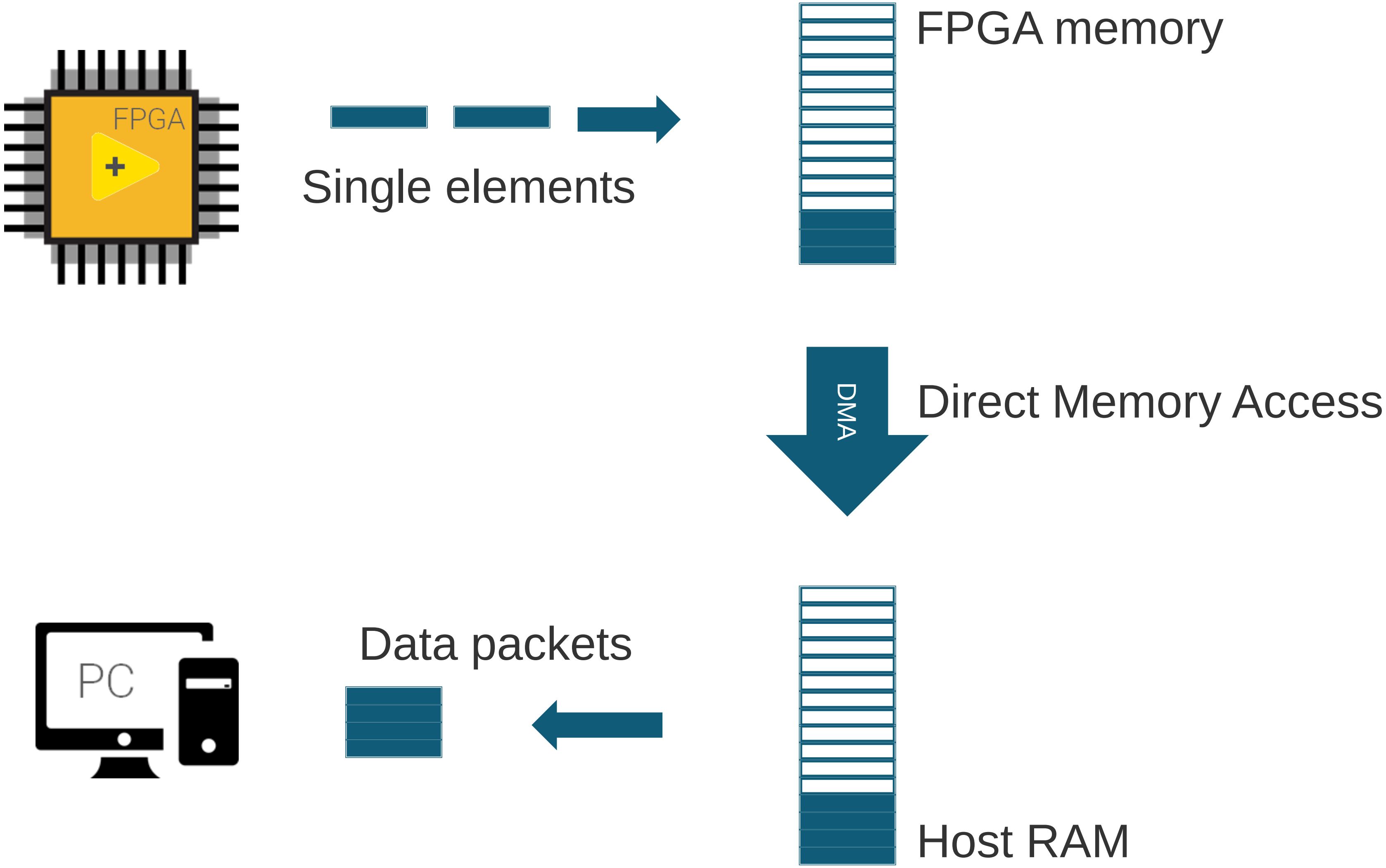
stop: STOP

Couse Project.lvproj/FPGA Target

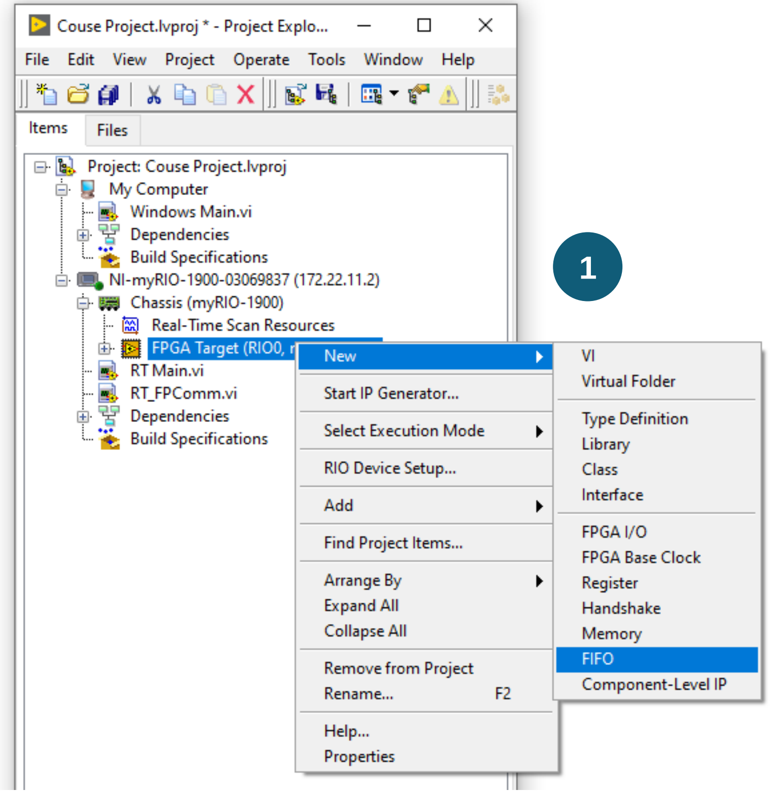


How to read every value?

DMA – FPGA-HOST



DMA – FPGA-HOST



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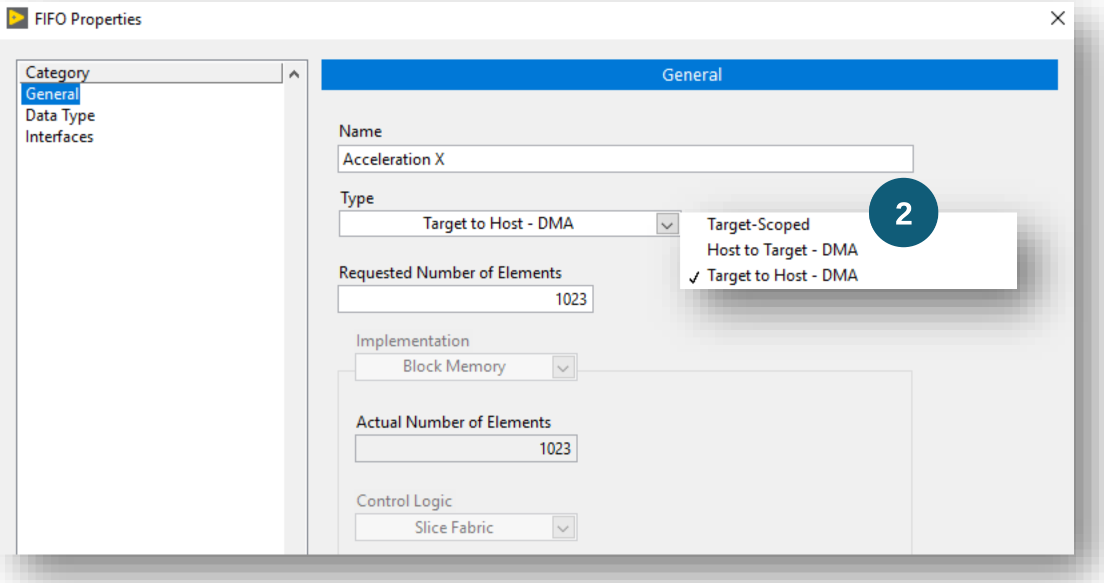


Name: Acceleration X

Type: Target to Host - DMA

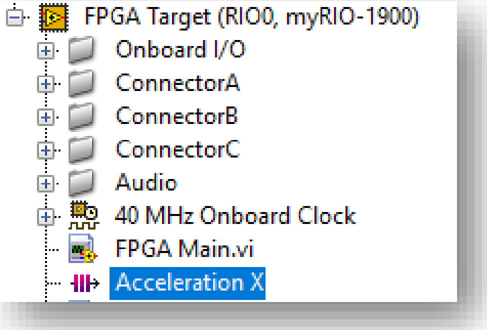
Requested Number of Elements: 1023

Implementation: Block Memory

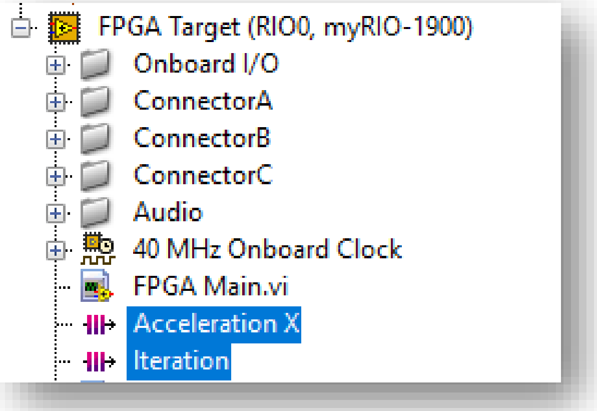
Actual Number of Elements: 1023

Control Logic: Slice Fabric

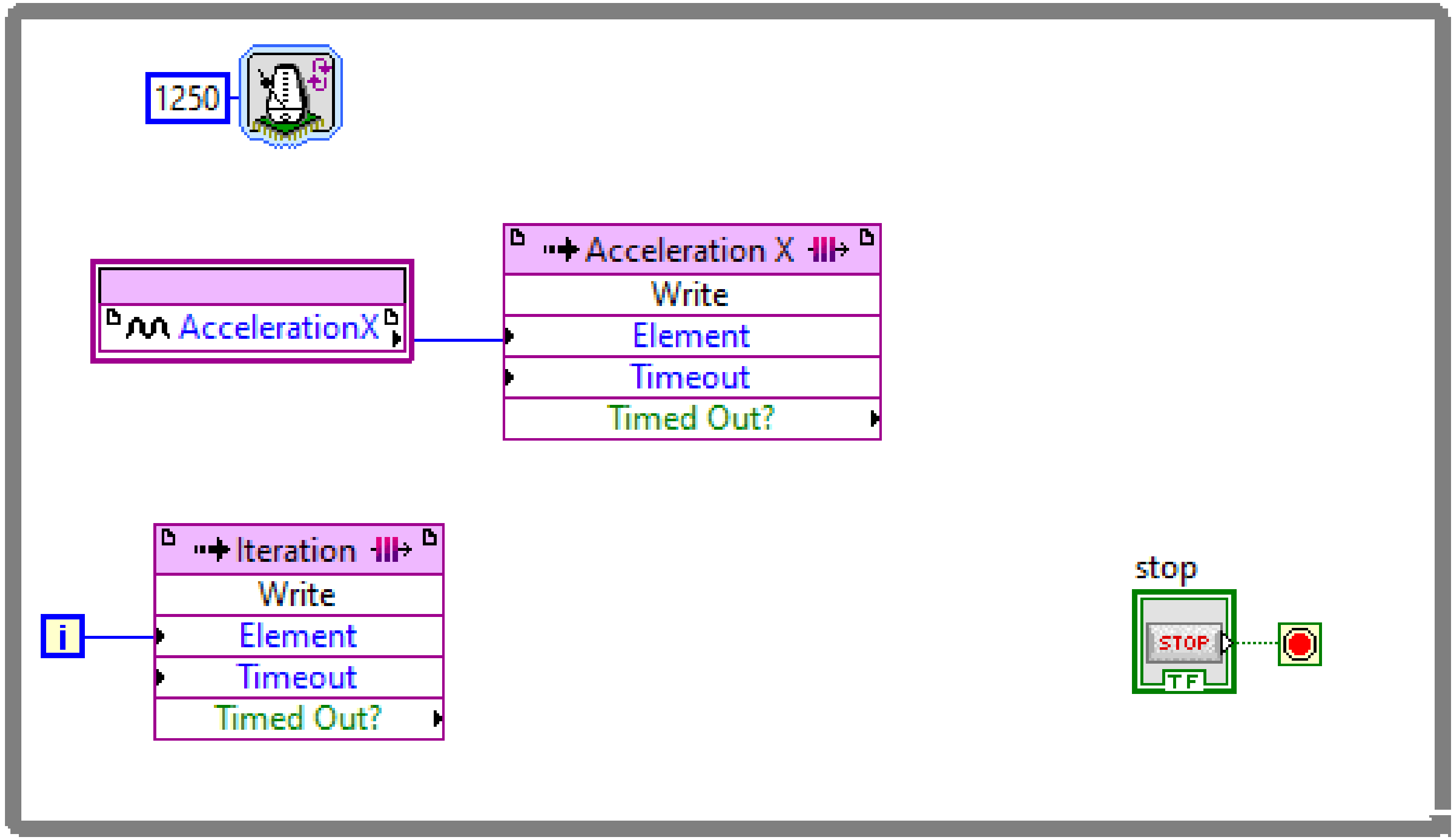
3



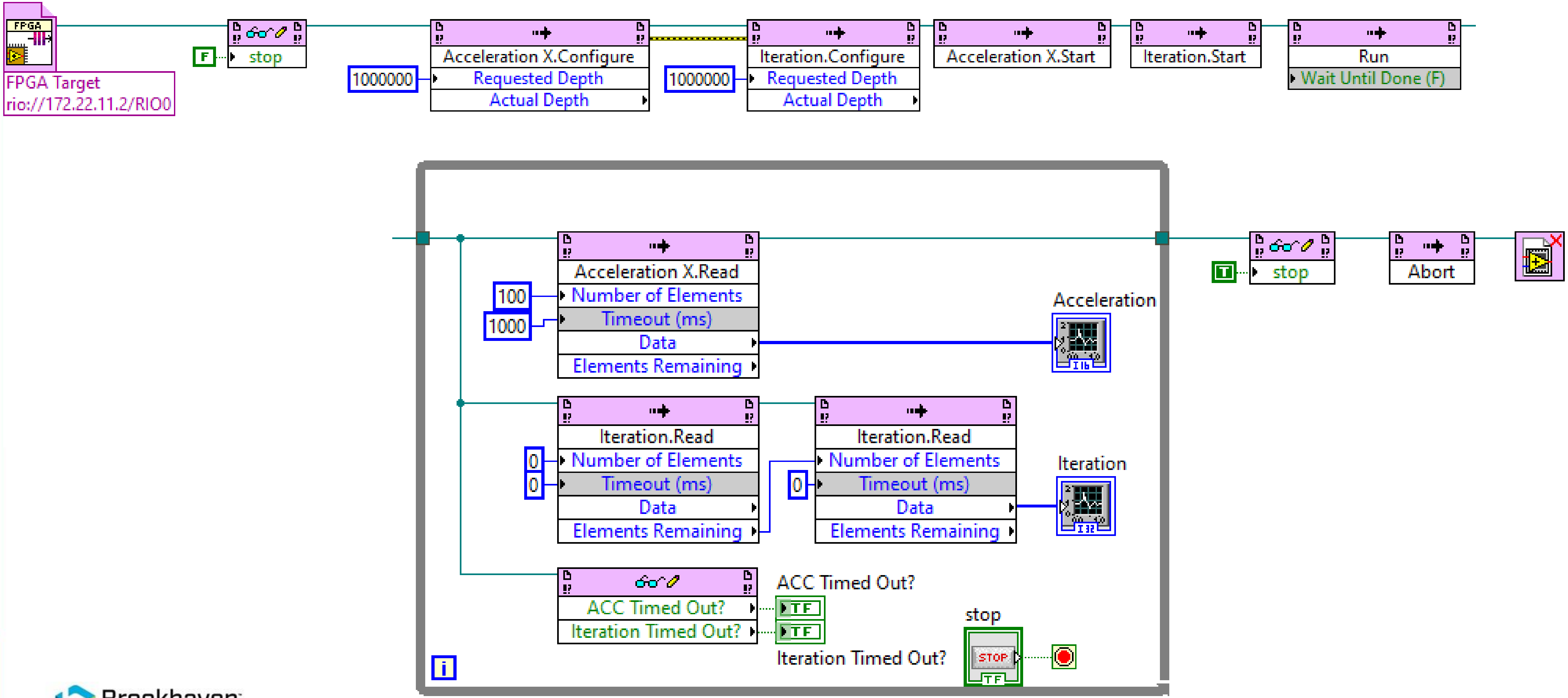
DMA – FPGA-HOST



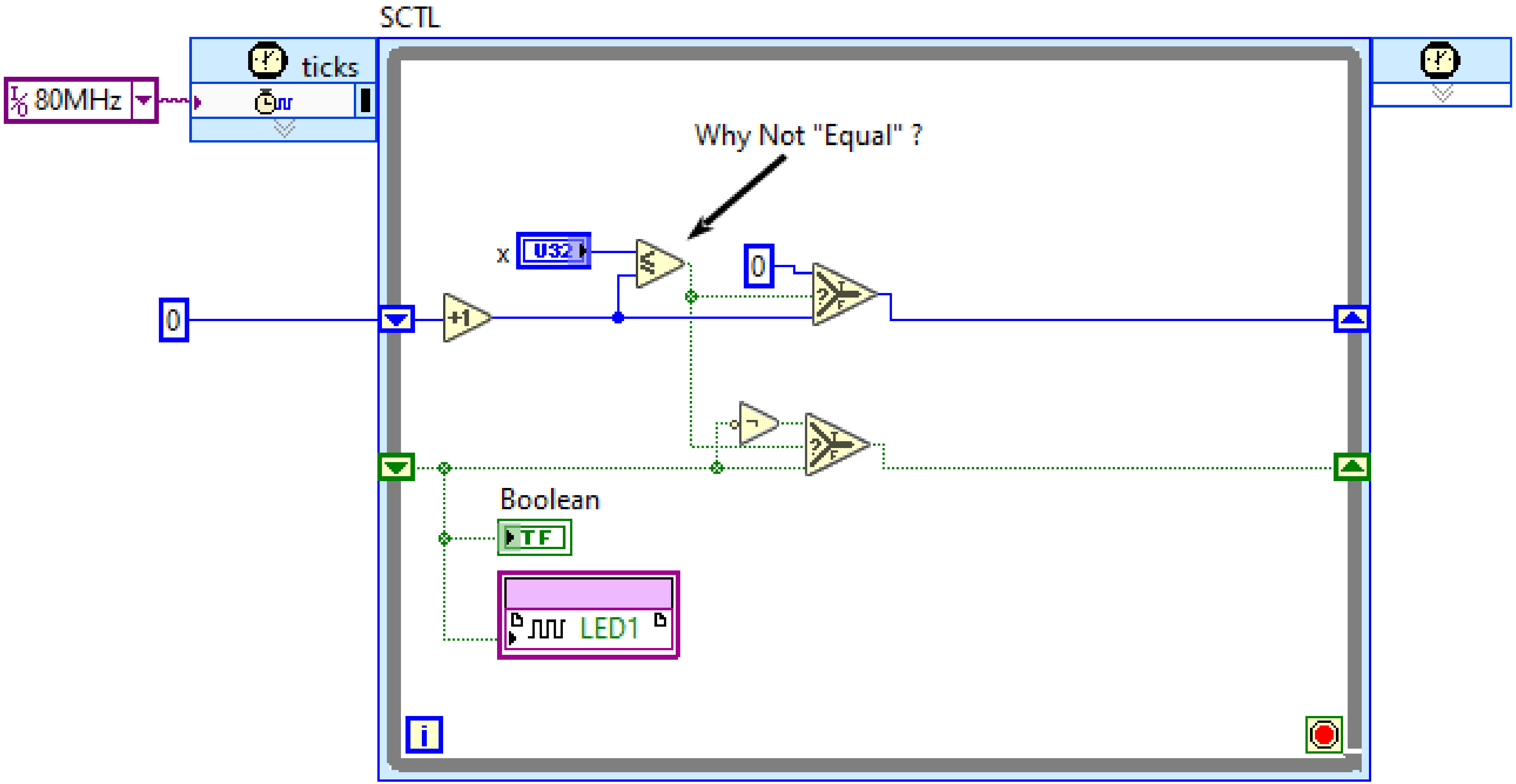
FPGA Target (RIO0, myRIO-1900)
- Onboard I/O
- ConnectorA
- ConnectorB
- ConnectorC
- Audio
- 40 MHz Onboard Clock
- FPGA Main.vi
- Acceleration X
- Iteration



DMA – FPGA-HOST



Counter FPGA implementation Example



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U.S. DEPARTMENT OF
ENERGY

Data Acquisition in ASIC testing

Piotr Maj on behalf of ASIC group

Date 10/19/2023

@BrookhavenLab