Discrete/COTS waveform readout FEB for backward ECAL

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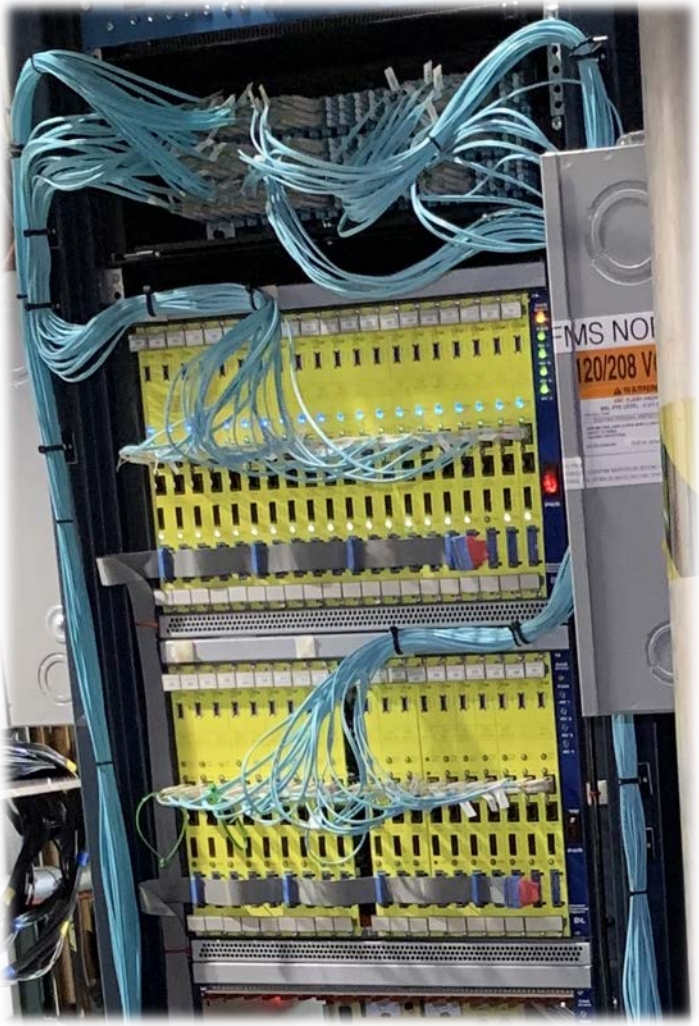


STAR FCS waveform readout (remote preamp/shaper), 32 ch/board

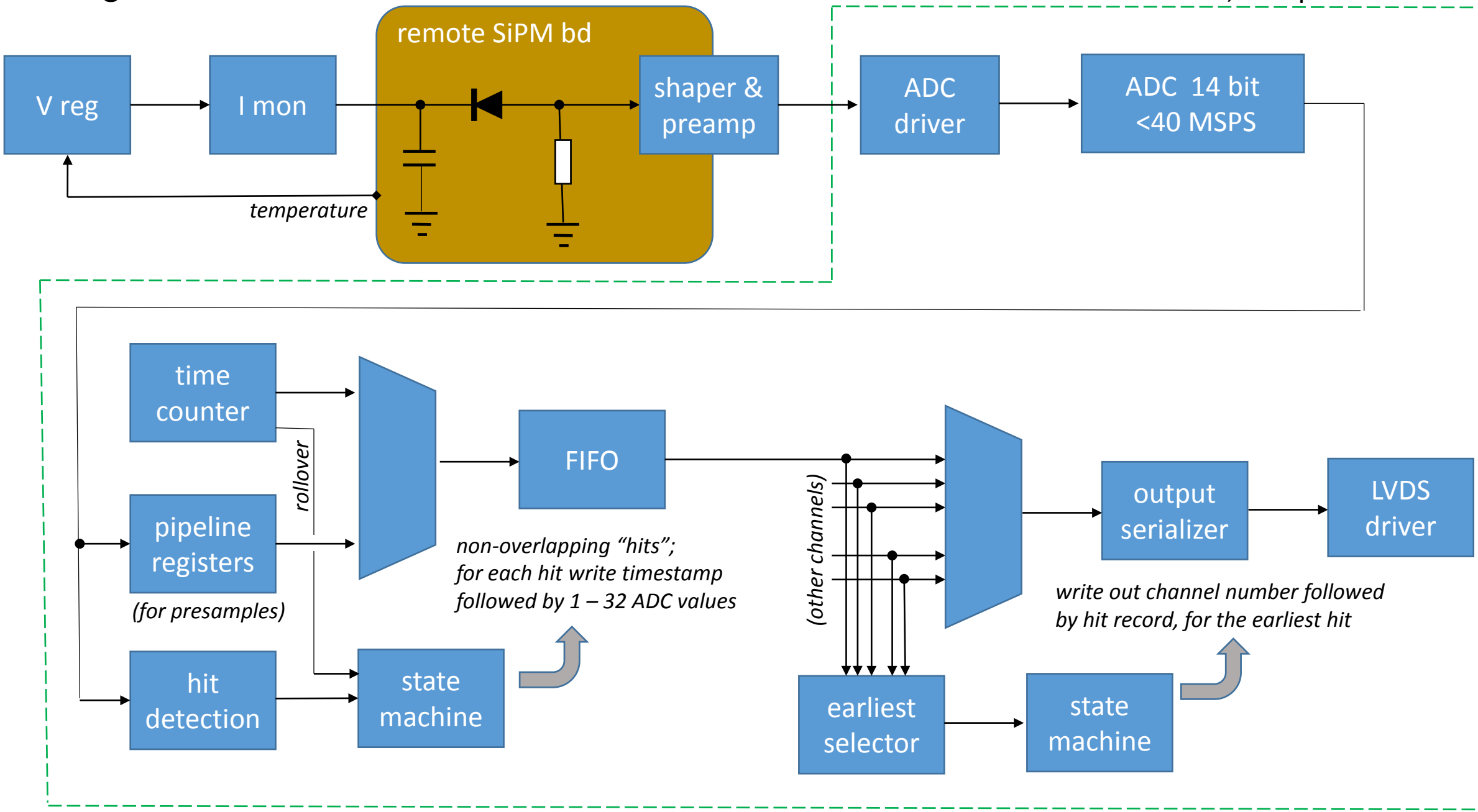
ePIC Calorimetry meeting, 9/13/2023

requirements and characteristics – for discussion / correction

see later slide

- 24 channel assembly
- dimensions: < 18 × 12 × 1.5 cm^3
- power: <120 mW/ch (2856 ch: 343 W)
- ADC: 14 bit, 39.4 MSPS (2/5 clock) or 32.8 MSPS (1/3 clock)
- peaking time: 4 – 5 samples
- number of samples taken: 8 (likely; adjustable)
- SiPM capacitance: 10 nF
- SiPM gain: 1.8 – 3.6 × 10^5 (TBD)
- light yield: 5.5 pixels/MeV (expected, TBC)
- signal range: 5 MeV (threshold) to 20 GeV [1.6 pC to 6.3 nC @ highest gain]
- SiPM DCR (after irrad.): TBD
- dark counts in pulse: TBD (roughly peaking × DCR)
- linearity (electronics only): 0.1%
- rate capability: **TBD** (50 kHz/ch ?)
- timestamp size: 24 bit (340 ms rollover)
- rollovers marked in datastream
- total hit data size: 144 bits (or less, w/ feature extraction, perhaps)
- max output (to RDO) data rate: 40 MB/s
- data cable: Cat6 or similar, <30 m
- SiPM bias control: per channel DAC, 33 – 47 V range, <10 mV stability, low noise <1 mV, *fast recovery*
- SiPM bias compensation: per channel thermistor, common slope DAC
- SiPM bias current monitor
- SiPM – FEB cable length: **≤ 60 cm** TBD, micro-coax
- input supply monitor
- on-board LV DC/DC, 10 – 13 VDC input

Block diagram

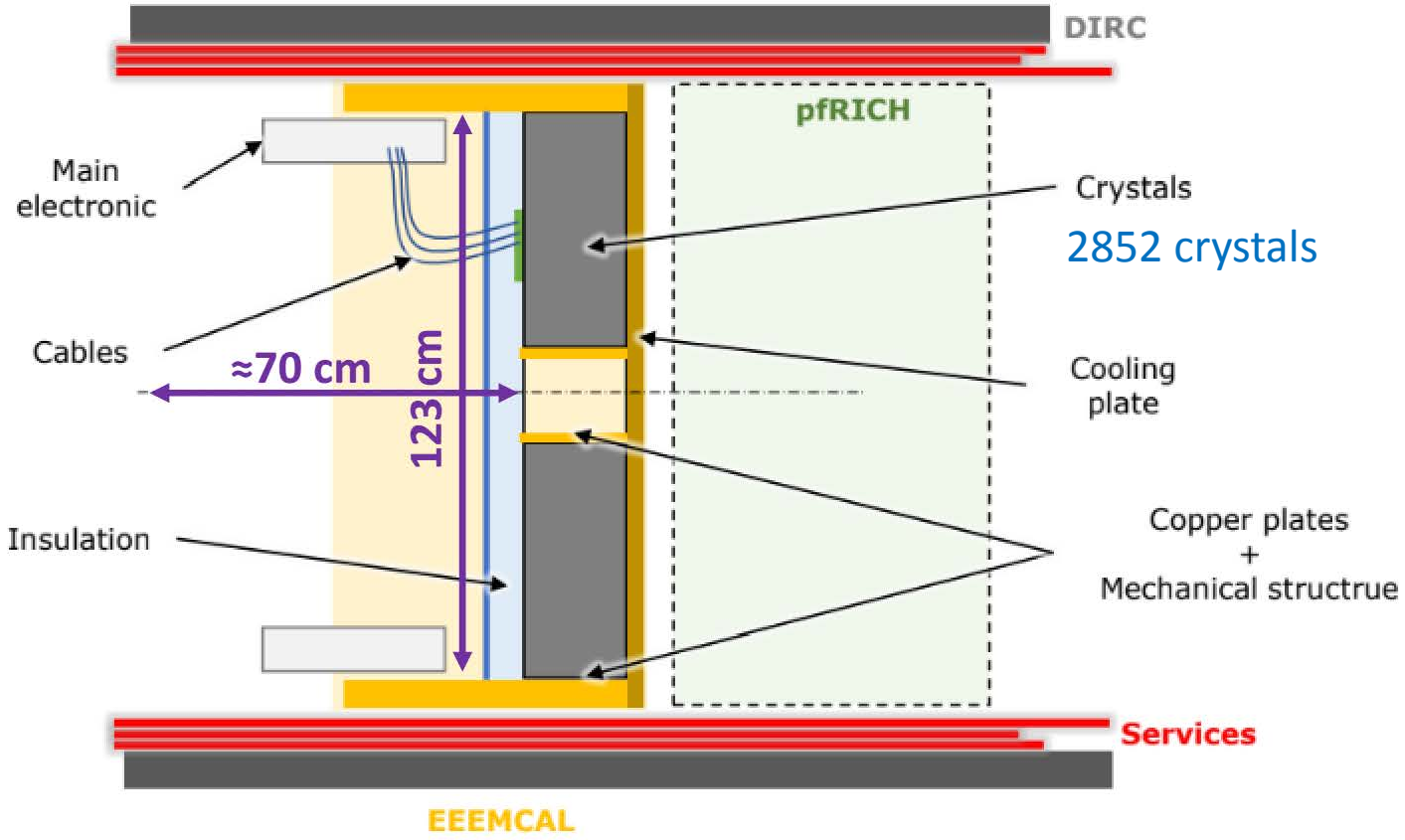


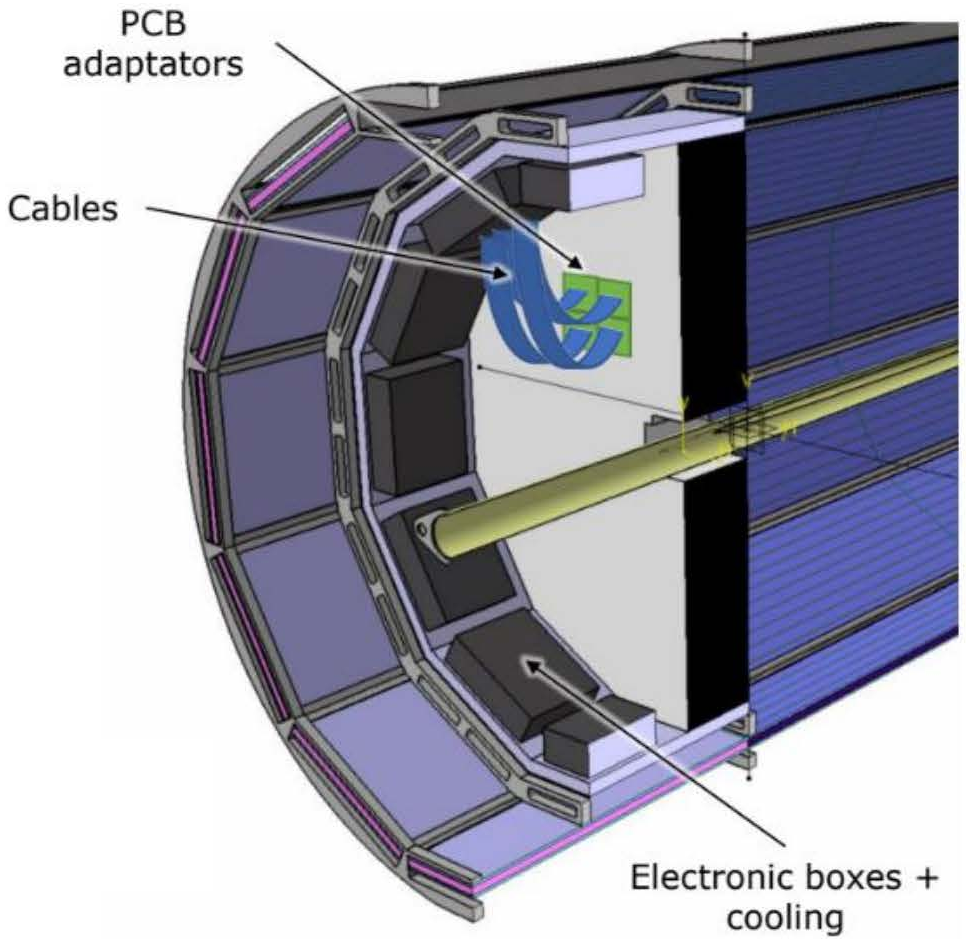
(borrowed slide, slightly trimmed)

EEEMCAL front-end electronics and cooling

No lack of integration space for electronics, I'd say.

It will be good to keep most electronics to the periphery, as planned/shown, to minimize radiation damage and to ease cabling.





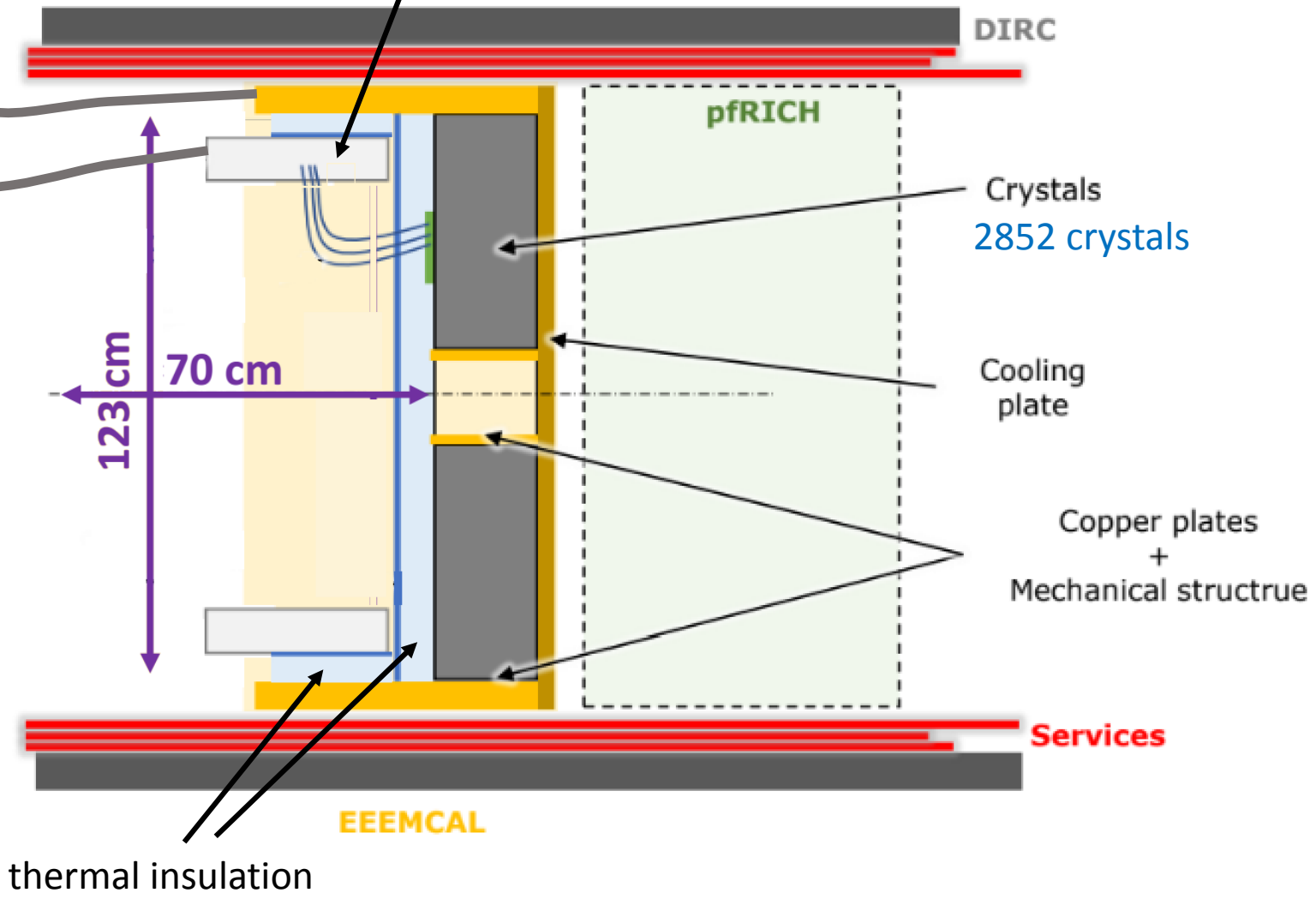
12 electronics assemblies

FEB mechanical & cooling

T control (cooling)
liquid for crystal array

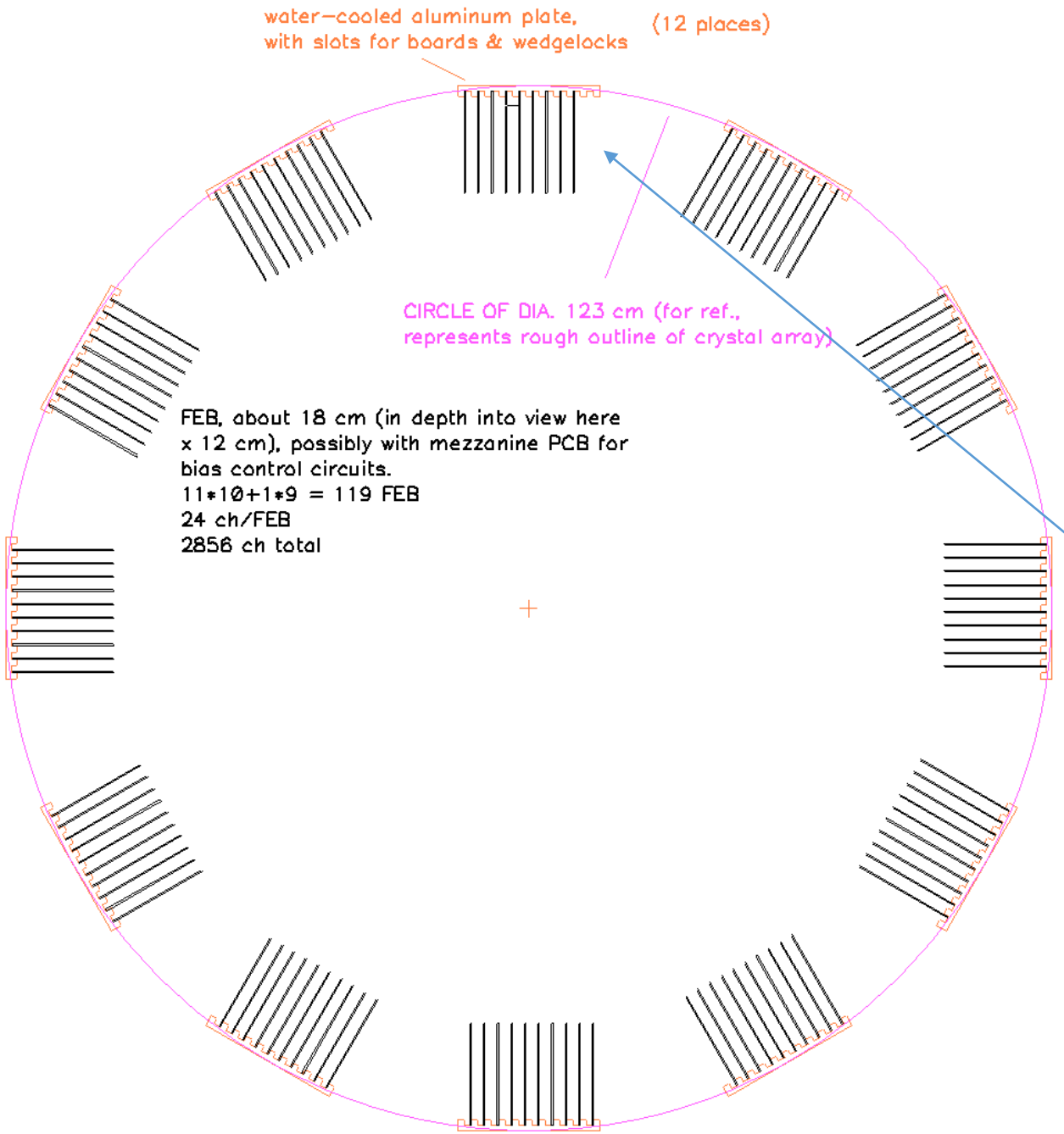
12 × FEB assy, 9 – 10 FEB each (119 FEB total, 2856 ch)
18 × 12 cm in this view (excl. coldplate)

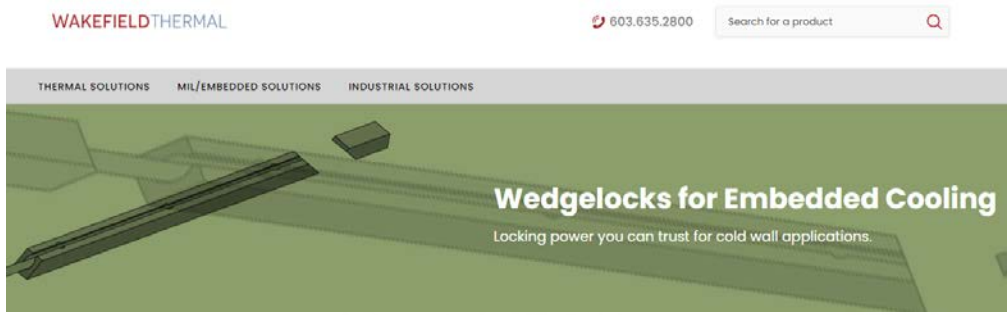
liquid cooling for FEB assy
6 loops, 2 assy in series
57 W per loop



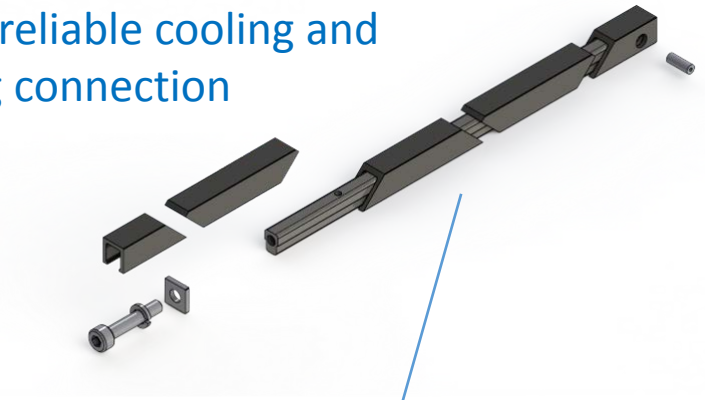
- Thermal insulation *all around* between FEB and crystal support & thermal structure
- **Separate** liquid temperature control loops for crystals & FEB's
- Preamp power on SiPM board must be / will be mimized
  - maybe 0 ?
- But, radiation damaged SiPM's will dissipate some heat:
  - e.g. 95 W @ 200 µA / SiPM…

FEB mechanical & cooling

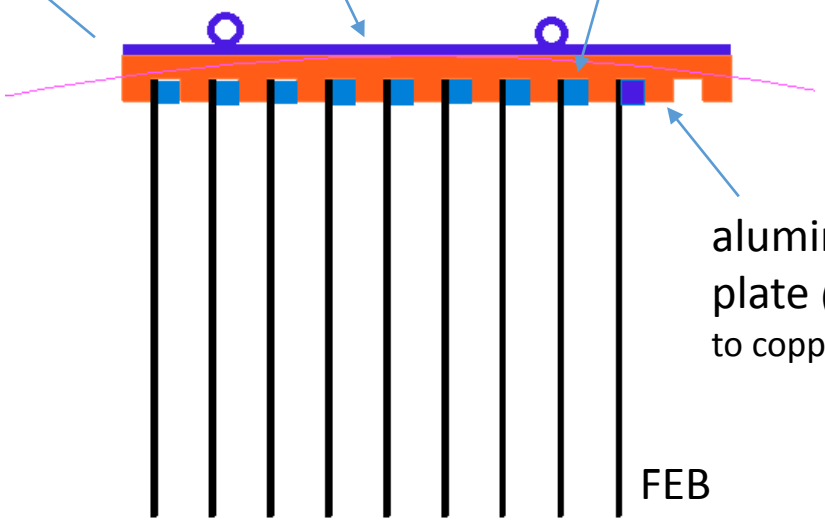




modular, reliable cooling and mounting connection

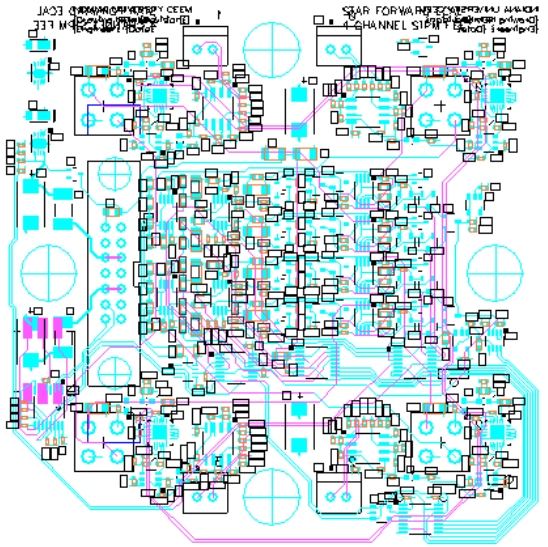


brazed copper heatsink



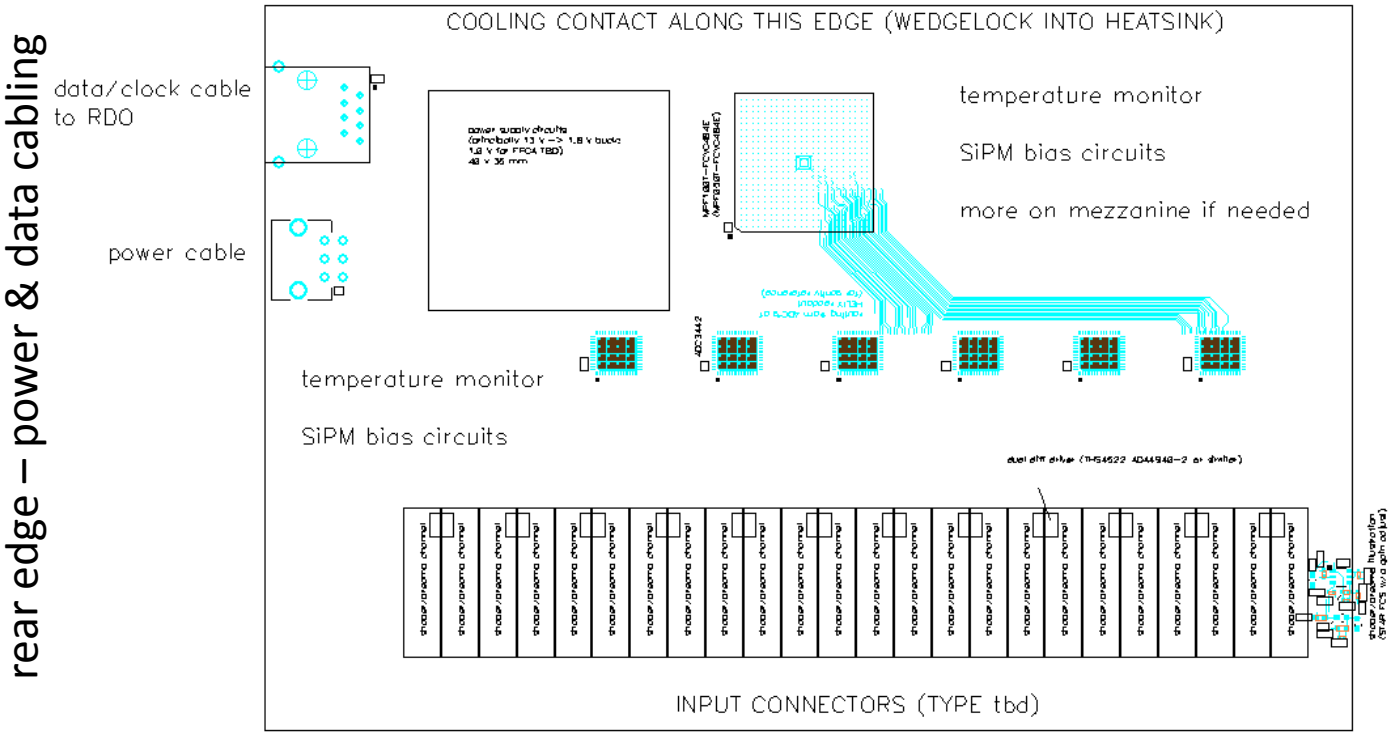
FEB layout sketch

shown with STAR FCS FEB for comparison



ePIC bwd ECAL waveform readout FEB
layout floorplanning sketch G. Visser 8/15/2023

shown with STAR fwd ECAL FEB



rear edge – power & data cabling

1 FPGA (Polarfire)
6 quad ADC's

inside radius edge – cables to SiPM boards

Closing remarks

- There seems to be plenty of room for FEB in the already planned scheme behind the crystal array and SiPM boards
- Adapting the discrete/COTS waveform readout as now being developed under eRD109 for forward ECAL to this case is straightforward enough
    - If agreed, we should start to think about how to make this happen
- Main change is the remote (60 cm) SiPM board. The baseline strategy should be to try to avoid needing a preamp on the SiPM board.
- A 24 channel or perhaps 32 channel FEB looks most sensible
- Risk of impacting crystal temperature control is (I think) minimal
    - *Can't forget about heat from radiation-damaged SiPM's though…*
- As in the forward ECAL case, replacement of the COTS ADC and FPGA by an ASIC offering an equivalent architecture & performance at lower cost and power would be great. Perhaps it's a possibility (e.g. several SBIR efforts underway).