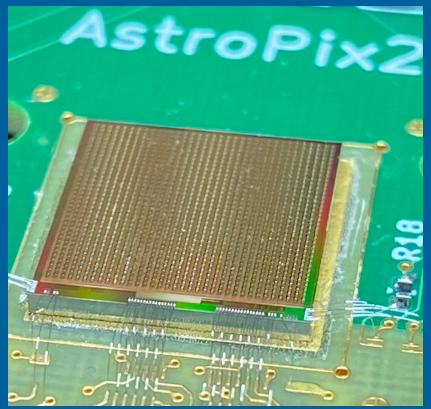
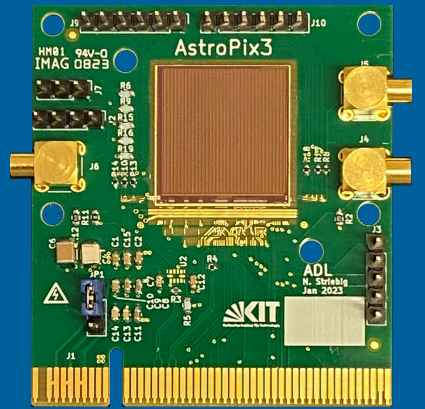
ePIC TIC Meeting - Barrel Imaging Calorimeter (BIC)

BIC - AstroPix





Manoj Jadhav
HEP, Argonne National Laboratory

October 2, 2023

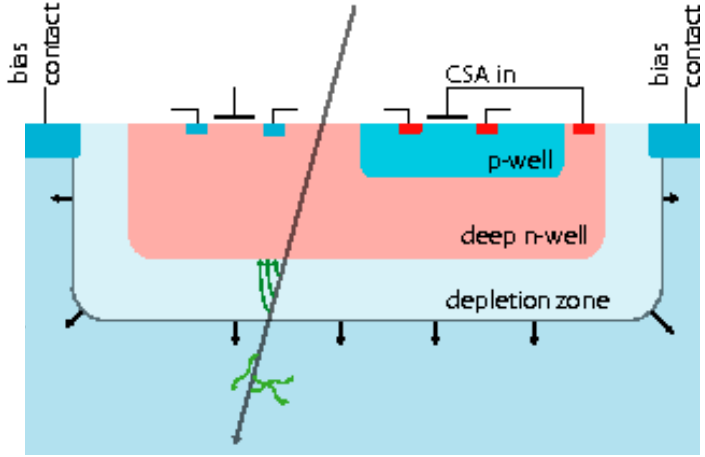
AstroPix


AMEGO-X
1U ETU
AstroPix_v3
Engineering Test Unit (prototype)
Roman Technology Fellowship
Future space-based applications
BIC@ePIC
AstroPix_v1, v2
ATLASPix
CARIBOU DAQ
Adapter board
FPGA
Lab development and optimization
2019 APRA
State-of-the-Art silicon detectors from collider-based particle physics

AstroPix

HV-CMOS Monolithic Active Pixel Sensor (MAPS):

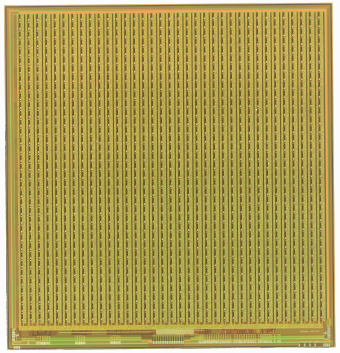
- Combination of silicon pixel & Front-End ASIC
- On-pixel charge amplification and digitization
- Technology uses more typical CMOS wafer processing for cost effective mass production
- Fabrication on single wafer enables shorter design cycle
- No need to bump-bond to each pixel - improves yield



AstroPix (based on **ATLASPix3** **arXiv:2109.13409**)

- 180nm HV-CMOS MAPS sensor
  designed at KIT (also designed ATLASPix, MuPix, etc.)
- Developed for AMEGO-X GSFC/NASA mission
  (Upgrade to the Fermi's LAT)
- Power consumption <1.5 mW/cm^2
- Energy resolution target of 2% @ 662keV

AstroPix v3 (Under test)



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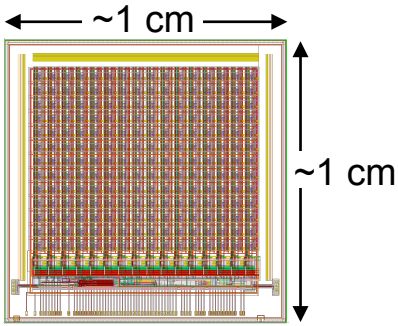


AstroPix v4
(MPW - delivered)

AstroPix Developments

AstroPix v1 - January 2021

- 0.45 × 0.45 cm² chip, 175 µm pixel pitch
- 18 × 18 pixel matrix
- Power dissipation ~14.7 mW/cm²

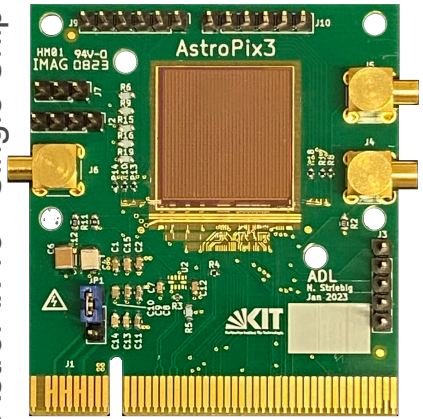
AstroPix v2 - December 2021

- 1 × 1 cm² chip with 250 µm pixel pitch
- 35 × 35 pixel matrix
- Hit identification with Row/Column readout
- Power dissipation ~3.4 mW/cm²

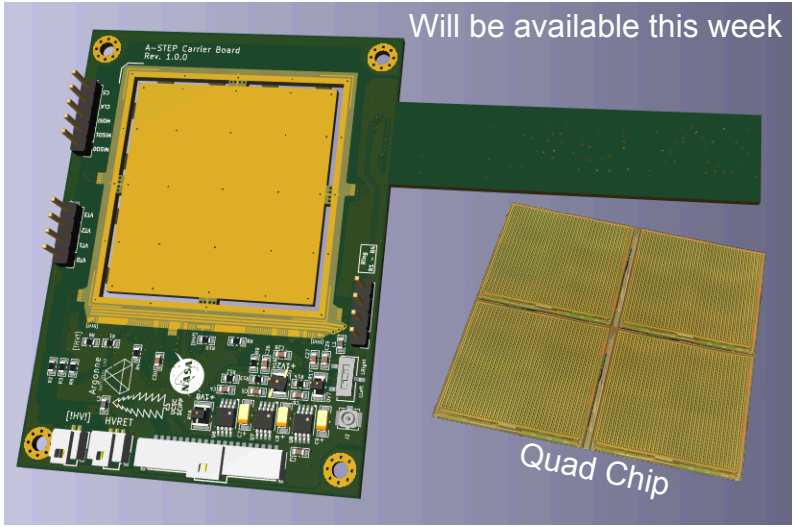
AstroPix v3 - February 2023

- 2 × 2 cm² chip with 500 µm pixel pitch
- Power dissipation <1 mW/cm² (targeted)
- Timestamp clock 2.5MHz, ToT 200 MHz
- 10 byte data frame per hit **(Amanda's talk)**

AstroPix v2



AstroPix v3 - Single Chip



AstroPix v3 Quad-chip Carrier Board

AstroPix v4/v5

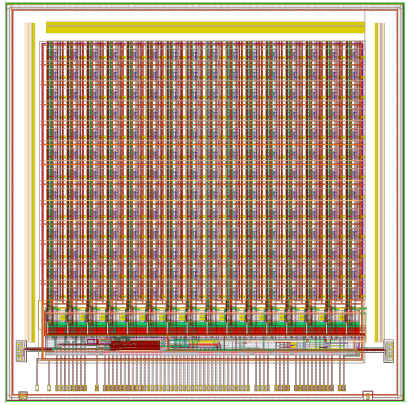
AstroPix v4 : Final design version will small size

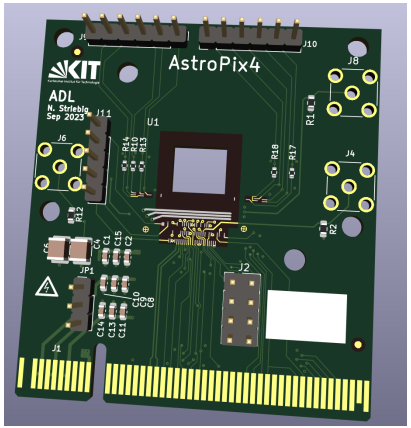
- Chip size 1 × 1 cm²; Thickness 700 µm, V_{BD} ~ 400V
- Pixel pitch 500 µm with pixel size 300 µm, 16 × 16 pixel matrix
- Individual pixel readout with individual hit buffer
  - No identification issue due to ghost hits
- 3 Timestamps - 2.5MHz (TS), 20 MHz (Fine TS), and 16 bit Flash TDC
  - Fast ToT and Timestamp with 3.125 ns time resolution
- TuneDACs - Pixel-by-pixel threshold tuning and pixel masking
- Daisy Chain readout - pass hits to next chip through QSPI
- Self-triggered (reads out active hits)

AstroPix v5 : Full size final design

- No planned design changes
- Fix any bug from v4
- Full size chip - 2 × 2 cm², pixel pitch 500 µm,
- 35 × 35 pixel matrix → 1225 hit buffers

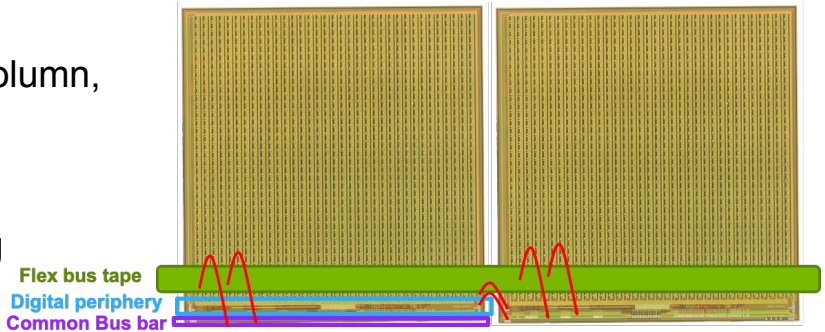
AstroPix v4

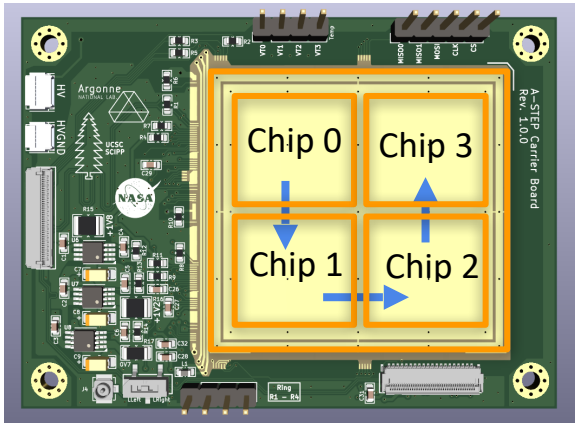




AstroPix Readout

- 8 bytes data per hit - header (chipID, payload), row/column, timestamp, ToT
- SPI I/O daisy chained - chip-to-chip signal transfer
  - signals are digitized & routed out to the neighboring chip using 5 SPI lines via wire bond
- Power/Logic I/O distribution on the module (through a bus tape)
  - 4 power lines (LV, HV), ~20 Logic I/O (SPI, clk, timestamp, interrupt, digital Injection, etc.)
  - HV, VDDA/VDDD(1.8V), VSSA(1.2V), Vminuspix(0.7V)
  - power distribution can be controlled using voltage regulators
  - mostly part of end of the stave services
- Data will be received by FPGA at the end of stave
  - FPGA aggregates data before sending off-detector
- Low heat load at chip, only cooling of end of the stave card
- Operational temperature for AstroPix is at room temperature and considered to be operated at 22 °C





AstroPix v3 quad-chip carrier board
- Demonstrate required services
- Daisy chaining

AstroPix at ePIC

Low Rates

- The expected hit rate for **all imaging layers together** is well below < 3×10^7 Hz
- This translates to a maximum hit rate per tracker stave (1 x 104 chips) < 36 kHz

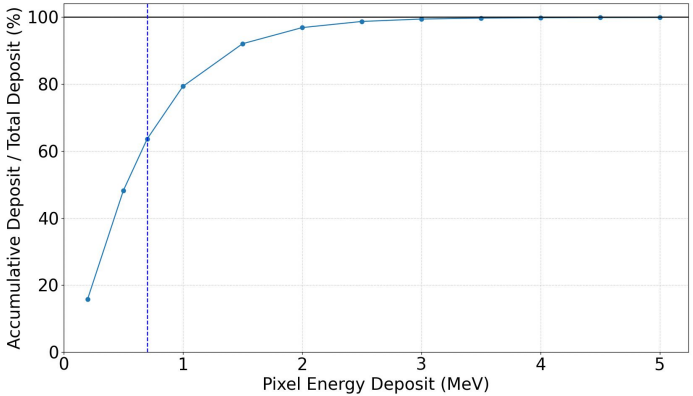
Zero-suppression below threshold 20 keV (4 × noise floor)
well suited for EIC electromagnetic showers

Timing requirement: 3.125 ns (v4/v5) - **driven by 10 ns bunch crossing**

Low Ionization radiation dose and neutron flux

- The maximum **ionizing radiation dose < 1 kRad/year** for the barrel region
- Max neutron flux - order of **10^9 $n_{equivalent}/cm^2$ per year**

Dynamic range (see plot for 2 GeV e^-)
~ 3 MeV



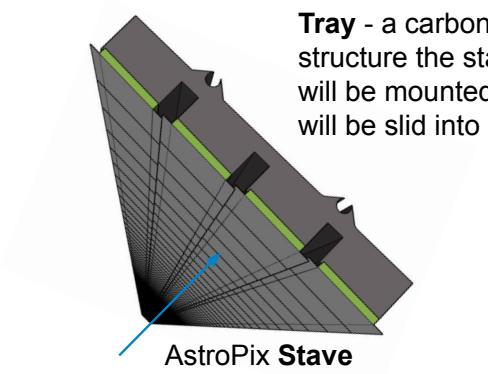
Accumulative energy deposit to the total energy deposit for 2 GeV electrons.

- About 63% of the energy deposit was made through hits with deposit < 700 keV
- hits with deposit < 3 MeV contribute to 99% of the total energy deposit

AstroPix Assembly

AstroPix v5 (Production version)

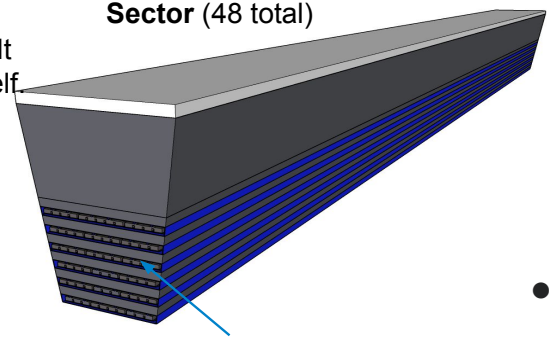
- Full size chip - 2 × 2 cm², pixel pitch 500 µm,
- 35 × 35 pixel matrix → 1225 hit buffers
- Fix any bug from v4



Tray - a carbon fiber structure the staves will be mounted on. It will be slid into a shelf.

AstroPix **Stave**
Consists of 1 x 108 chips with the support structure, "turbofanned"
AstroPix **Module**
Subset of chips

Sector (48 total)



Shelf - a carbon fiber structure that is glued to the Pb/ScFi layers, that we will slide trays with AstroPix staves on.

*The designs presented on these slides are not final but for illustration only

Module Strategy

- QC testing with wafer probing + Module and stave level QC testing and tuning
- "Baseline" model of Modules on Stave
  - Module - 8 single chips
  - Stave - 13 Modules - 104 chips
  - 12 or 14 Staves per AstroPix layer per Calorimeter Sector
  - Total 249600 chips
- All staves are identical and gets combined in a separate production step
- Data transmitted to end of the Stave card using flex base tape
- Institutions - ANL, GSFC/NASA, KIT ,UCSC, Korea, Oklahoma State

AstroPix Timeline and Production

v3 full size chip (ongoing testing)

- Test bench characterization (ongoing)
- Testbeam performance studies
- Active and passive irradiation **~10^{15} $n_{equivalent}/cm^2$**
- **Quad-chip readout (ready to test)** for NASA's hosted payload mission (A-Step) - **January 2025**
- Integration with Pb/SciFi - FY2024 **(Henry's talk)**

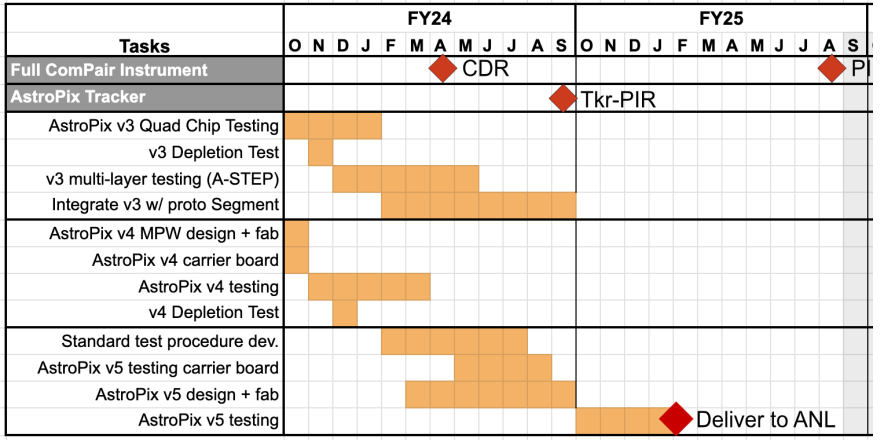
v4 new features for better performance (MWP)

- **Final design version**, smaller chip (1cm × 1cm)
- Fabricated wafers **delivered last week**
- Chip carrier board design for bench test is ready for the PCB fabrication

v5 full size final chip

- Fix any bugs from v4
- v5 chips available **November 2024**

GSFC/NASA ComPair-2 AstroPix timeline



BIC@ePIC Timeline

- **Prototype R&D** (v3) Ongoing - till Nov 24
- Pre-Production (v5) chips starts **Nov 2024**

(More info in Maria's talk)

Production

- Fabrication by TSI - with a large production order, AMS is a backup

Thank you