AstroPix Testing Status Update

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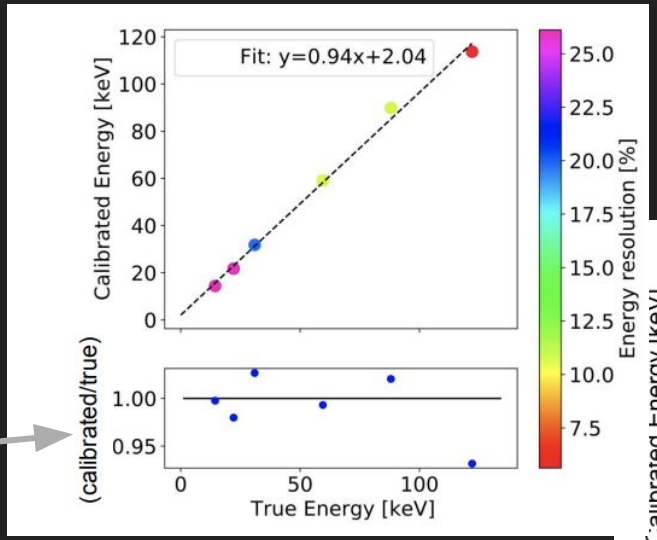
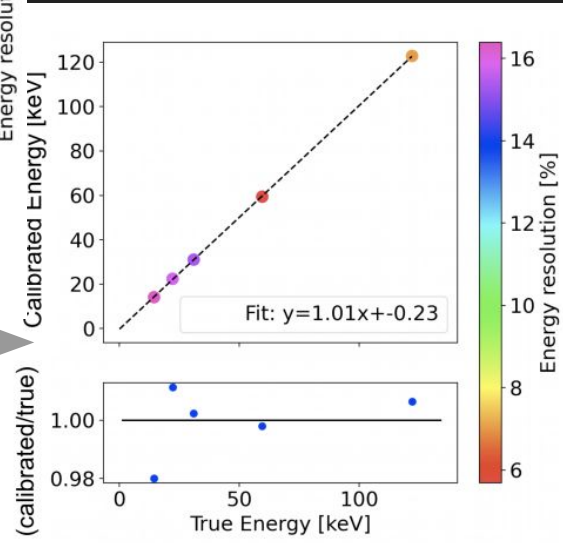
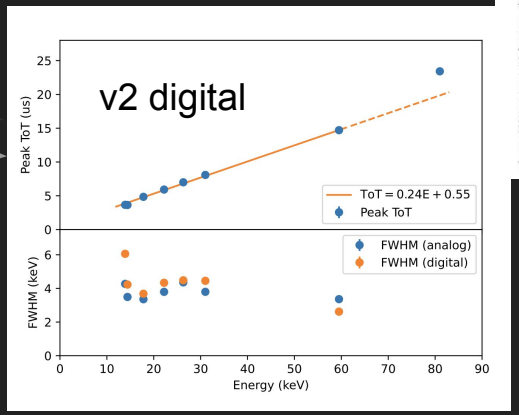
ePIC TIC

Publication history

- ATLASPix
  - https://arxiv.org/abs/2101.02665
  - https://arxiv.org/abs/2109.13409
- AstroPix_v1 (analog data)
  - https://arxiv.org/abs/2209.02631
- AstroPix_v2 (analog data)
  - https://arxiv.org/abs/2302.00101
- AstroPix_v2 (digital data), initial AstroPix_v3
  - https://pos.sissa.it/444/644/pdf
- A-STEP, utilizing AstroPix_v3
  - https://pos.sissa.it/444/579/pdf

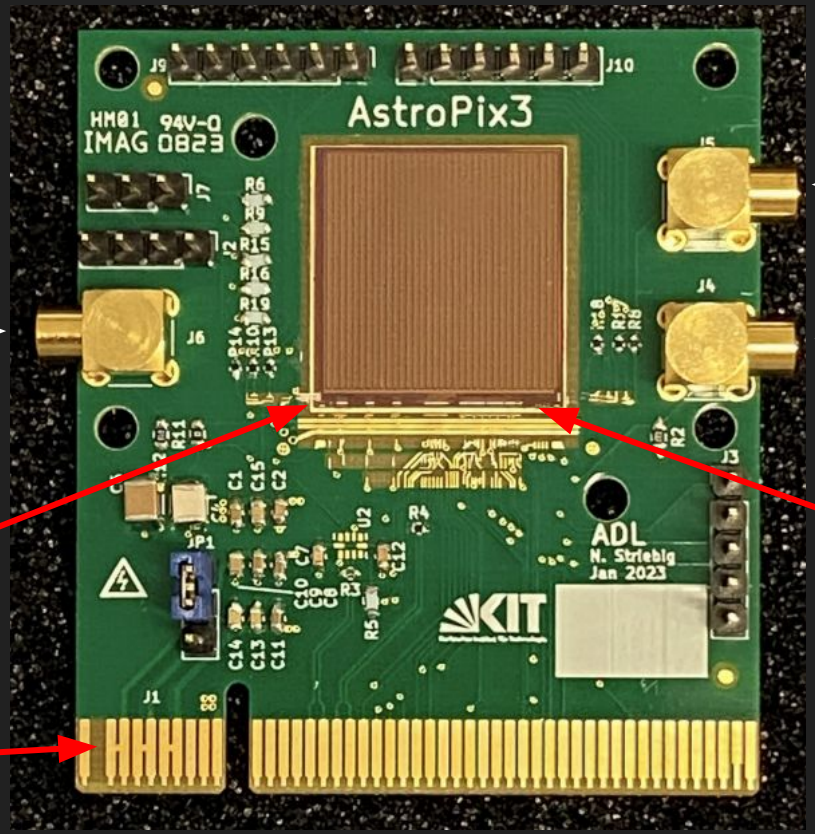






Incremental changes stepping from ATLASPix to benchmarked AstroPix

Chip PCB



200 MHz sample clock

High-voltage bias (-160V)

Output analog signal

Digital periphery, “digital top”

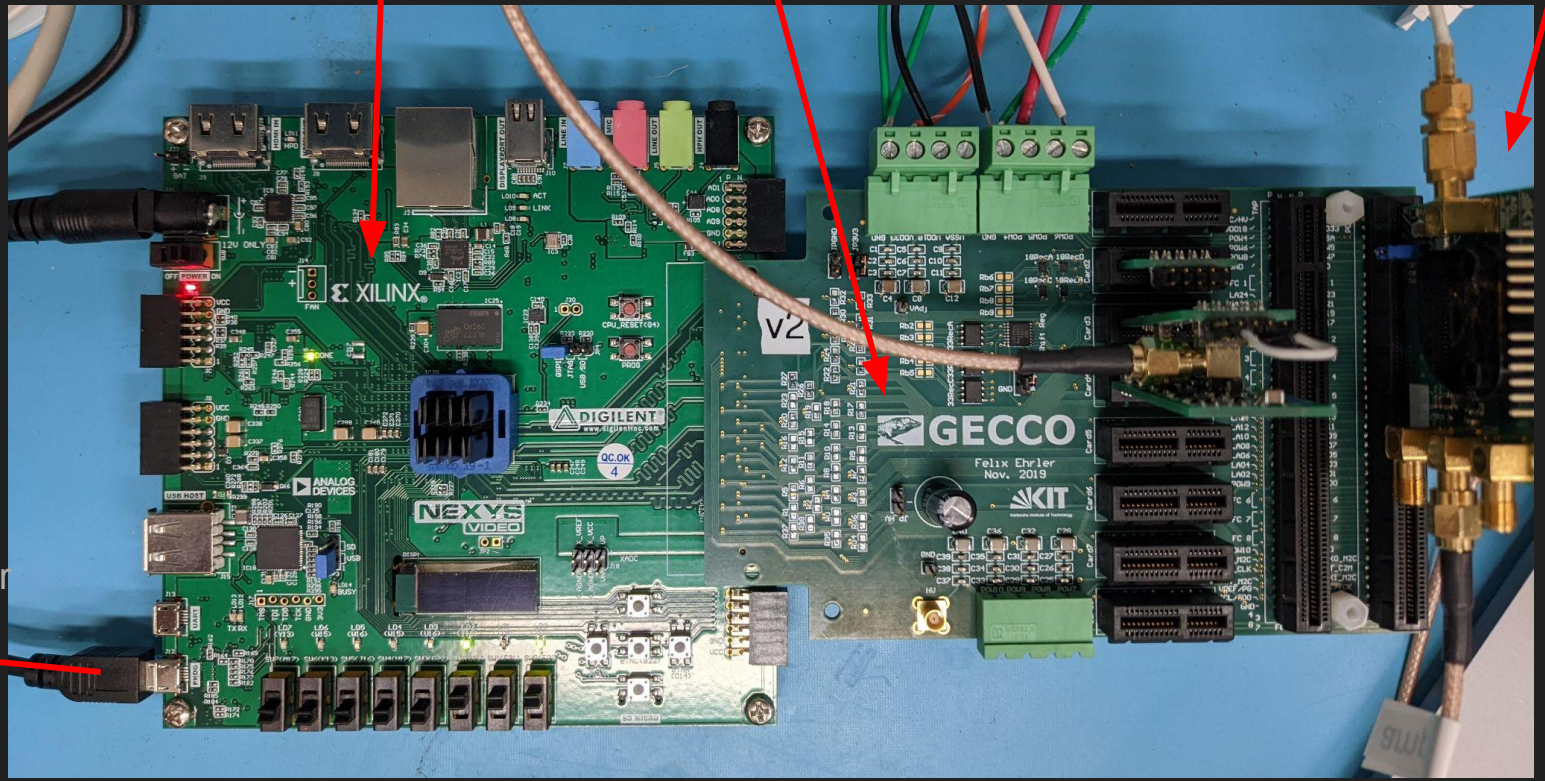
Wire bonds for power and IO

Connection to testing readout board

Chip PCB

Testing readout board

FPGA



Computer

Testing Tools

Inputs

- Injected voltage
  - Voltage generated on chip or on board and delivered to individual pixel
- Radioactive sources
  - Focusing on 14-122 keV range for now
  - Have sources with lines up to 650 keV+

Outputs

- Analog data
  - Output of the charge-sensitive amplifier
  - Requires wiring directly to the pixel so limited to the 35 pixels in first row (near periphery)
  - For debugging
- Digital data
  - Fully digitized signal
  - Full array accessable

Disclaimer slide!

The incremental development of AstroPix enables **previous chips informing the development and performance** of future versions

These results all feature the newest fabricated chip, **v3**, which serves as heritage for the improved **v4** (the final chip version for ePIC integration)

Unless explicitly stated, v3 procedures / pipelines / characterization can be applied directly to v4

Example data

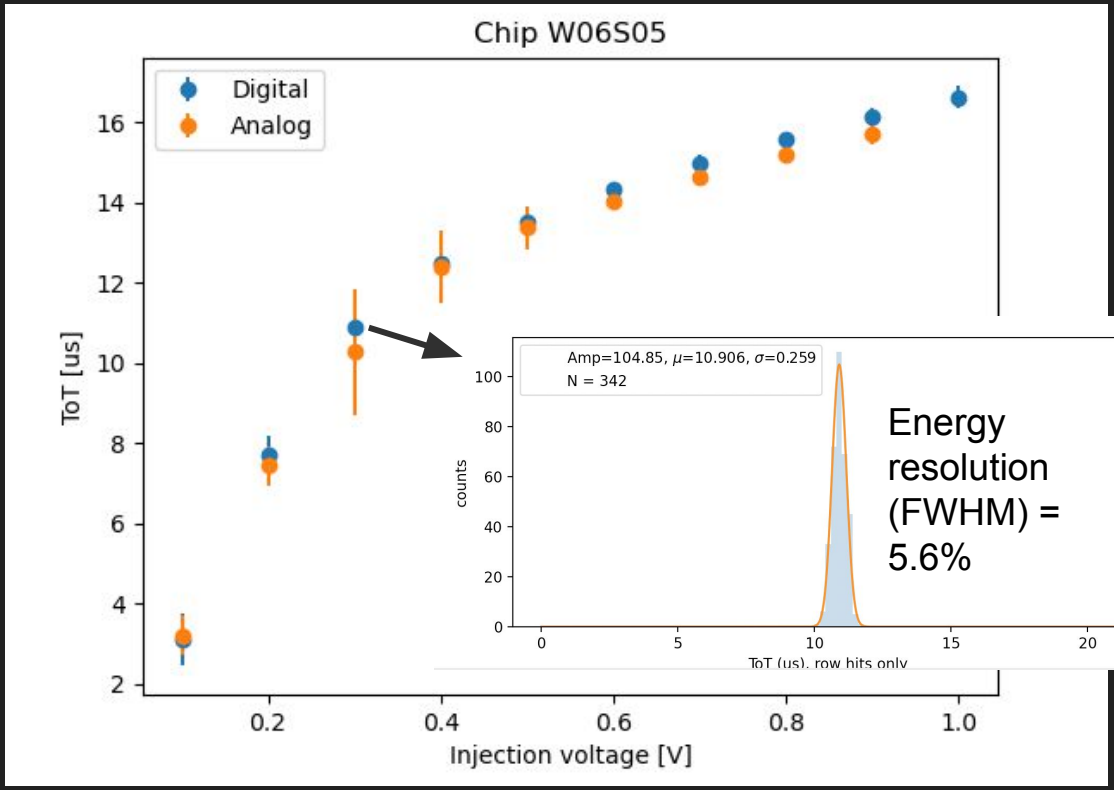
Chip returns bitstreams :

Which encode info: (v4 will encode row and col hit info in same packet)

Chip ID	payload	location	isCol	timestamp	tot_msb	tot_lsb	tot_total
0	4	0	False	119	11	55	2871
0	4	0	True	119	11	35	2851

ToT = “time over threshold” = time [μs] that signal exceeds a user-defined threshold value, global quantity in v3 but pixel-tunable in v4

Analog and digital outputs agree

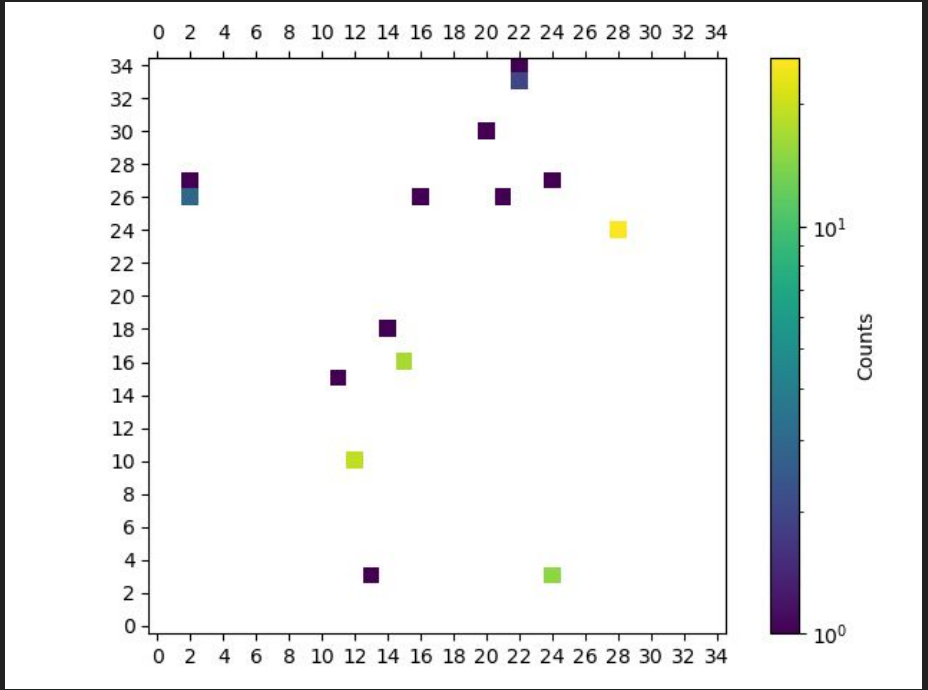


- Scan injection voltage to pixel r0c10
- Good agreement between digital and analog data (collected at same time)
  - Analog ToT “proxy” calculated off trace
- Not triggering on noise
- Precise energy resolution with clean input signal

Low noise rates

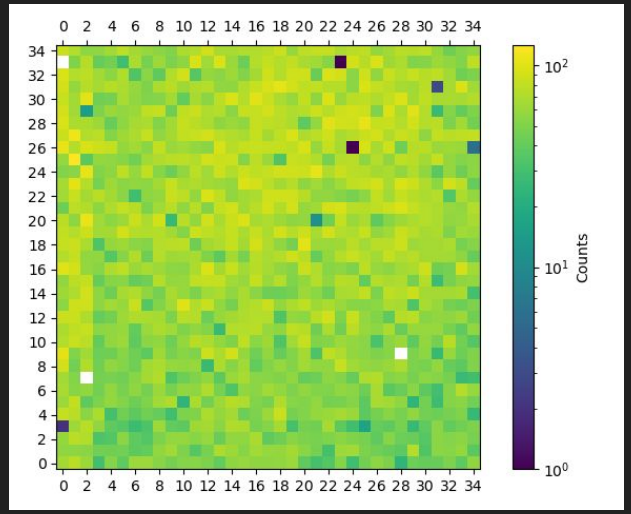
- <1% of array (6 pixels) are noisy and require masking (disable comparator output)
- No geometric factor influencing noisy pixels
- 0.6 Hz noise rate with noisy pixels masked and all others enabled

1 min noise run, ~0.5 Hz



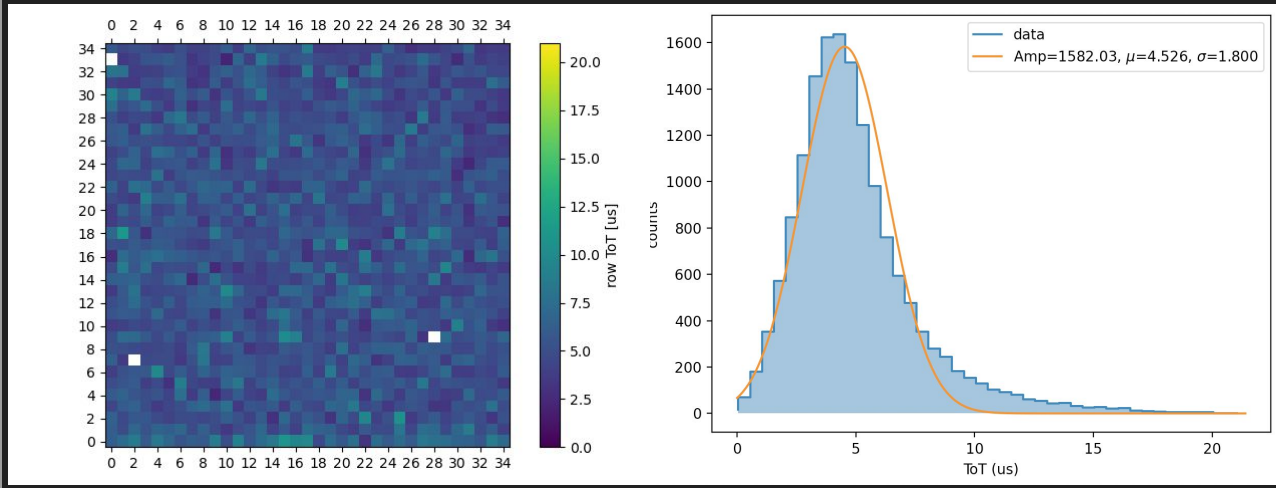
Barium-133 illumination of full array

Number of triggers



Even activation across full array

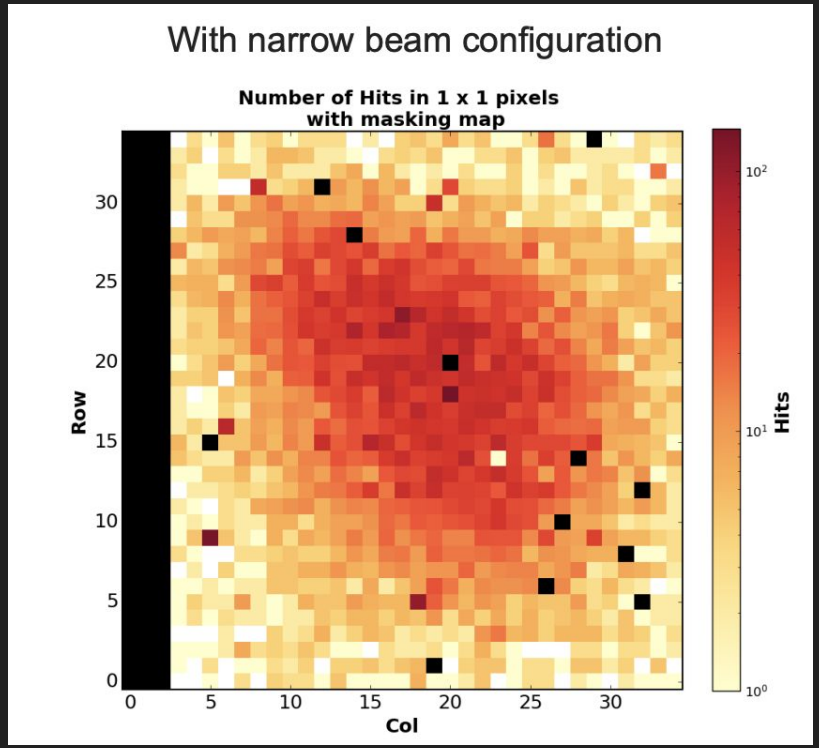
Mean ToT of distribution from each pixel



- Variability V = σ/μ *100% = 39.7%
  - WIP = final configuration optimization
- We have known since v2 that individual pixel calibration will be required
  - WILL NOT BE NECESSARY FOR v4 with individual pixel tuning

Radiation testing in 120GeV proton beam, FNAL

- 20000 protons/spill
  - Much harsher environment than EIC
- 4.6 mm 5.4 mm beam spot
- 3 hours of data collection
- Total 16,629 raw events
  - 63.28 % of events were decodable
  - 86.94 % of pixels were fired
  - Software not optimized for this uniquely large flux
- Passive and active irradiation studies indicated low risk of latchup / complications
- Continuing work/collaboration with facilities at FNAL



Software and Firmware Development Highlights

SW led by N. Striebig (KIT) and A. Steinhebel (GSFC), FW led by R. Leys and N. Striebig (KIT)

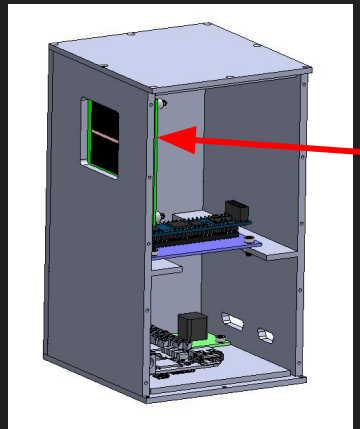
- FW-driven SPI readout to reduce deadtime
  - Chip itself triggers readout when there is data in buffers without SW check
  - Sensor data frame detection, IDLE discard, Tagging/reframing, routing to single Readout Buffer
- FW Scale-ability
  - Read through the daisy-chain in FW rather than SW
  - Up to 20 daisy-chained SPI input has own interface which feed into global buffer (one chip reads out a time)
- SW speedup to match FW
  - Reduce chance of incomplete data return
  - Speed-up in analysis scripts, esp. when probing every pixel individually

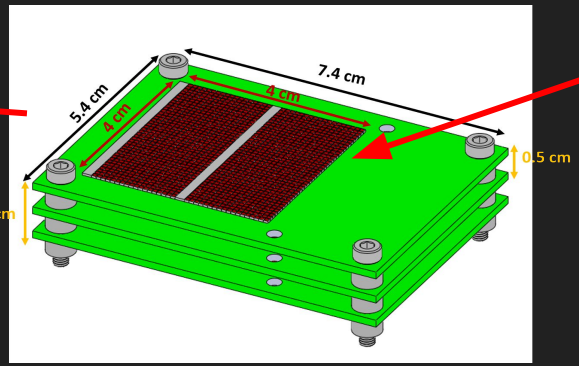
Next Steps

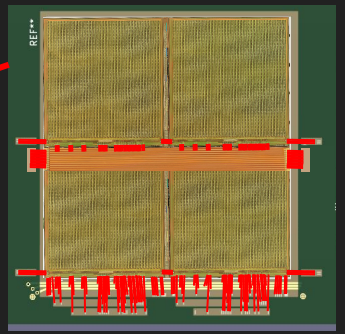
- Full array calibration, including individual-pixel corrections (not needed in v4)
- Finalize configuration settings, including global threshold level (not needed in v4)
- Measure depletion depth with transient current techniques (TCT), compare to simulation

A-STEP payload

- Validate operation of v3 quad-chip in space environment on sounding rocket
  - 3-layer prototype system
- Build structured chip test program and sophisticated FW/SW/analysis pipelines that can be directly applied to ePIC







Backup

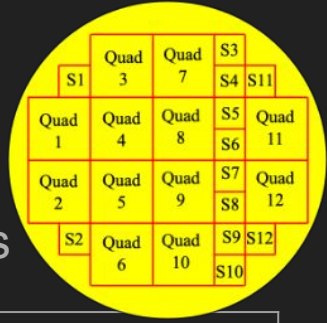
Digital Data

DIFFERENT DATA STRUCTURE IN V3 THAN IN V4

- OR row and column information to only two channels (row, col) are sent to digital top
  - Pixel array acting like strips
- Encoded digital information:
  - ChipID - relates chip to location in daisy chain
  - Payload - relates to SPI line
  - Location - row or column with comparator that measured over threshold
  - Timestamp - 8bit value counted with 2 MHz clock
  - isCol - boolean for row or column
  - LSB, MSB, ToT - time over threshold value, converted to us offline given clock speeds
- Each hit (row or column data packet) = 5 Bytes
- A “good event” requires:
  - One row and one column packet in same readout stream
  - Matching timestamp
  - No ToT matching requirement at GSFC

v3

V3 substrates

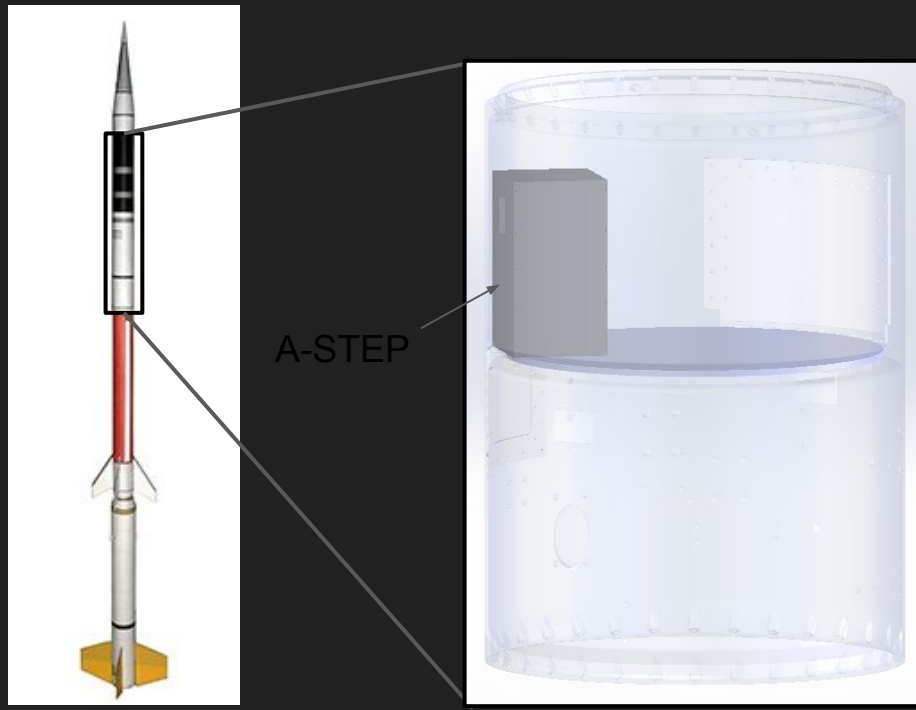


Fabricated chips (single chips and quad-chips) using 3 different substrates

	TSI Substrate	Okmetic Substrate	Topsil Substrate
Purpose	Testing	Backup	Flight
Resistivity [Ω*cm]	50	300-400	10,000
Number of wafers	2	2	3
Diced and mounted on test board?	Yes	No (in progress)	Yes
Breakdown voltage [-V]	250	290	High leakage current (uA) with any applied voltage
Leakage current, -150V [-nA]	40	40	High (80mA at -30V)
Testing notes	Low-quality substrate, high pixel variability	Primary test substrate, to fly on A-STEP	Challenging - WIP to understand

Work to be done for A-STEP

- First flex bus bar designed to connect upper 2 chips in quad chip ✅
- First test of chip daisy-chains
- Scaling of firmware to handle multiple chips / multiple layers ✅
- Mechanical testing of wire bonds, support structure (windowpane-like supports, not solid PCB)
- Flight software for data packetization and telemetry (new sophistication to DAQ)
- Eventual environmental testing of full system
  - Vibration, temperature/vacuum, etc



Firmware Development Highlights

Led by R. Leys and N. Striebig (KIT)

- Two FW lines
  - “simple” / easily hackable version for 1 chip and NEW multi-layer / multi-row FW
- Support for multiple targets
  - Different FPGA boards (bench testing vs A-STEP flight) and chip configs (single chip, multi-layer, etc)
- FW-driven SPI readout
  - Previously, SW-driven readout strategy introduced additional deadtime
  - Now chip itself triggers readout when there is data in buffers
  - Sensor data frame detection IDLE discard, Tagging/reframing, routing to single Readout Buffer
  - Readout config options: Continuous, interrupt driven, trigger support (in development), etc
- Scale-ability
  - Read through the daisy-chain in FW rather than SW
  - Each daisy-chained SPI input has own interface which feed into global buffer (one chip reads out a time)
    - Supports up to 20 SPI inputs but exact number in use can be easily modified

MORE Firmware Development Highlights

Led by R. Leys and N. Striebig at KIT

- Host communication
  - Interface with computer via Host SPI, USB-UART, FTDI USB-FIFO (for now)
- Simulated test structures and ease of coordinate development
  - Improved Python SW interfacing with FW type
  - Version discovery to ease SW development
  - Simulate hit data at “SPI interface to global buffer” level
  - Python-based verification (Cocotb) allows SW testing in simulation, regression testing
  - WIP: Generate physical SPI frames for verification simulations (N. Striebig, S. Scherl)
- Housekeeping
  - Include packets of housekeeping data in data stream, as defined by user (voltages on FPGA, FPGA temp, etc)
  - FPGA XADC driver for internal values, SPI channels for external ADC
  - Readout and external IC support fully SW driven