Alternative vendors readout chip update – erd109 effort

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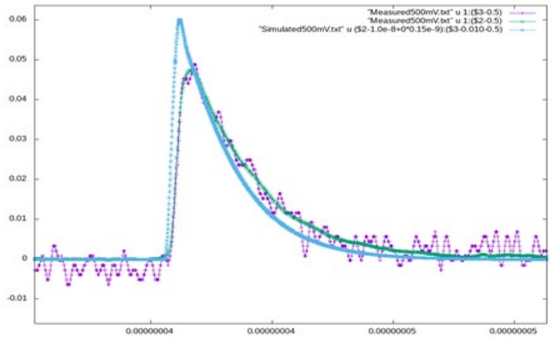
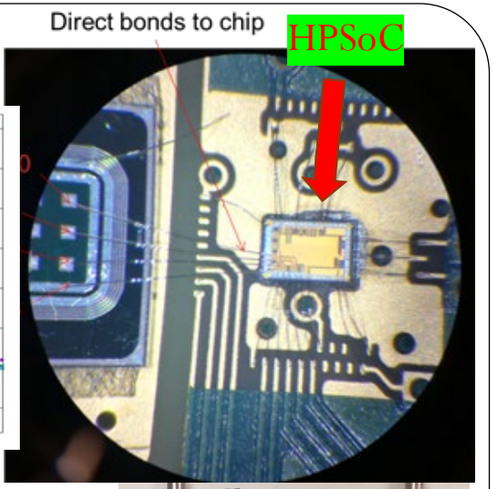
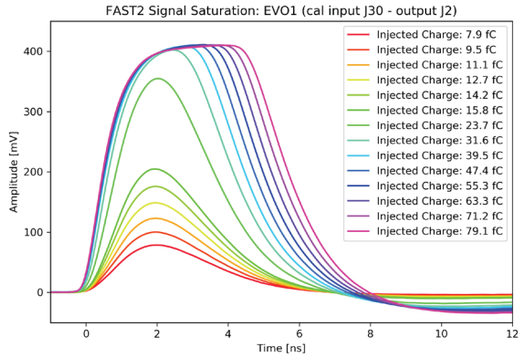
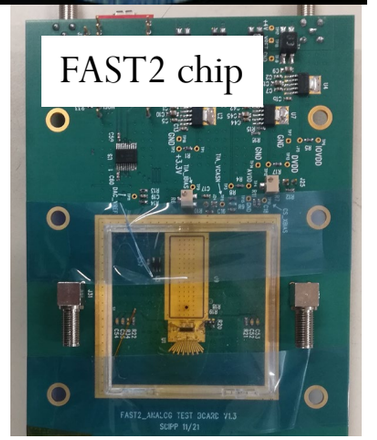
Alternative vendor chip status

- UCSC is working on three alternative vendor ASICs for ePIC
  - AC-LGAD readout
- Goal
  - Fast timing, Jitter <10 ps
  - Power < 1 mW per channel

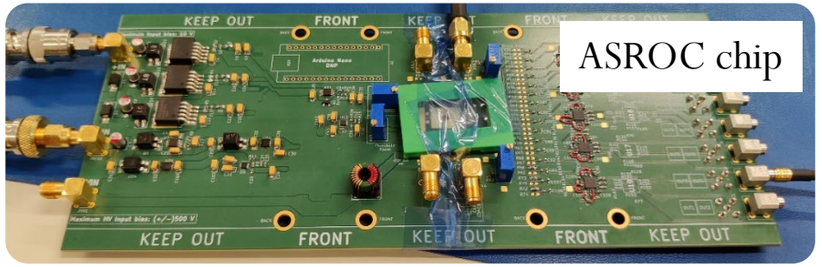








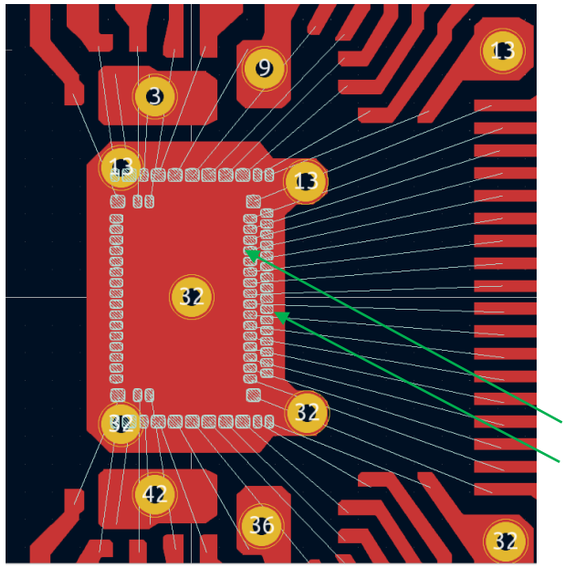
Institution	Name	Technology	Output	# of Chan	Funding	Specific Goals	Status
INFN Torino	FAST	110 nm CMOS	Waveform & TDC	20	INFN	Large Capacitance TDC	Testing
NALU Scientific	HPSoC*	65 nm CMOS	Waveform	5 (Prototype) > 81 (Final)	DoE SBIR	Digital back-end	**V2 ready**
Anadyne Inc	ASROC**	Si-Ge BiCMOS	Discrim.	16	DoE SBIR	Low Power	**Testing**

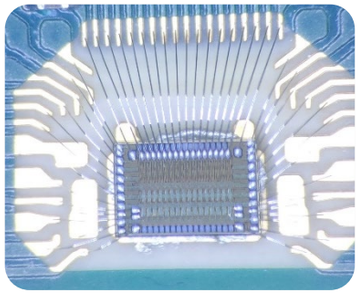


AS-ROC status

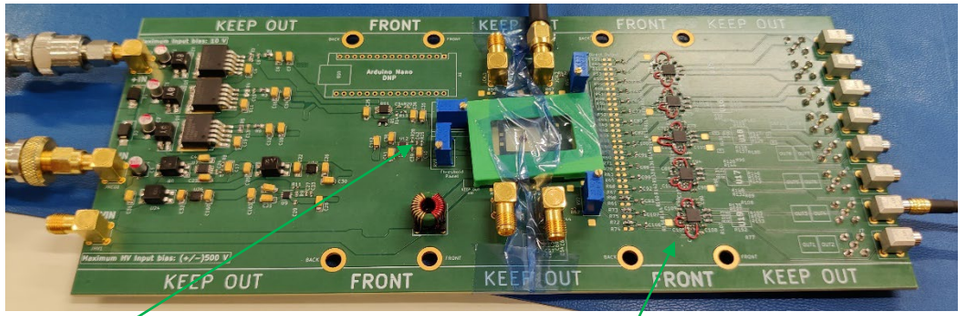
SiGe readout chip

- Chip developed together with Anadyne Inc. (actually run by former SCIPP members) and J. DeWitt
  - Received ~2 weeks ago
- Use of Tower Semiconductor SiGe technology
- AC-LGAD readout for EPIC
  - Low power consumption (<1mW/ch)
  - 16 channels
  - Developed for low input capacitance (pads)
  - **Both analog and discriminator output**
- Readout board developed by SCIPP
- Two version of the chip: low and more power
  - **Results shown for low power version**, another board will be ready soon to test more power version





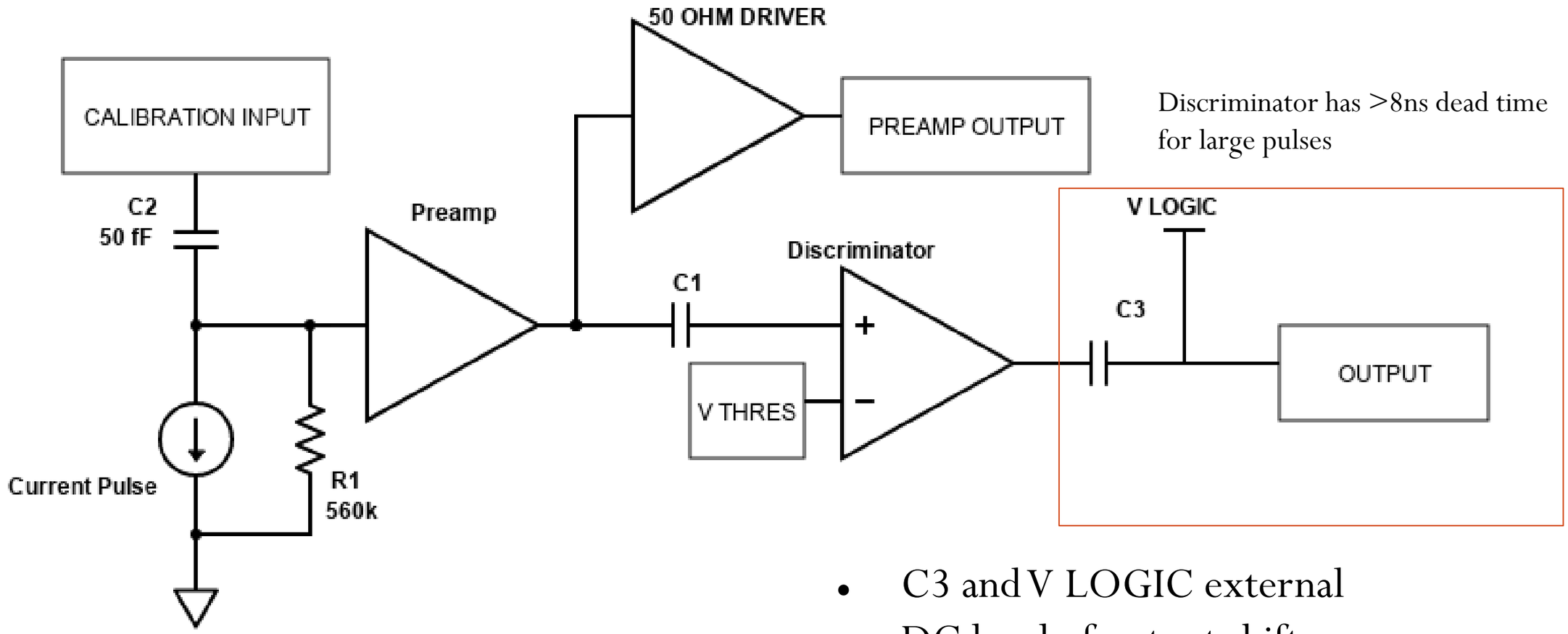
Analog Discriminator



Potentiometers to change discriminator threshold

Buffers

Block Diagram



Discriminator has >8ns dead time for large pulses

- C3 and V LOGIC external
- DC level of output shifts over Monte Carlo, cap reduces jitter
- Disc cannot drive 50 Ohms

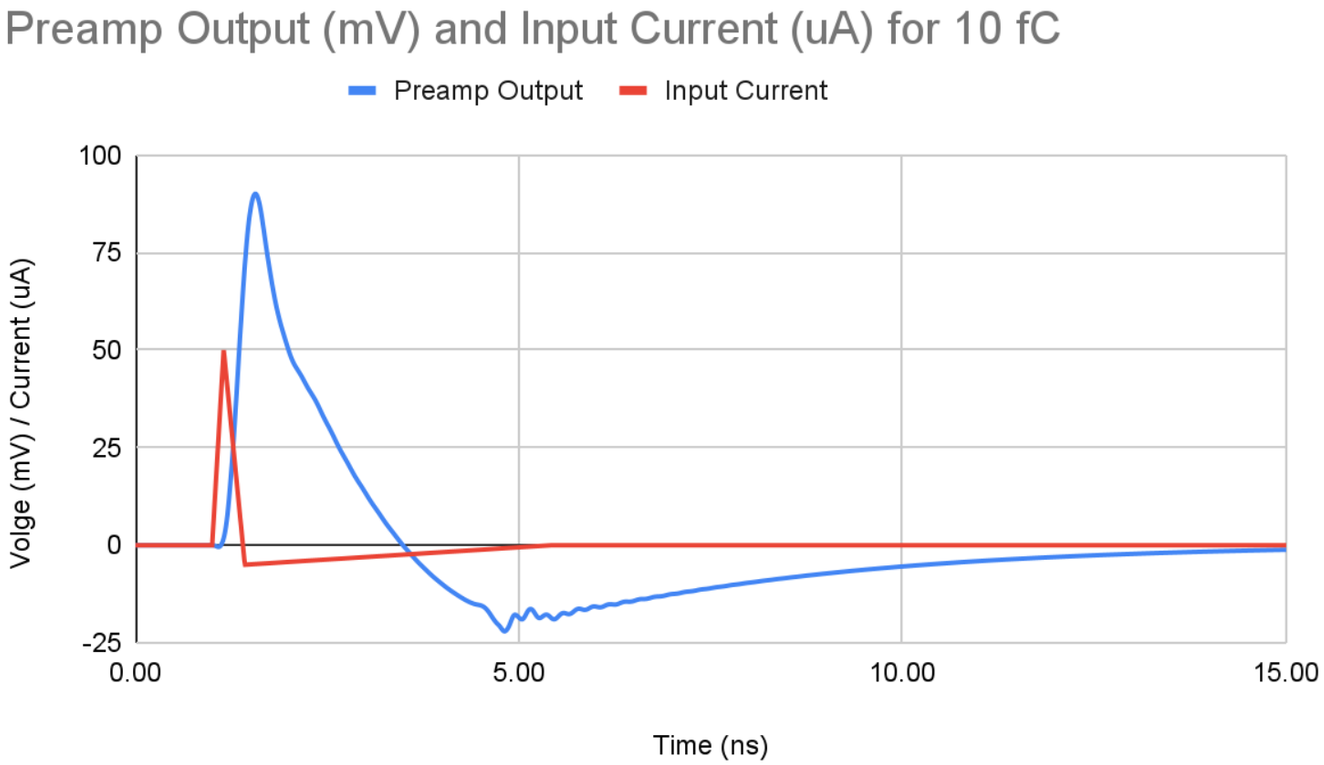
Simulation - Input Signals

Rise time = 150 ps

Fall time = 250 ps

Undershoot = 10 % (total charge = 0)

Sensor capacitance = 200 fF



Simulation - Timing Resolution

Jitter measured at 1 V threshold

Low input charge timing resolution strongly dependent on power draw

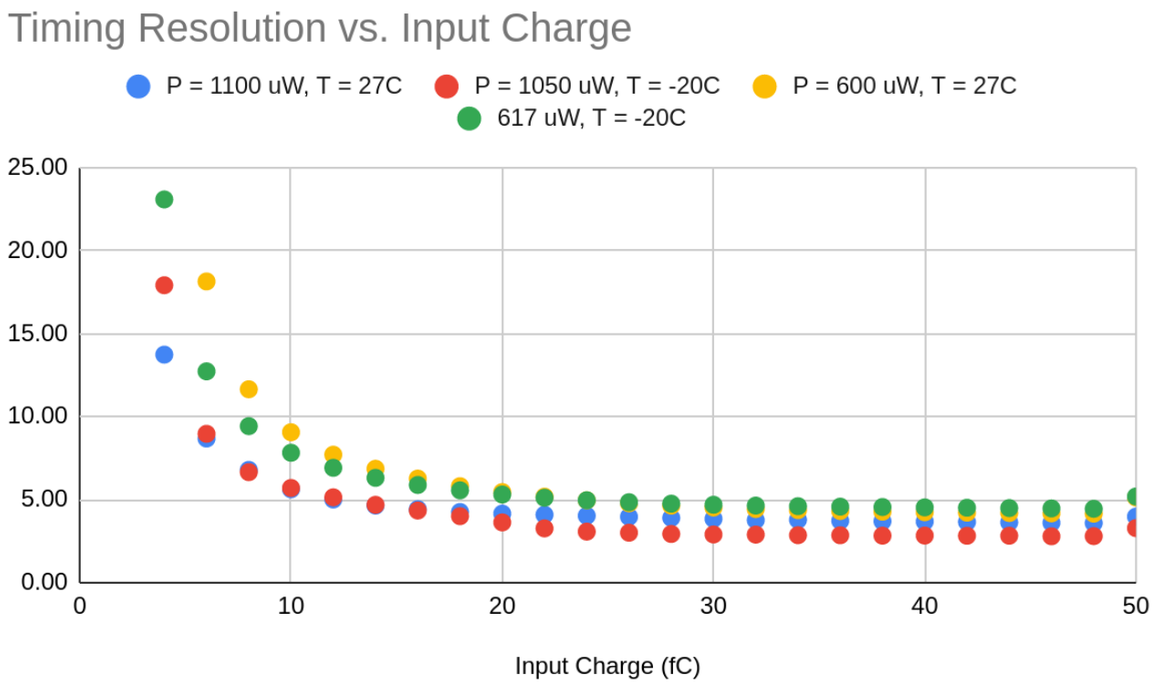
Threshold ~ 2.2-3.7 fC

Preamp noise ~ 0.4-0.7 mV, signal 18-35 mV

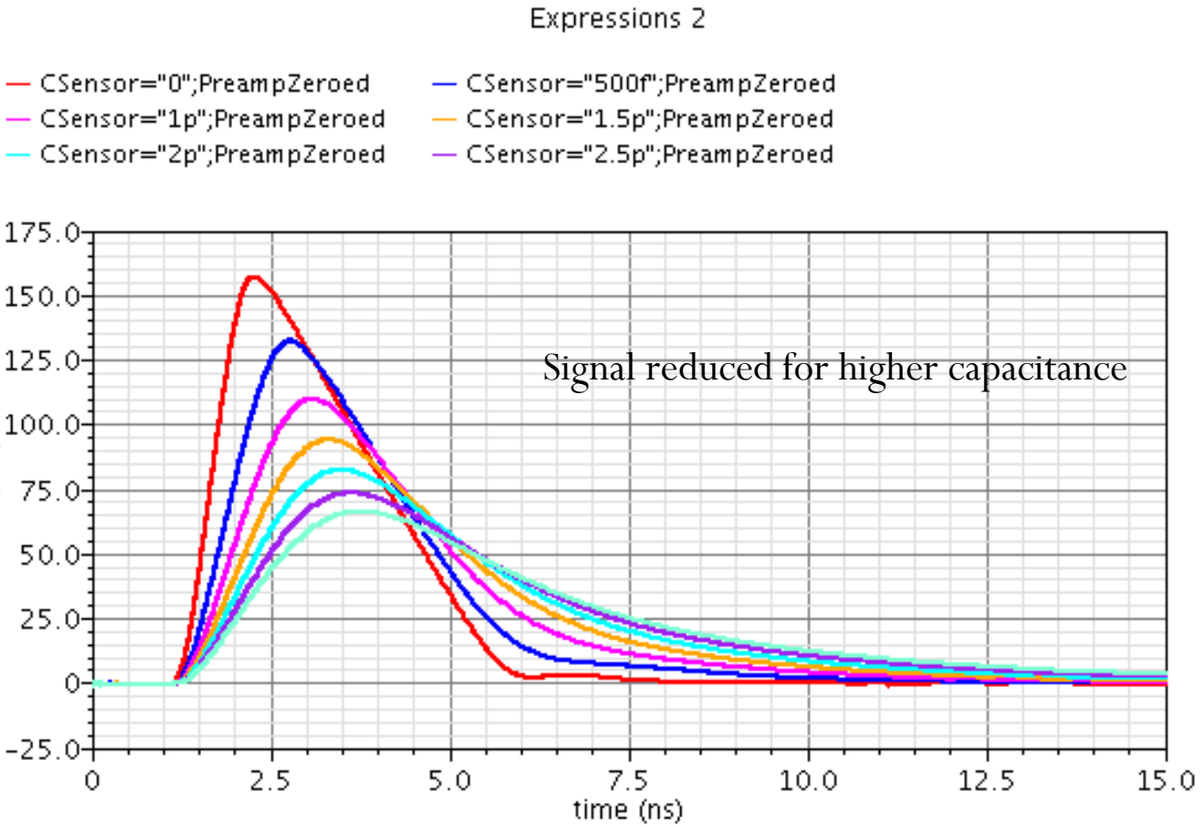
Performance improves with lower temperature

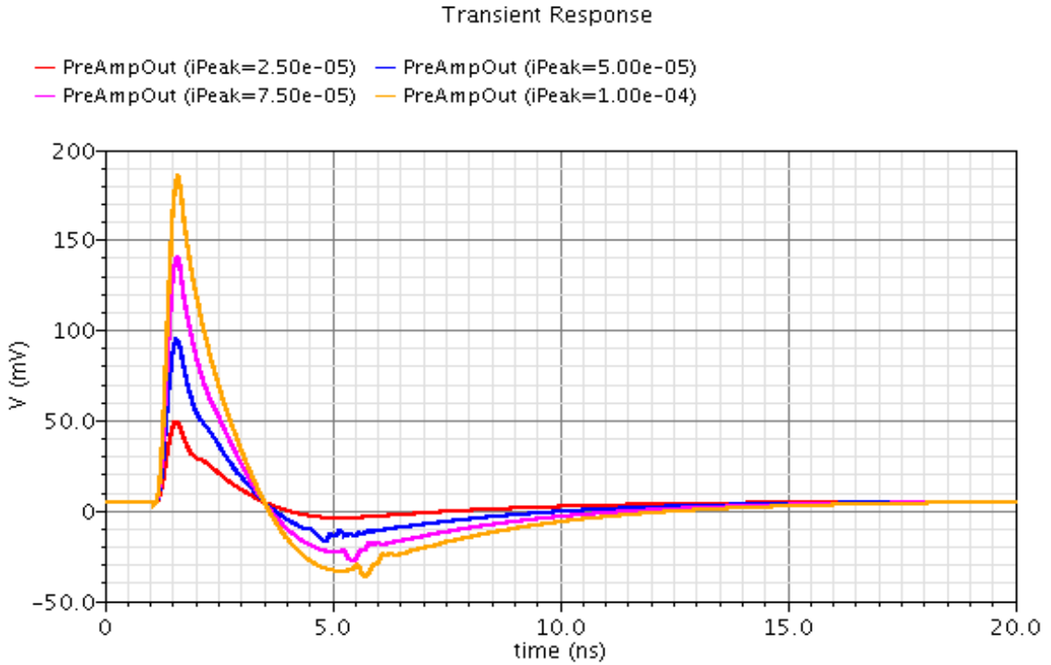
Decreasing the threshold greatly reduces performance for < 10 fC of input charge

Resolution improves ~ 2 ps at 490 uW at -20 C

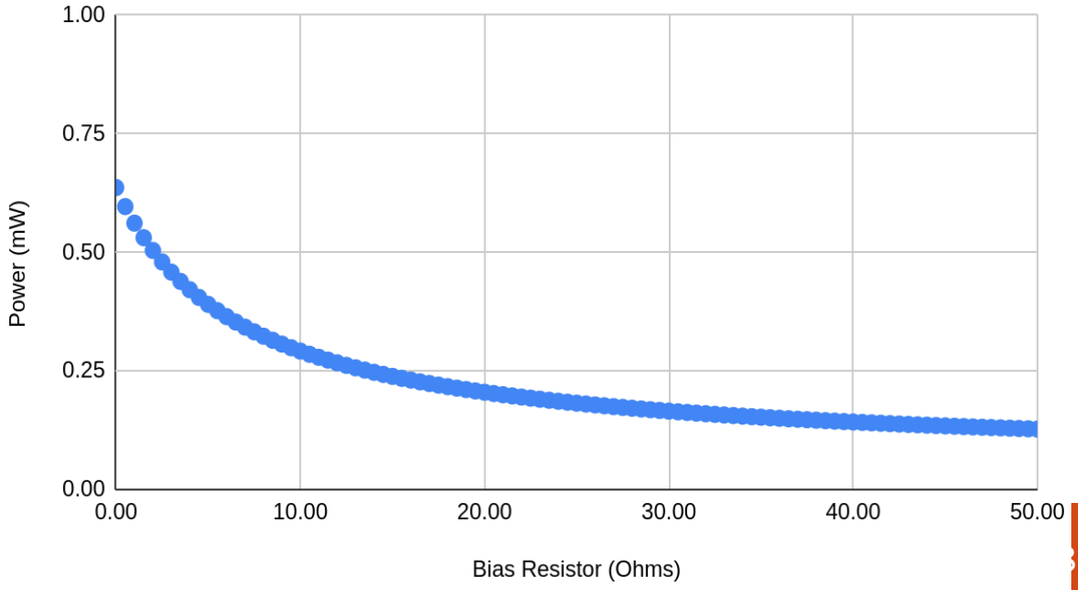


Simulation - Preamp

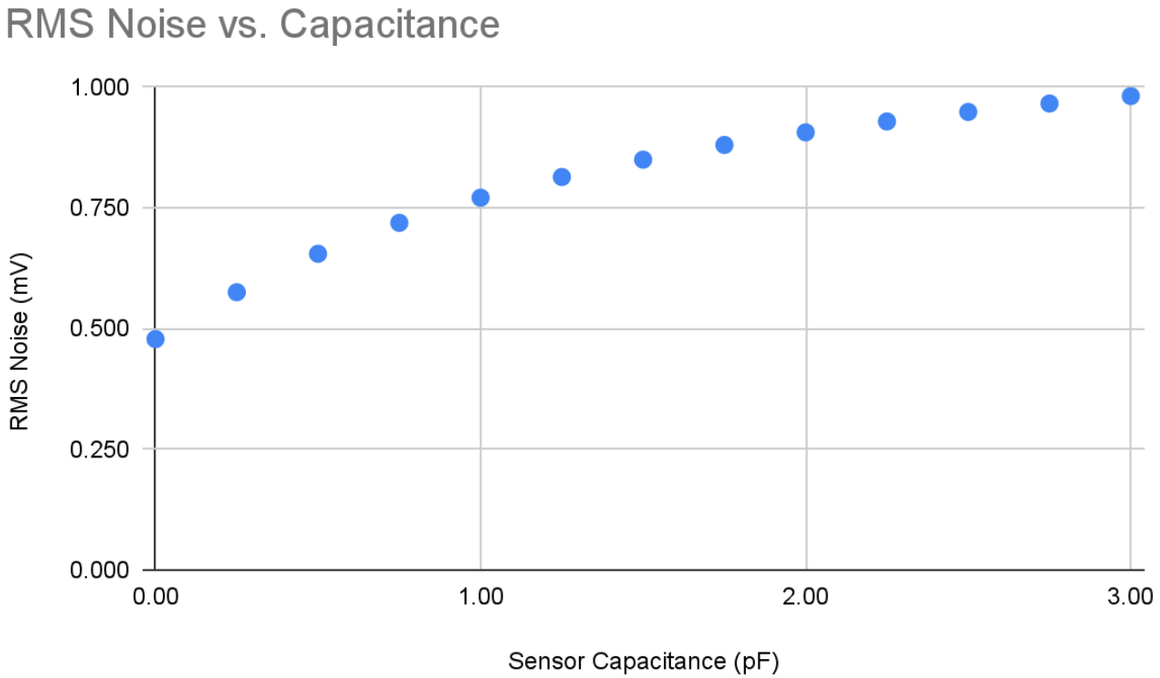


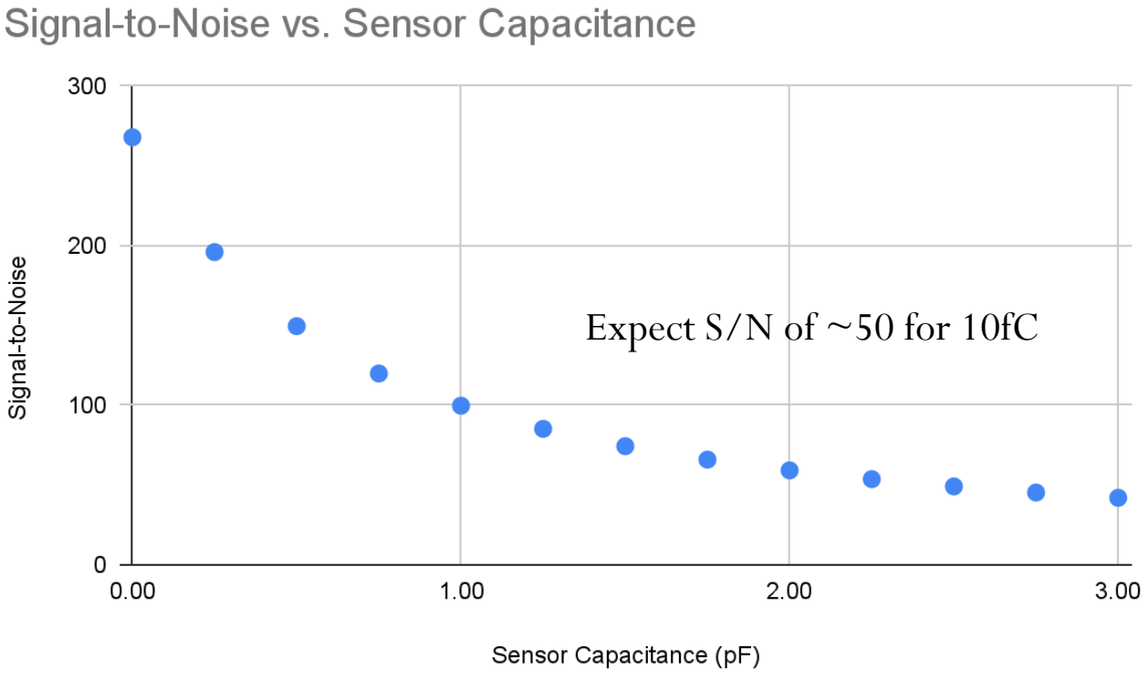


Front End Power vs. Bias Resistance



Preamp Signal and Noise - Simulation

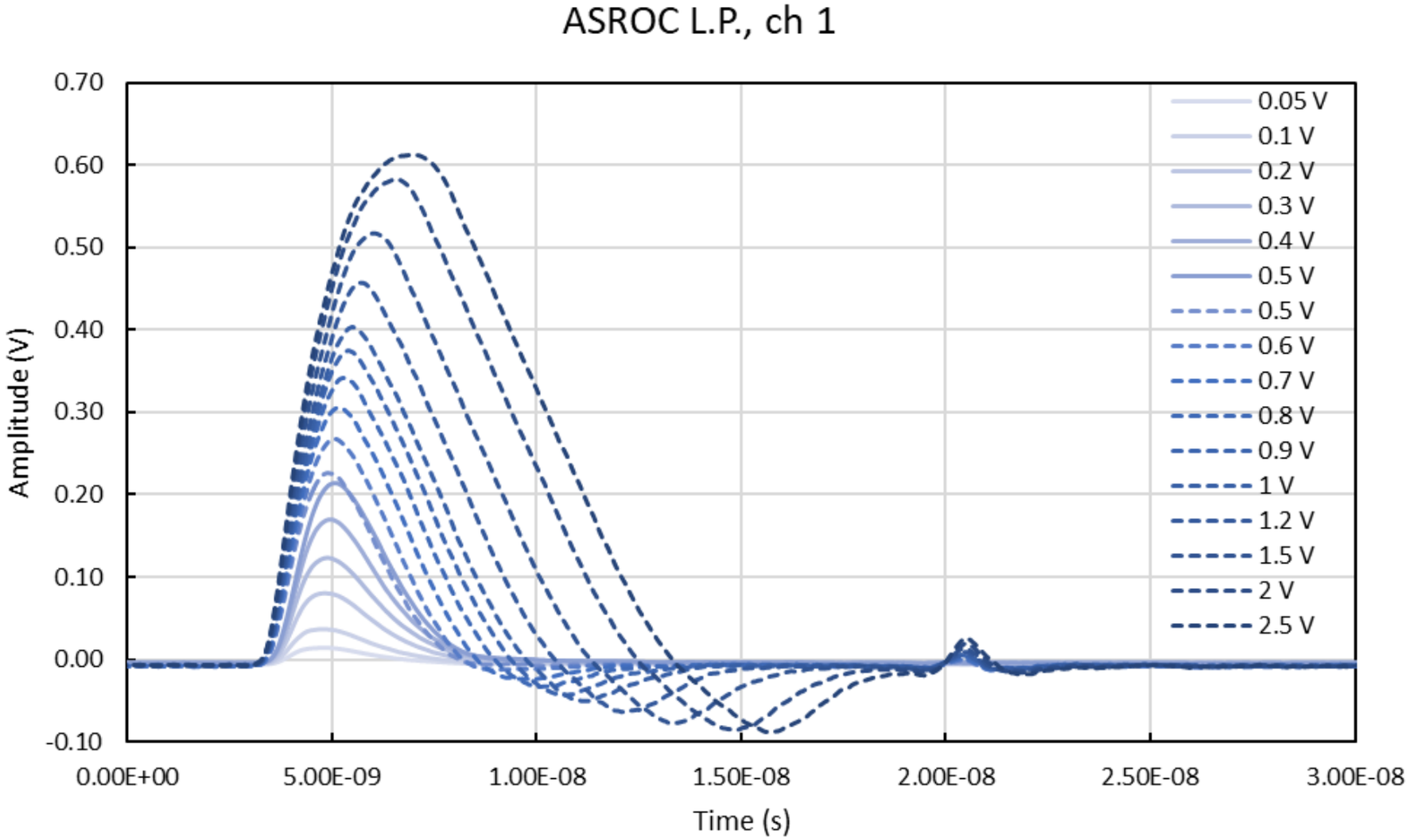




Noise was integrated from 1 Hz to 2 GHz

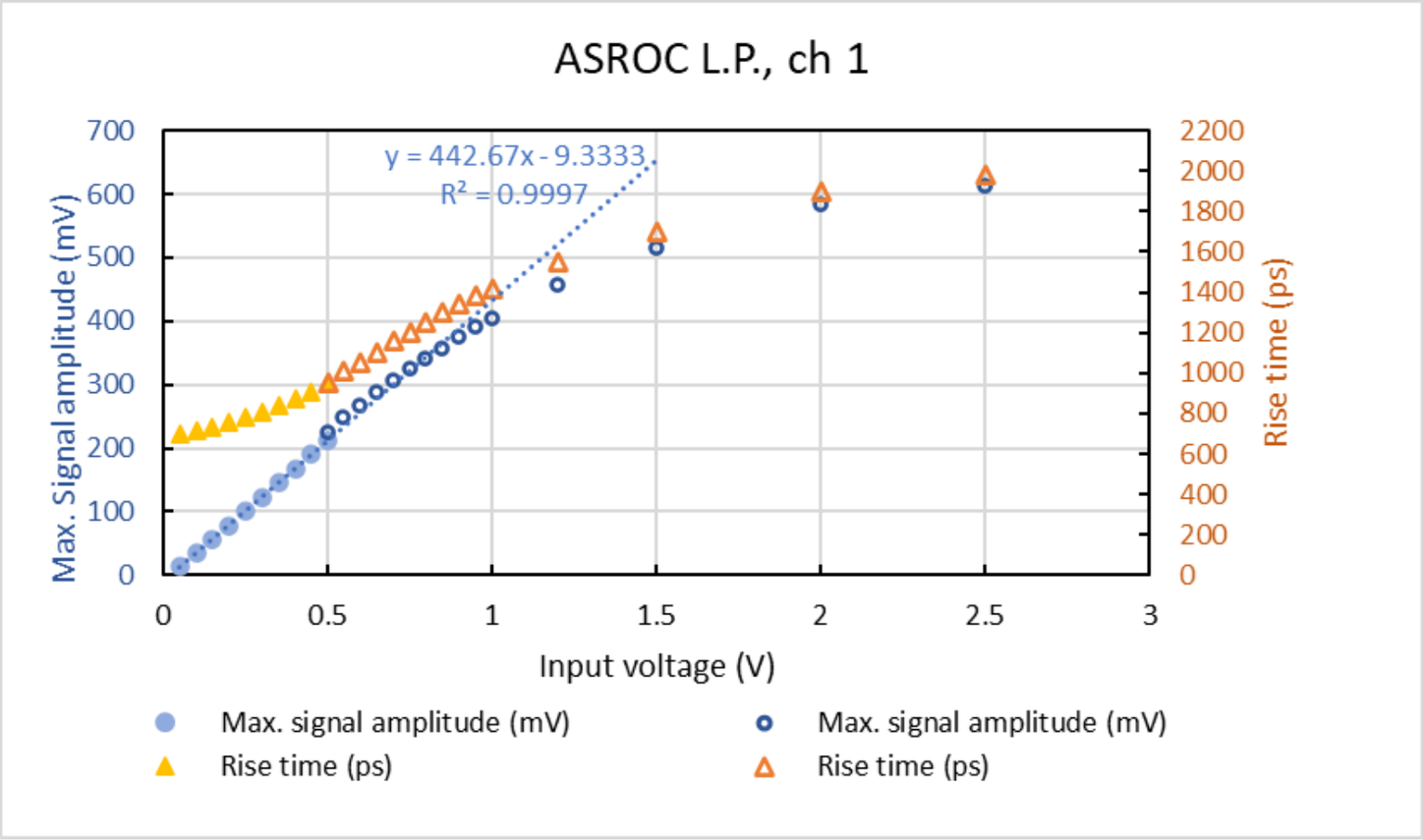
Preliminary pre-amplifier results - data

- Calibration input on the board
  - 50fF calibration capacitance on chip
- Input signal: square pulse with height as in legend
  - 50 mV to 2.5 V
  - 50 mV input → 5mV/2fC output
- Output between ~10mV and ~600mV



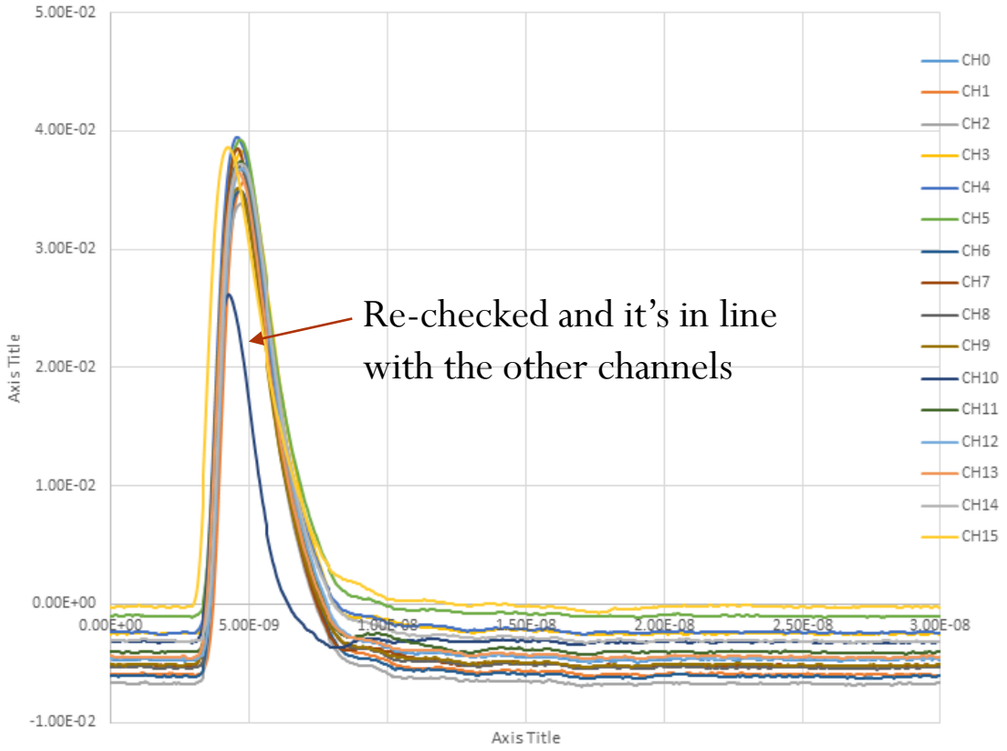
Preliminary pre-amplifier results - data

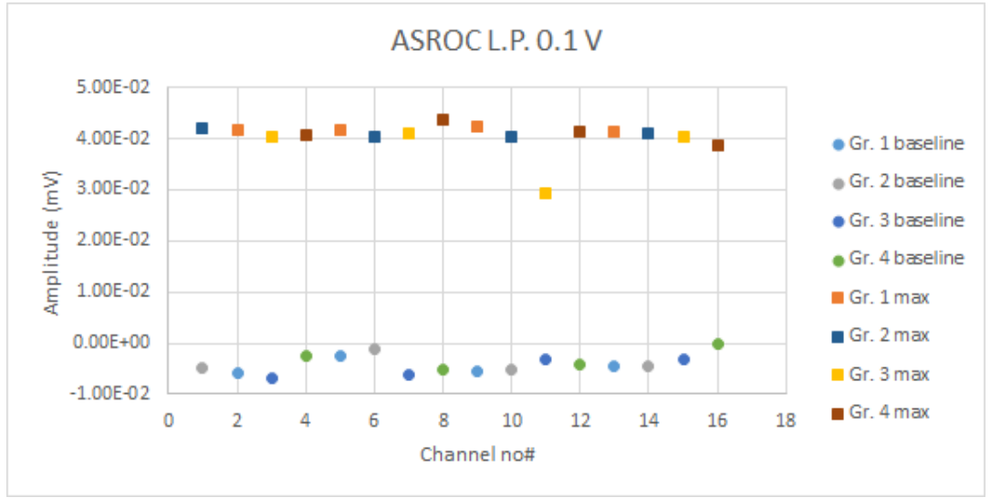
- Good linearity until ~1V input. ~2.5mV per fC (for 50fF calibration capacitance)
- Rise time between 700ps and 2ns (higher than expected)

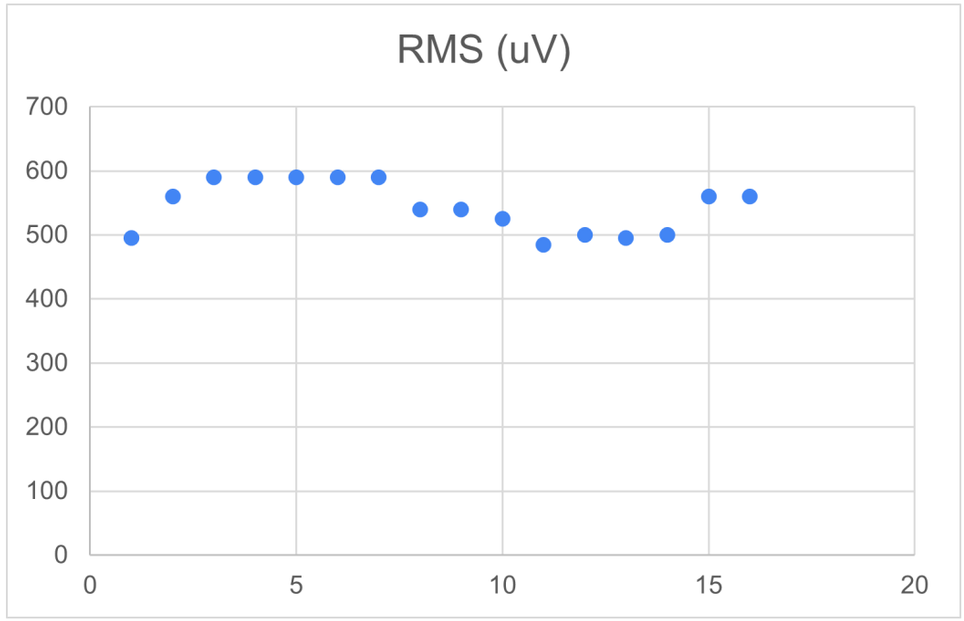


Preliminary pre-amplifier results - data

- Small baseline shift (<10 mV) likely induced by the buffer
- Very low noise (~500 uV) but this is almost without input capacitance (likely ~100 fF)
  - Scope with 2GHz bandwidth (scope noise ~300 uV)

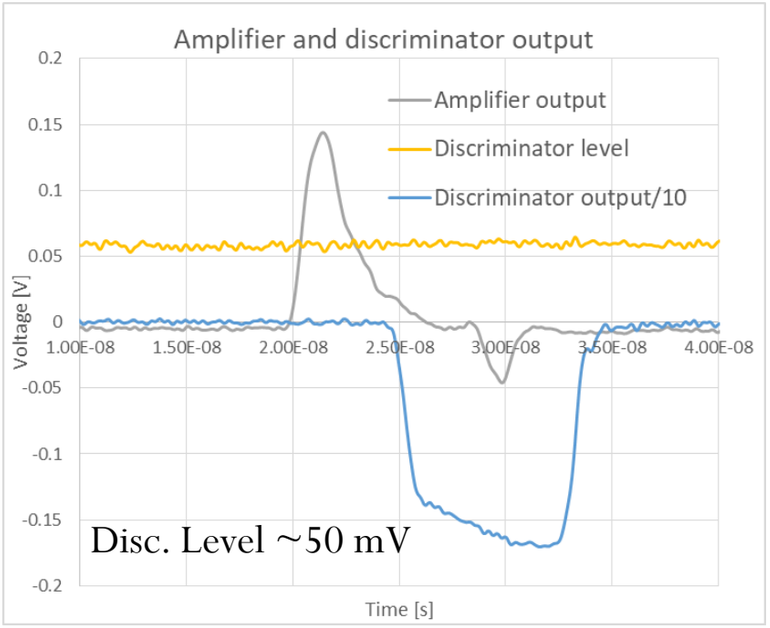


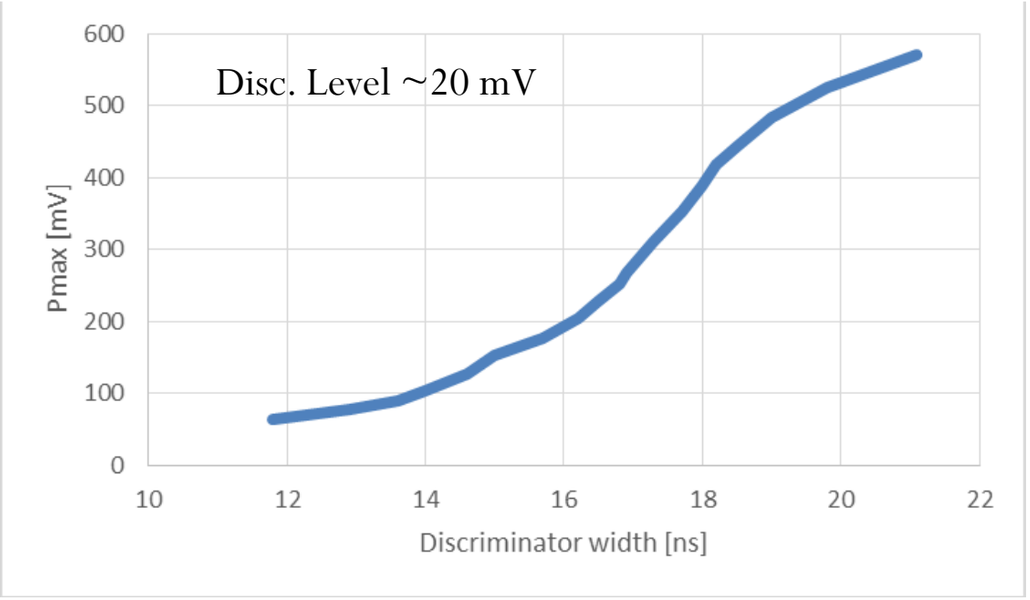




Preliminary discriminator results - data

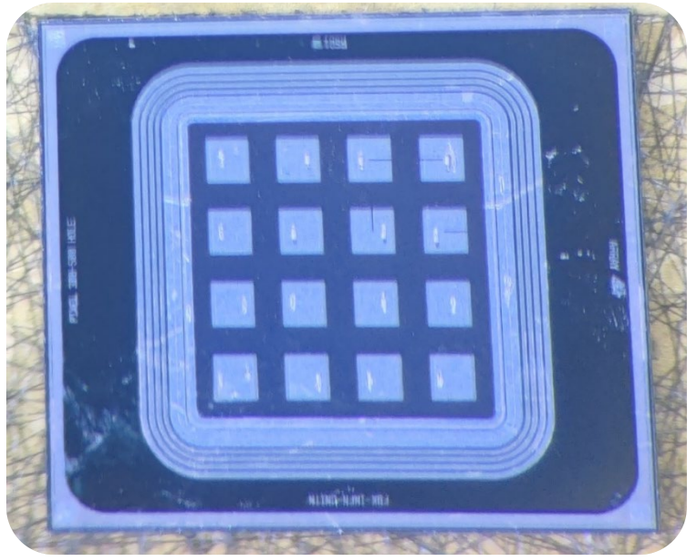
- **Discriminator performance**
  - Discriminator output is an adjustable (1.5V in the tests) step function with rise time < 1 ns
  - Discriminator Jitter < 10 ps
  - Discriminator level can be adjusted with external reference
  - Width of the discriminator output is proportional to the pulse maximum
    - Can be used to correct arrival time for time walk

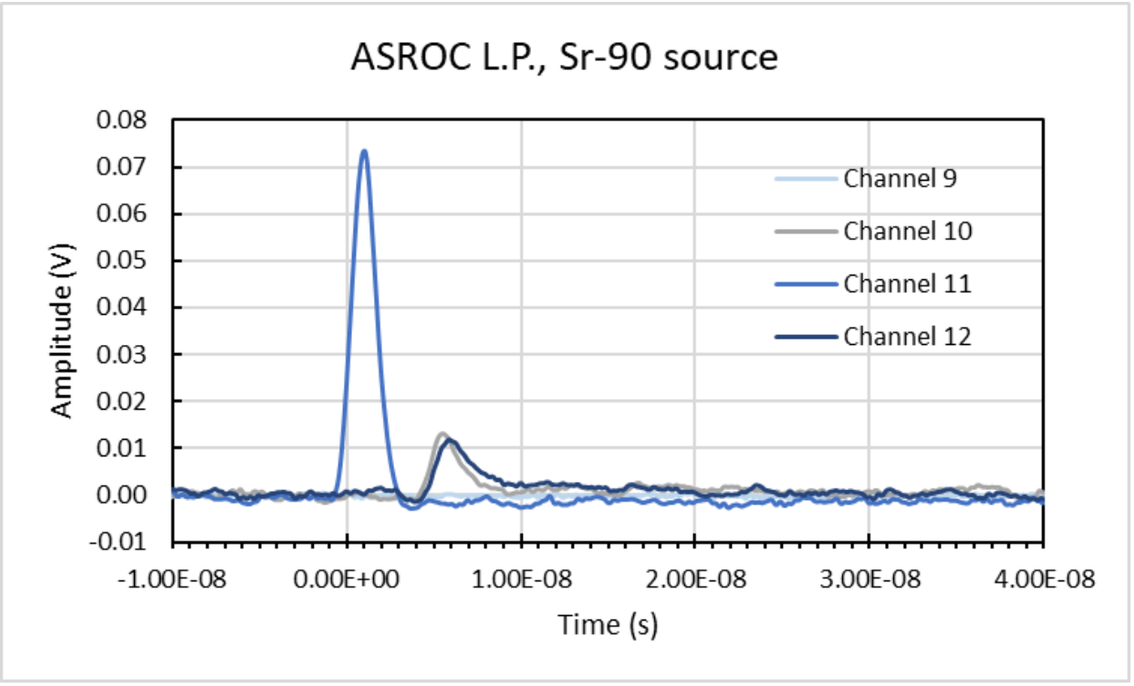




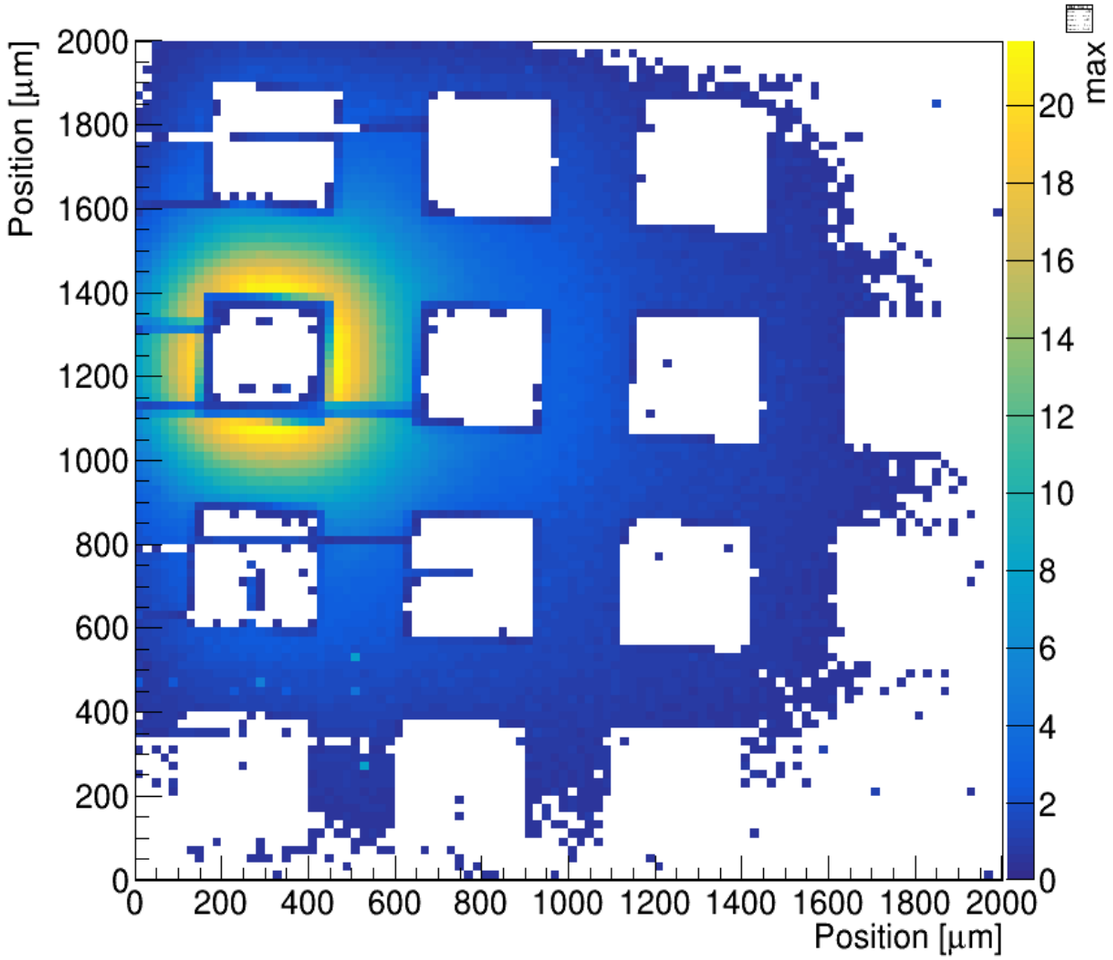
Sensor pre-amp output

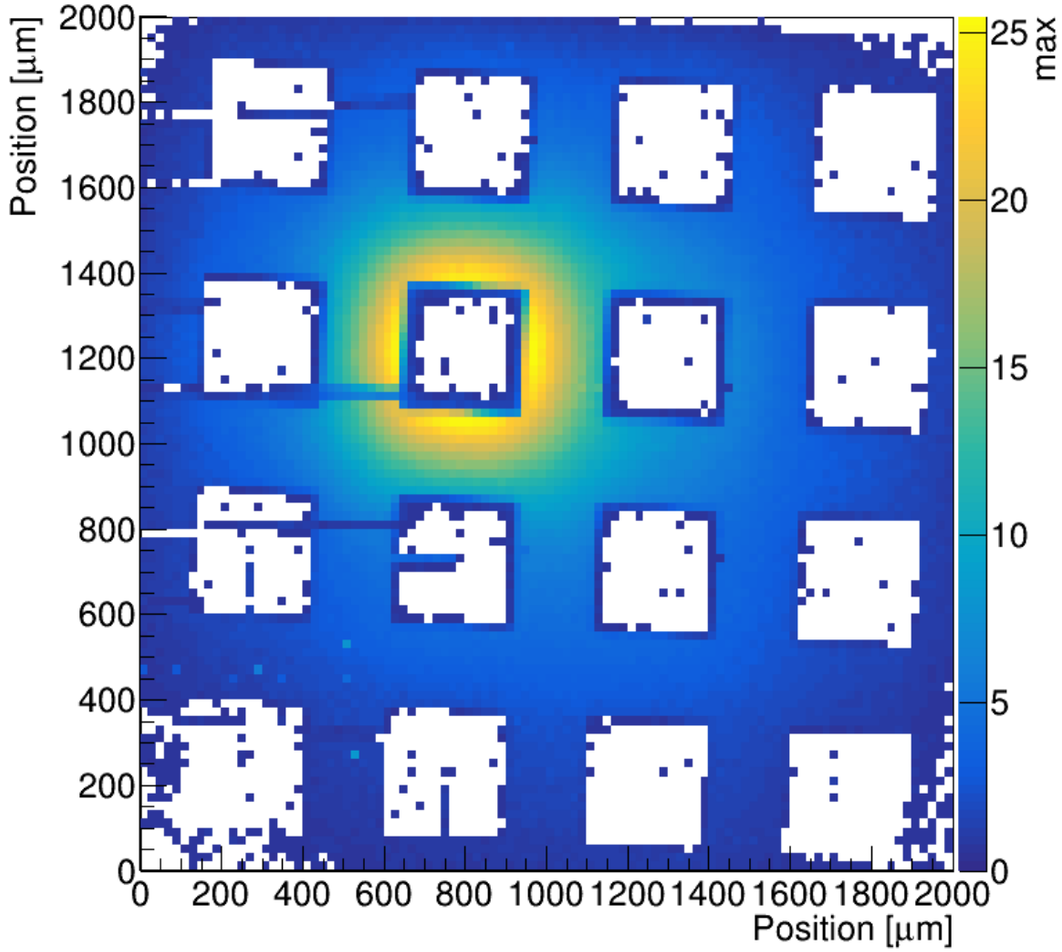
- **Performance with sensor**
- Connected to a pad AC-LGAD (from FBK RSD1 production)
  - 500 um pitch, 300x300 um pads
  - Sensor couldn't run at high gain (somewhat high leakage current)
  - For discriminator test we had to increase laser power to have larger signal
- Noise level ~700 uV for input capacitance of 500 fF
  - As expected!
- Tested with Sr90 beta source and TCT IR laser
- Very good S/N with sensor response
  - **Observed AC-LGAD charge sharing**



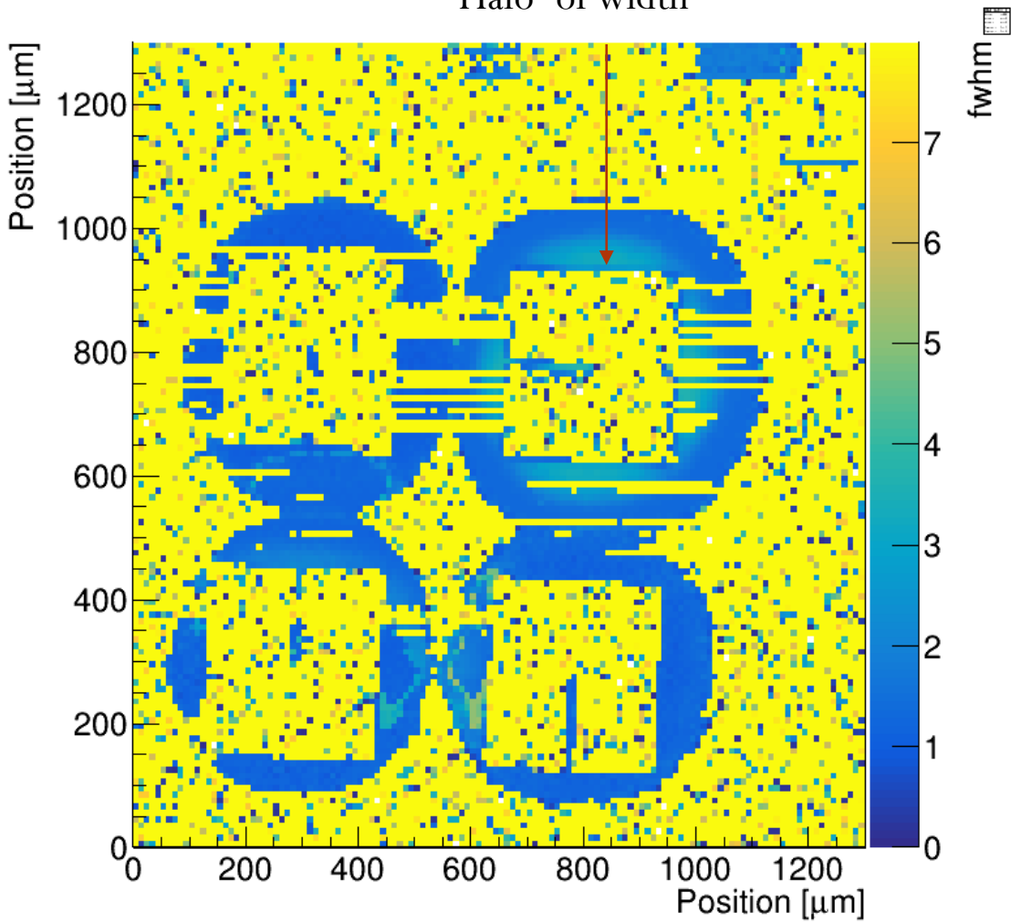


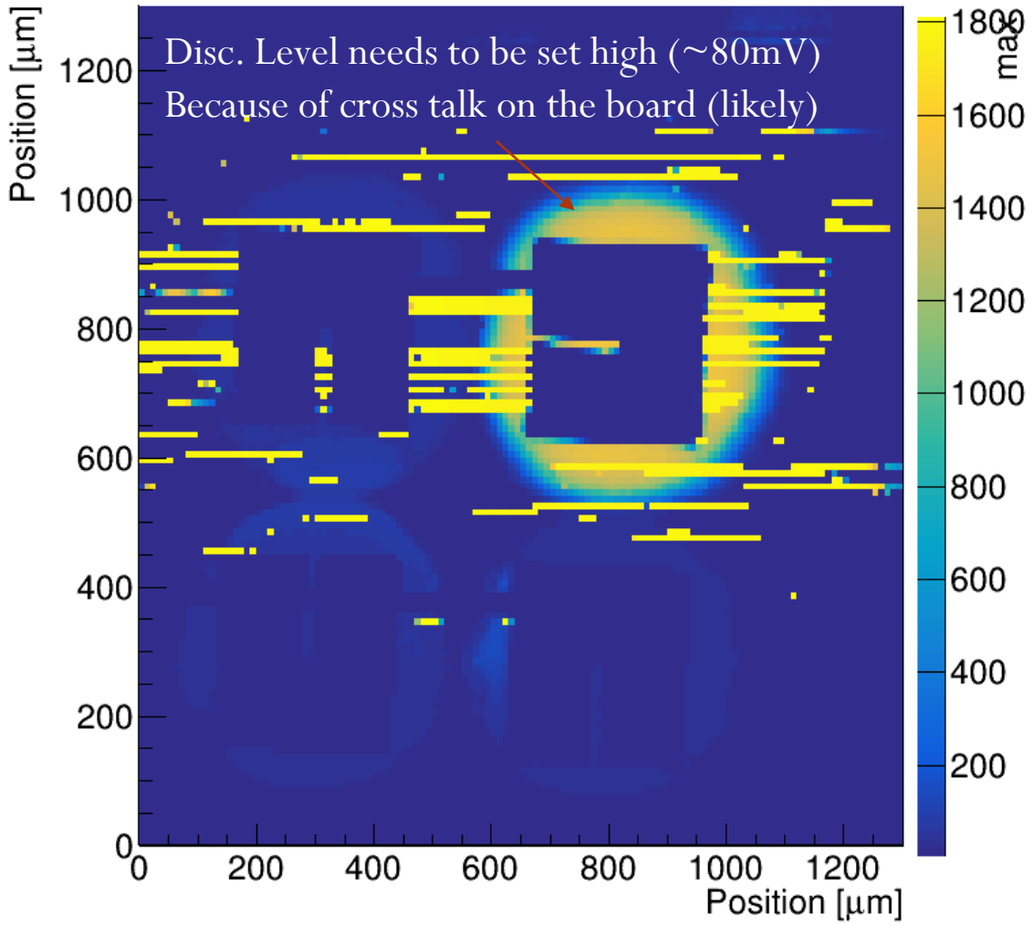
Sensor pre-amp TCT scan



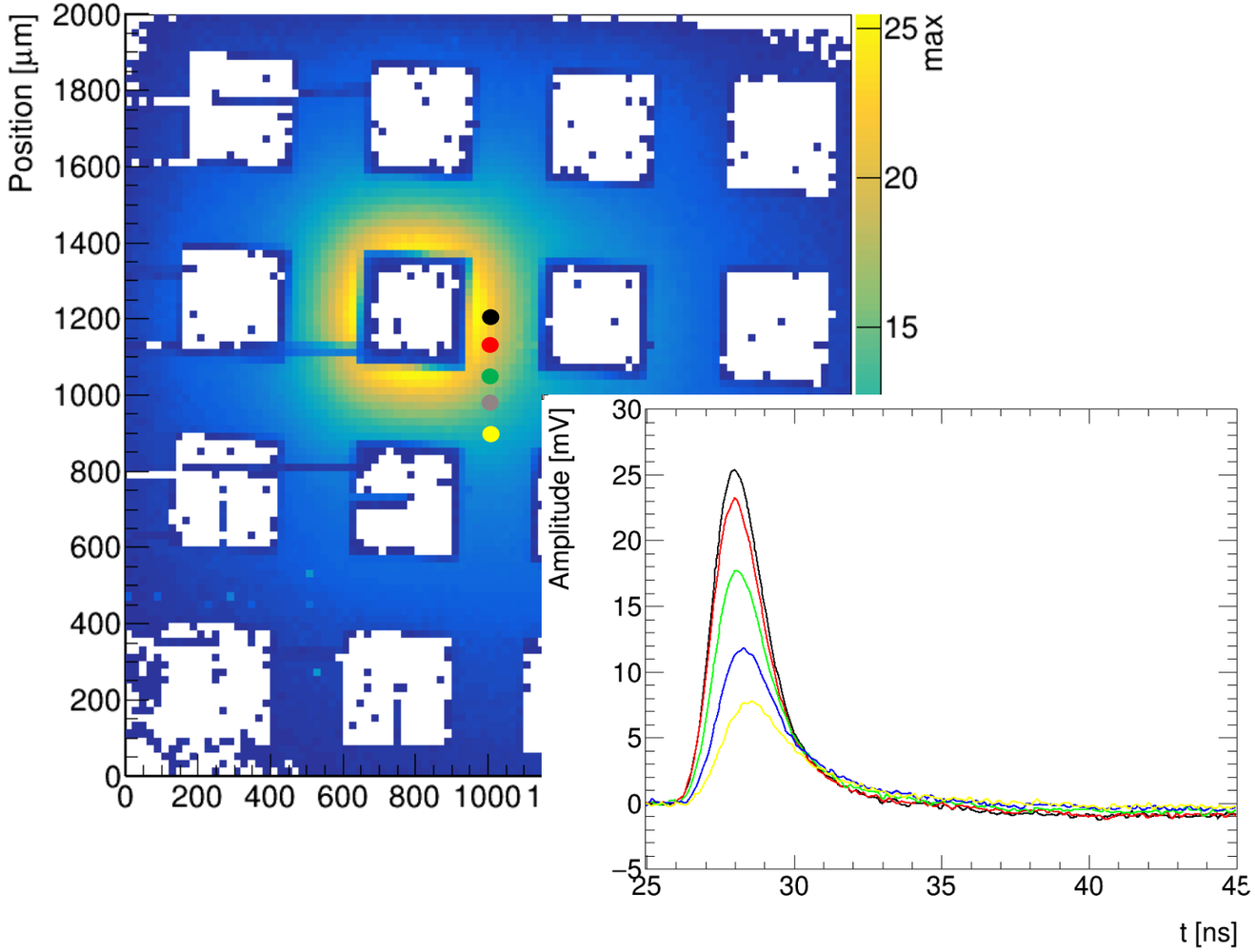


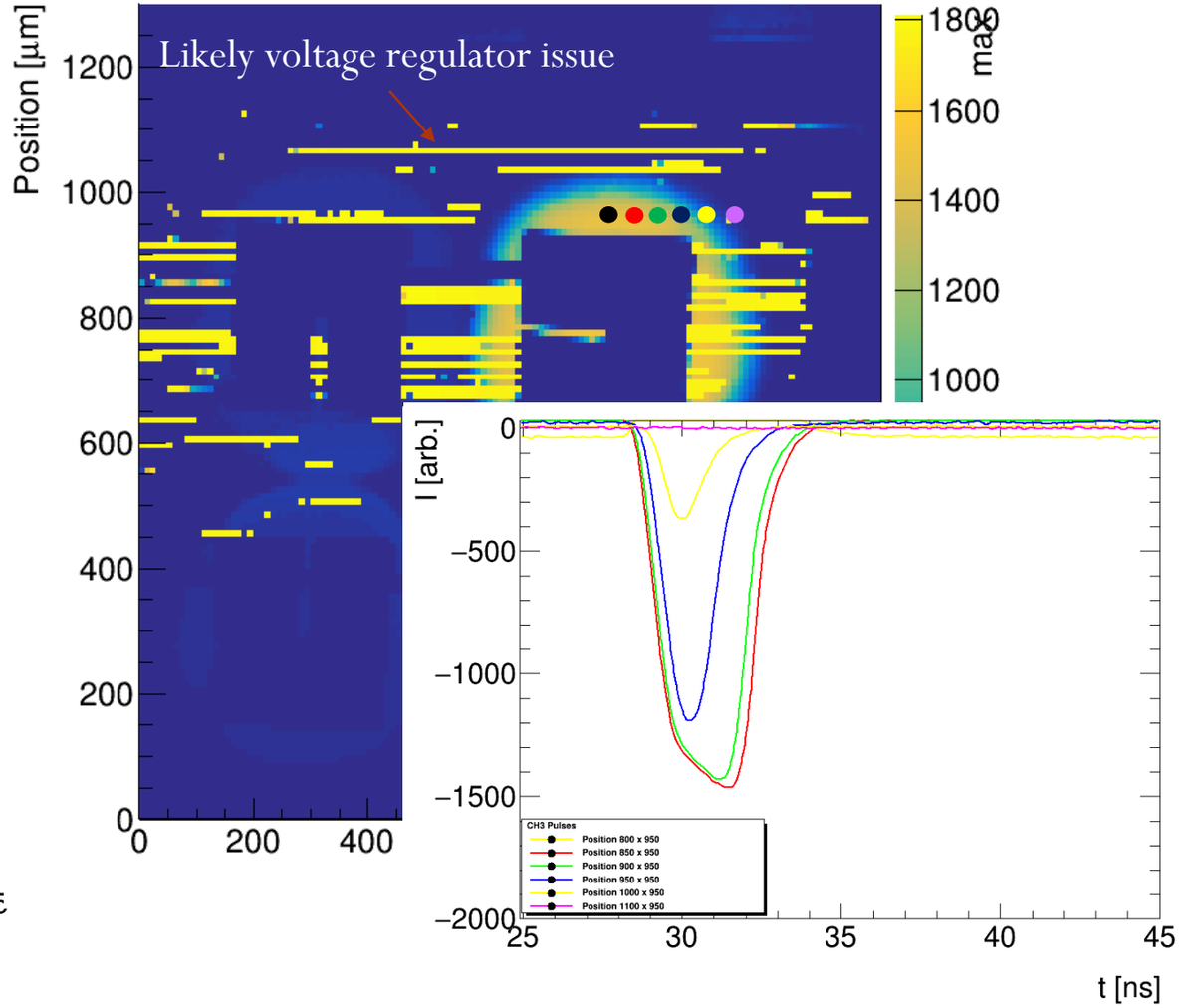
Sensor discriminator output (laser TCT scan)





Laser TCT scan – pre-amp vs discriminator





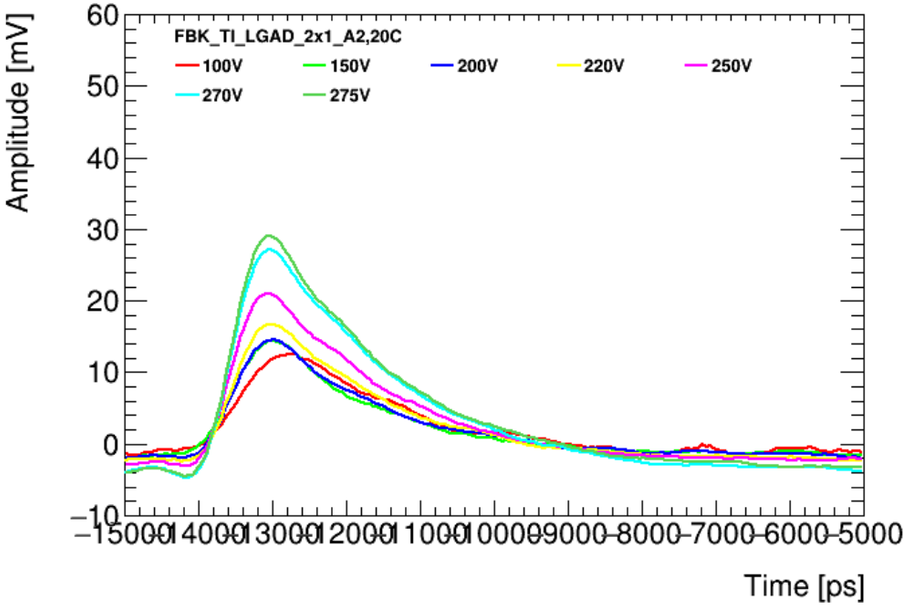
Next steps

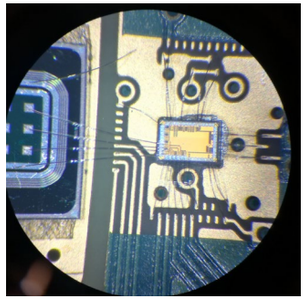
- Test the chip with a higher capacitance sensor (several pF)
  - Test with 1cm long strips (20um and 50um) from HPK and BNL
  - Chip noise is very dependent on input capacitance, can be used to estimated the "effective" input capacitance of sensors (CVs have large frequency dependence)
- Estimate the power consumption
  - We tried a few methods to estimate current draw but results are not consistent with expectation (power consumption is too low)
- New board loaded with MP chip
  - Issue with one component, replacement arrived yesterday
  - MP chip should drain more power but have better performance (better rise time and gain)
- Presenting at TWEPP next week: https://indico.cern.ch/event/1255624/contributions/5445271/

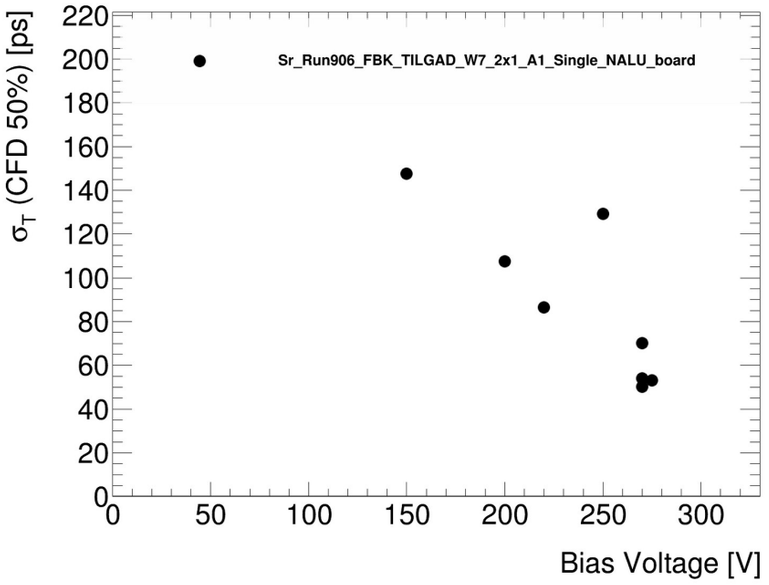
HP-SoC status

HP-SoC v1 (last year)

- First version (2022) had good power consumption and pulse rise time
- Issues:
  - low amplifier gain and issues with digital readout
- Jitter goal was <10ps, observed was >30 ps
  - Results with 50um sensor showed 50ps time resolution
- New version with improved performance is ready!

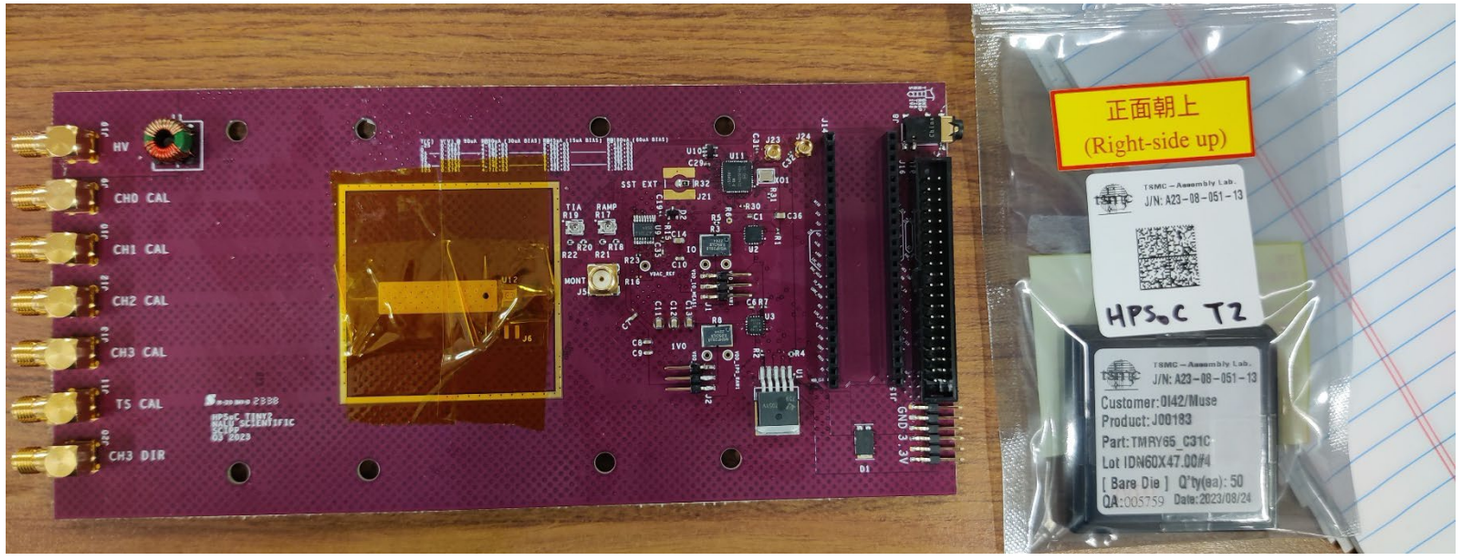






HP-SoC v2

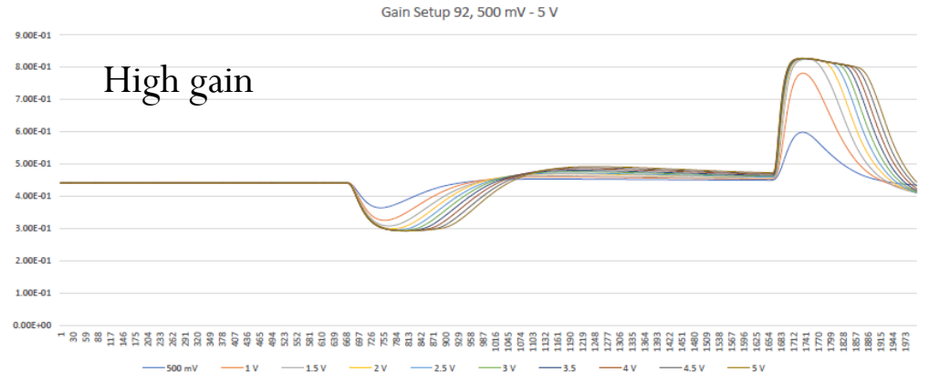
- New HP-SoC version and readout board arrived a SCIPP yesterday
  - 4 channels total with TiA + digital output
  - 1 ch TIA amplifier readout to check pulse
  - Expected working digital communication (via FPGA)
- Not enough time even for a brief look, but expect updates in the next meeting or via email

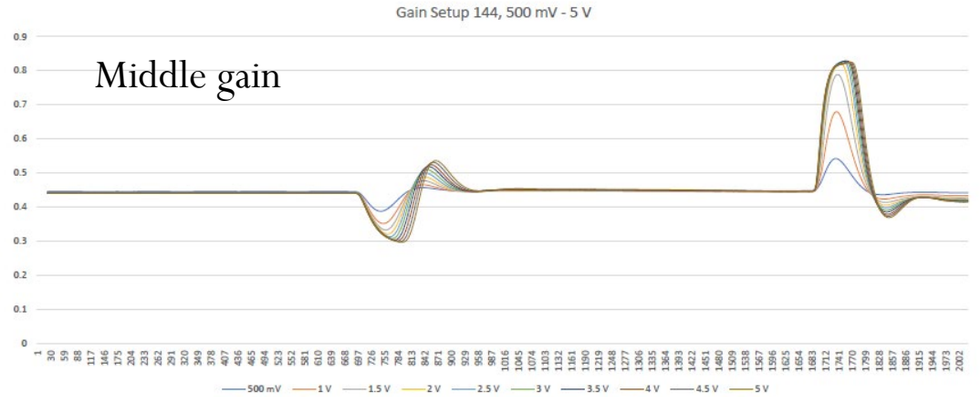


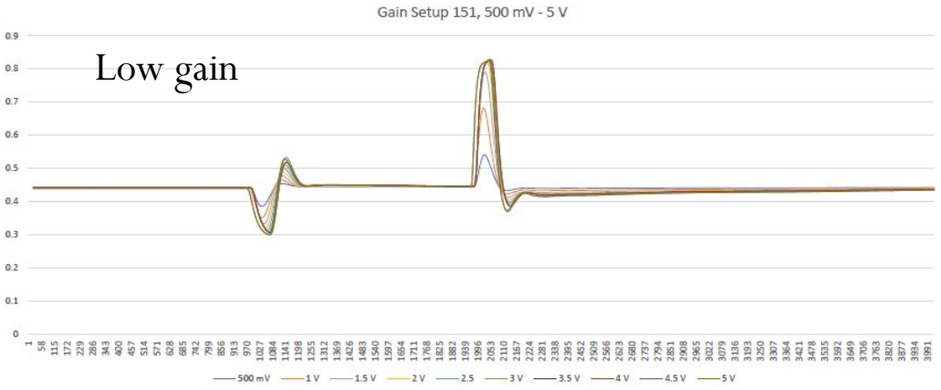
FAST2/3 status

FAST chip activities

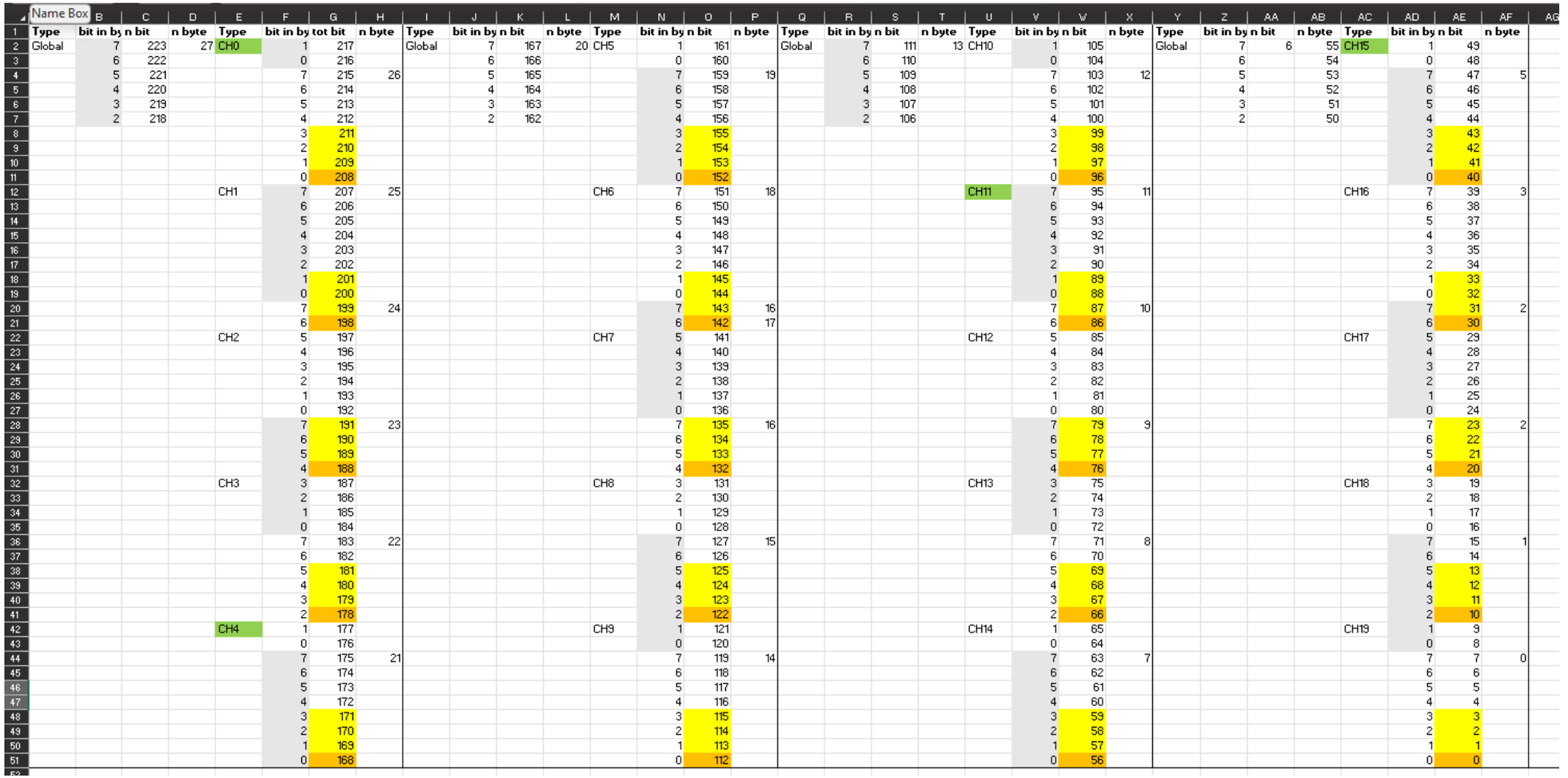
- In the past months we probed the adjustable gain capabilities of FAST2
- Tested the three gain setting
  - Actually 8 gain settings but only 3 main ones
- Gain can be adjusted channel by channel
  - Issues with shift registry mapping that took a long time to resolve
  - Provided documentation not accurate, partial byte shifts







FAST2 shift registry map



	Type	bit in by	n bit	n byte	Type	bit in by	tot bit	n byte	Type	bit in by	n bit	n byte	Type	bit in by	n bit	n byte	Type	bit in by	n bit	n byte	Type	bit in by	n bit	n byte	Type	bit in by	n bit	n byte	Type	bit in by	n bit	n byte
1	Type	bit in by	n bit	n byte	Type	bit in by	tot bit	n byte	Type	bit in by	n bit	n byte	Type	bit in by	n bit	n byte	Type	bit in by	n bit	n byte	Type	bit in by	n bit	n byte	Type	bit in by	n bit	n byte	Type	bit in by	n bit	n byte
2	Global	7	223	27	CH0	1	217		Global	7	167	20	CH5	1	161		Global	7	111	13	CH10	1	105		Global	7	6	55	CH15	1	49		
3		6	222			0	216			6	166			0	160			6	110			0	104			6		54		0	48		
4		5	221			7	215	26		5	165			7	159	19		5	109			7	103	12		5		53		7	47	5	
5		4	220			6	214			4	164			6	158			4	108			6	102			4		52		6	46		
6		3	219			5	213			3	163			5	157			3	107			5	101			3		51		5	45		
7		2	218			4	212			2	162			4	156			2	106			4	100			2		50		4	44		
8						3	211							3	155							3	99							3	43		
9						2	210							2	154							2	98							2	42		
10						1	209							1	153							1	97							1	41		
11						0	208							0	152							0	96							0	40		
12					CH1	7	207	25					CH6	7	151	18					CH11	7	95	11					CH16	7	39	3	
13						6	206							6	150							6	94							6	38		
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37						6	182							6	126							6	70							6	14		
38						5	181							5	125							5	69							5	13		
39						4	180							4	124							4	68							4	12		
40						3	179							3	123							3	67							3	11		
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42					CH4	1	177						CH9	1	121						CH14	1	65					CH19	1	9		
43						0	176							0	120							0	64							0	8		
44						7	175	21						7	119	14						7	63	7						7	7	0	
45						6	174							6	118							6	62							6	6		
46						5	173							5	117							5	61							5	5		
47						4	172							4	116							4	60							4	4		
48						3	171							3	115							3	59							3	3		
49						2	170							2	114							2	58							2	2		
50						1	169							1	113							1	57							1	1		
51						0	168							0	112							0	56							0	0		

FAST3 chip

- FAST3 chip arrived
- Improved front end and buffers
- Better dynamic range

- Available soon!
- As soon as we get it we'll start testing and report

Conclusions

AS-ROC

- SiGe chip is ready and being tested!
- **Very good performance for first prototype:** low noise as expected
- Low power version tested, more power version should have better performance
- **Discriminator output is good**
- Tested with AC-LGAD pad sensor with input capacitance <1pF
  - Good results for both amplifier output and discriminator
  - Test with several pF sensor next (AC-LGAD strips)

HD-SOC

- New iteration of the chip received with readout board received yesterday
- 4 ch TiA+Digital, 1 ch with TiA output
- Applying to JLab funding for continuation of the project

FAST

- Digital part and mapping understood for FAST2
- FAST3 chip is ready, available for testing in a few weeks