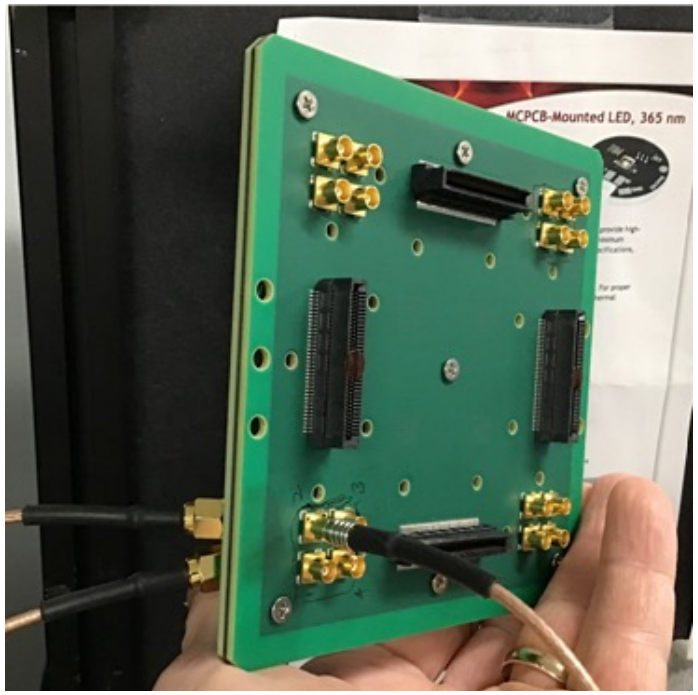
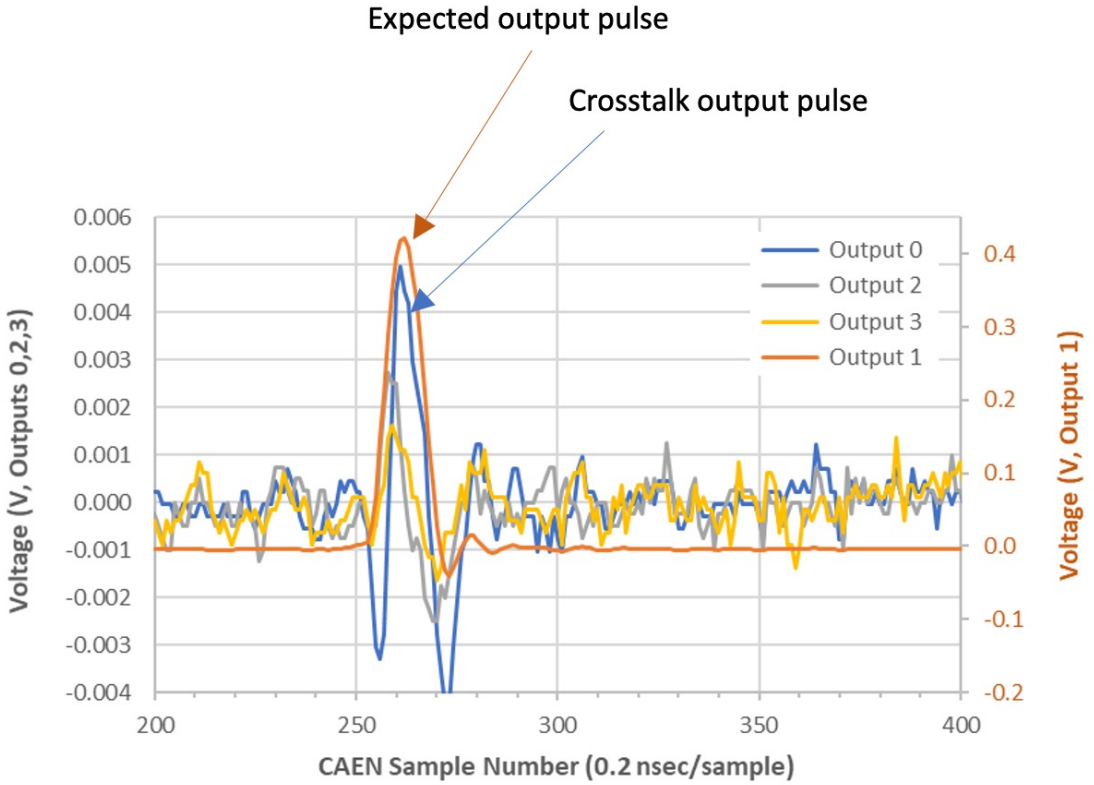
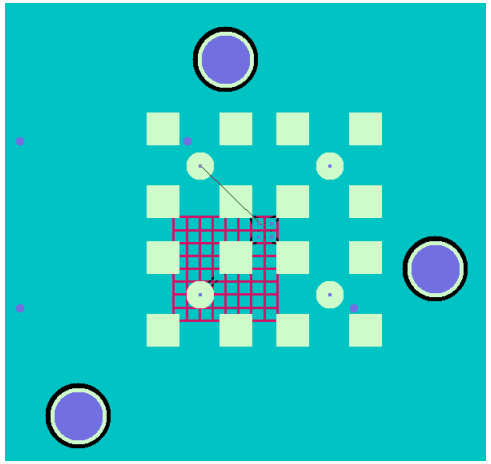
Interposer interface cross-check at Incom



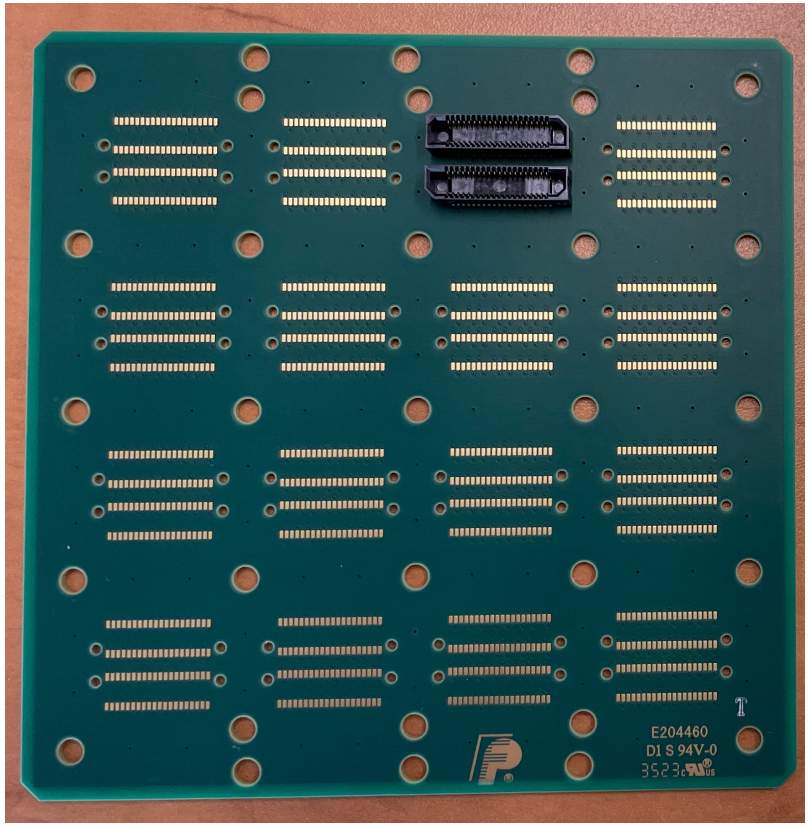


Two boards bolted together back-to-back via a stock Samtec interposer

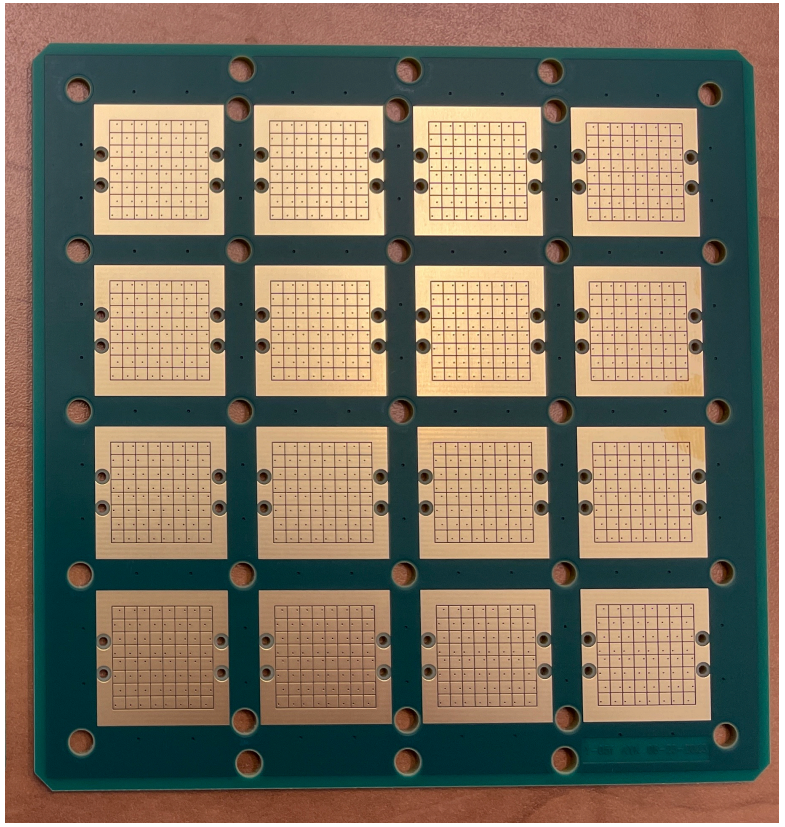
- A 2x2 pad area on an older board was used for this exercise (Y05a)
- Observations:
  - Signal transmission via “5mm trace -> interposer -> 5mm trace” (and a pair of RG-316 cables) ~98%
  - Cross-talk on a neighboring pad <2%



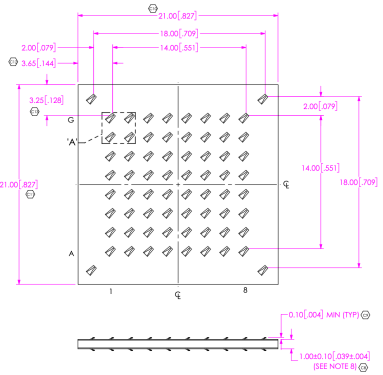
A dummy HRPPD readout board Y05f



top side (32x Samtec ERF8 connectors)

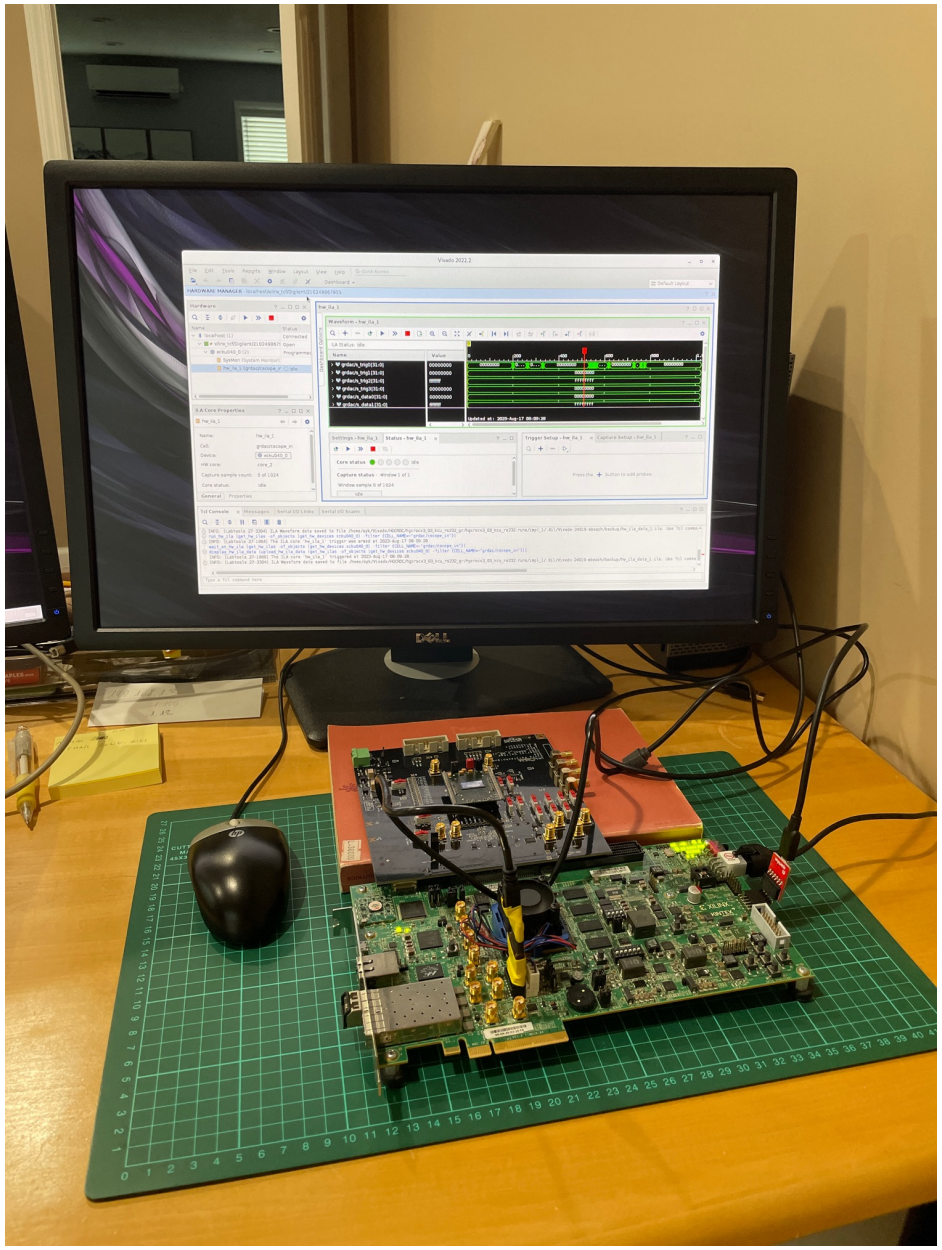


bottom side (matches HRPPD rear side)

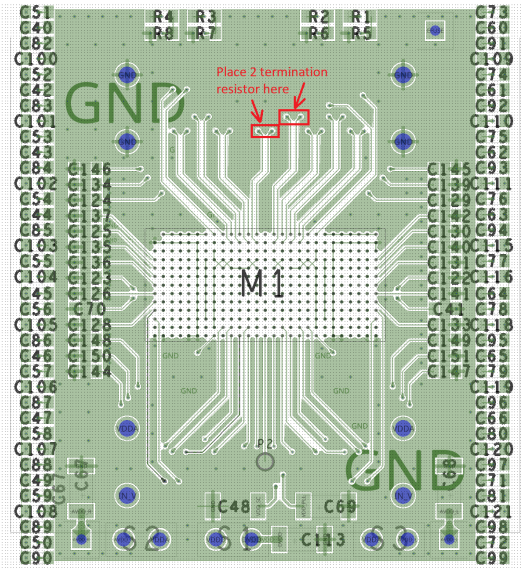


- Assembly order for 5 boards is being placed
- Connectivity for any of the sixteen 8x8 pad fields (got a quote already):
  - A set of [2x Samtec ERM8 -> MMCX] adapters, 32ch (4x8) connected at a time
  - A set of ERM8-based grounding caps for all other 8x8 fields

Test stand at Brookhaven



- A small HGCROC3 installation at BNL
  - Essentially a Linux-based copy of Oak Ridge setup
    - KCU105 FPGA kit provided by John Kuczewski (BNL)
    - Carrier board by Norbert Novitzky (ORNL)
    - HGCROC3 mezzanine board by Damien Thienpont (IN2P3)
    - FPGA firmware by Miklos Zeller (Debrecen)
  - Should be sufficient for writing an RCDAQ driver
    - First via USB, then gigabit ethernet
  - Not really functional as of yet
    - Issues with on-board termination
    - A fix by Miklos was a partial success story
  - Where do we go from here:
    - AK meets with Norbert in the US?
    - AK comes to Orsay mid October?



A situation with FY24 funding

- ASIC interface development was originally split between two *R&D* proposals:
  - eRD110 (photosensors): pilot version and a single full set ($10k)
  - eRD114 (pfRICH prototype): four more sets ($25k)
  - Money gets dispatched via BNL (easy way)

This did not really fly

- Present status: everything is packed into eRD114 proposal

Five 3D printed HRPPD enclosures	$2k
120 HGCROC3 ASIC chips	$12k
Five readout backplane assemblies	$16k
Two KCU105 evaluation kits	$8k
Beam test travel	$35k
Total	**$73k**

This does not seem to fly either

- Next iteration: a consolidated *PED* funding request for the same grand total of ~$35k?
  - Money gets dispatched via JLAB (a “less easy” way)

Timeline-wise boundary conditions

- pfRICH beam test in June 2024 (all five ASIC / FPGA board sets + DAQ interface)
  - Obviously, all this needs to be available several months earlier
    - Call it March 2024 the latest?

- HRPPD routine evaluation in the lab (first BNL, then Yale, then INFN, Argonne & Glasgow)
  - If it starts past June 2024, this is probably fine