

AC-LGAD Workfest Report

Satoshi Yano (Hiroshima University)

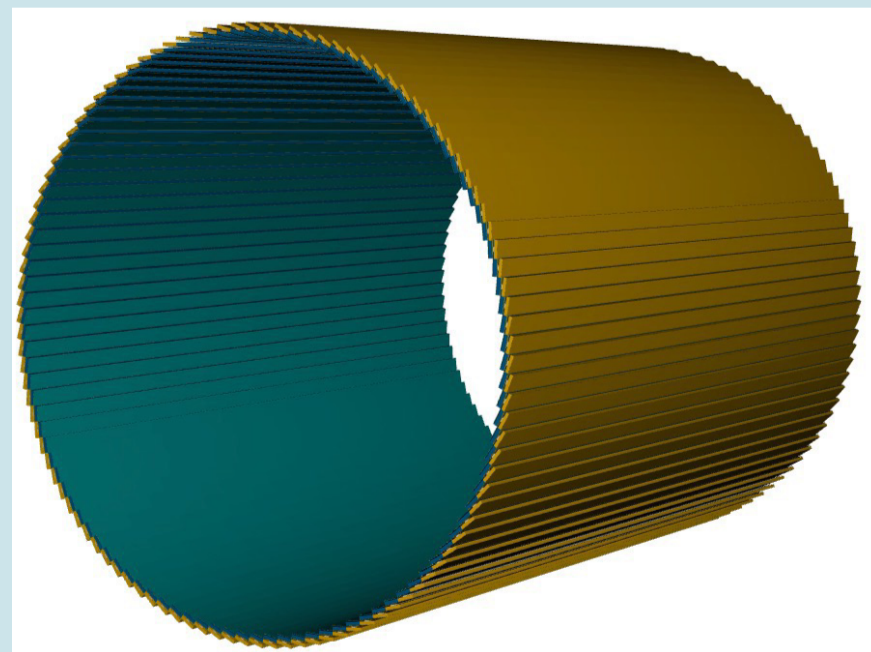
ePIC Collaboration meeting @ Lehigh University

07/27/2024

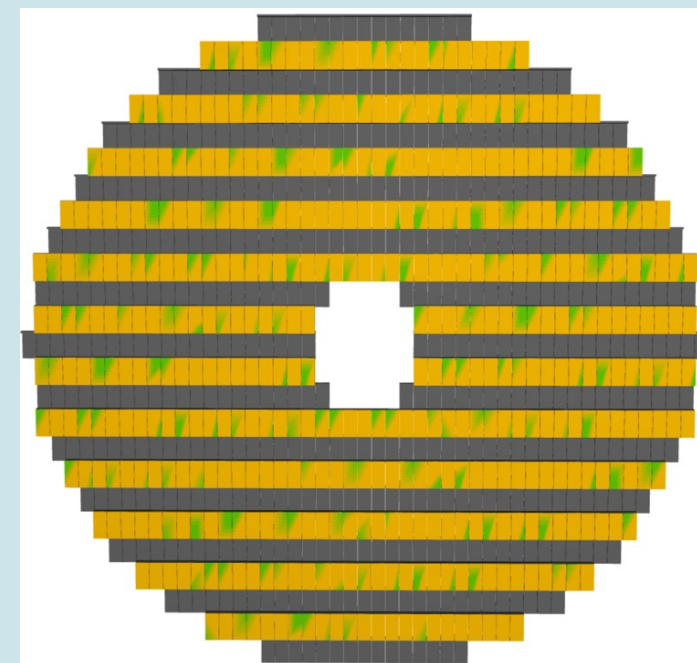
Overview

- Description: Discussion and coordination of detectors using AC-LGAD sensor, BTOF, FTOF, and FF detectors

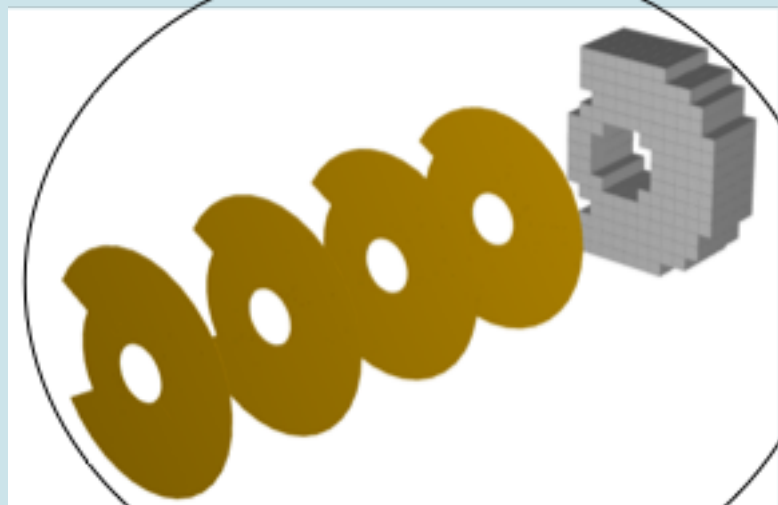
BTOF



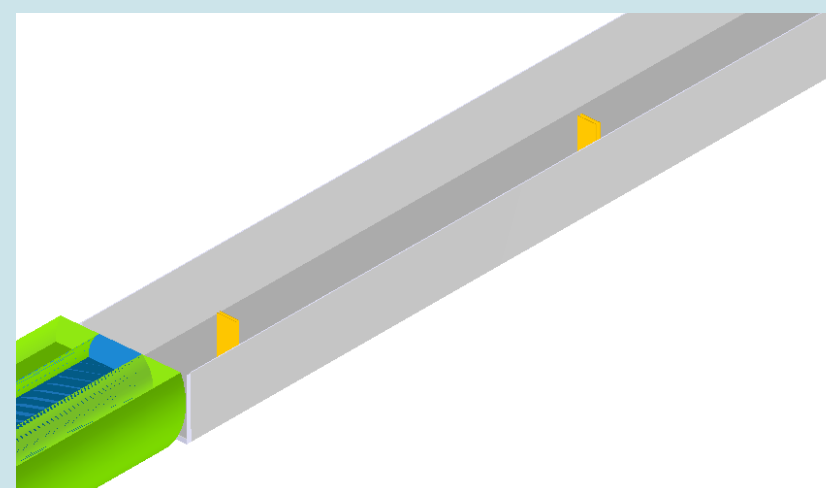
FTOF



B0



OMD



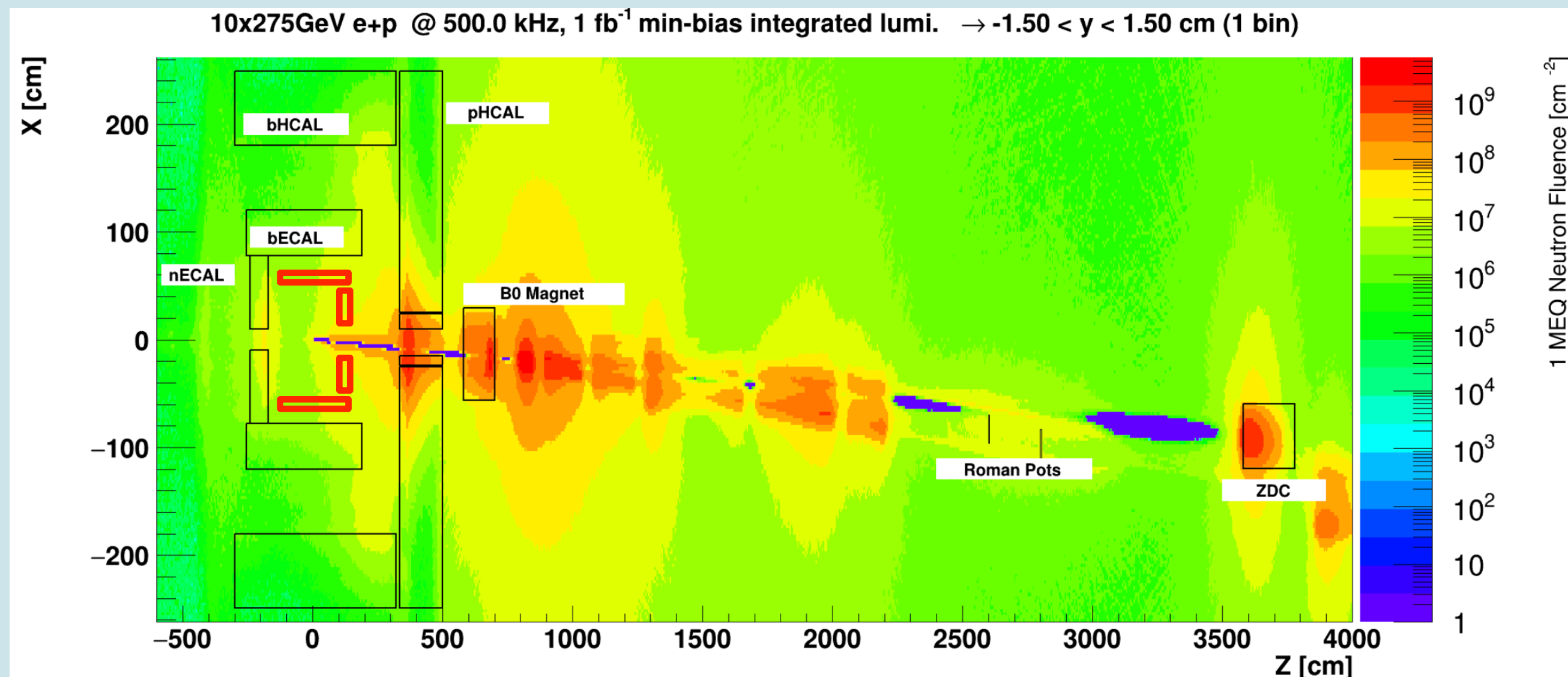
Roman Pots



	Print	PDF	Full screen	Detailed view	Filter
13:00	Introduction				Zhangbu Xu 🔗
	Rm 85, Rauch Business Center				13:00 - 13:10
	Barrel TOF				Satoshi Yano 🔗
	Rm 85, Rauch Business Center				13:10 - 13:25
	Forward TOF				Prof. Wei Li 🔗
	Rm 85, Rauch Business Center				13:25 - 13:40
	FF AC-LGAD detectors				Alexander Jentsch 🔗
	Rm 85, Rauch Business Center				13:40 - 14:05
14:00	Luminosity Tracker				
	Rm 85, Rauch Business Center				14:05 - 14:06
	eRD112				Alexander Jentsch et al. 🔗
	Rm 85, Rauch Business Center				14:20 - 14:45
	Coffee Break				
15:00	Rm 85, Rauch Business Center				14:45 - 15:15
	FCFD				Artur Apresyan et al. 🔗
	Rm 85, Rauch Business Center				15:15 - 15:30
	EICROC				Christophe de la Taille 🔗
	Rm 85, Rauch Business Center				15:30 - 15:45
	Electronics				Prof. Wei Li 🔗
16:00	Rm 85, Rauch Business Center				15:45 - 16:05
	Support structure & PCB & Cooling				Oskar Hartbrich 🔗
	Rm 85, Rauch Business Center				16:05 - 16:25
	Digitization				Prithwish Tribedy 🔗
	Rm 85, Rauch Business Center				16:25 - 16:45
	Discussion				
17:00	Rm 85, Rauch Business Center				16:45 - 17:05

Requirements for AC-LGAD

	Area (m ²)	channel size (mm ²)	# of channels	Timing reso.	Spatial reso.	Material budget
BTOF	12	0.5x10	2.4M	35 ps	30 μm in r·φ	0.01 X ₀
FTOF	1.4	0.5x0.5	5.6M	25 ps	30 μm in x·y	0.025 X ₀
B0	0.07	0.5x0.5	0.28M	30 ps	20 μm in x·y	0.05 X ₀
RPs/OMD	0.14/0.08	0.5x0.5	0.56M/0.32M	30 ps	140 μm in x·y	no strict req.



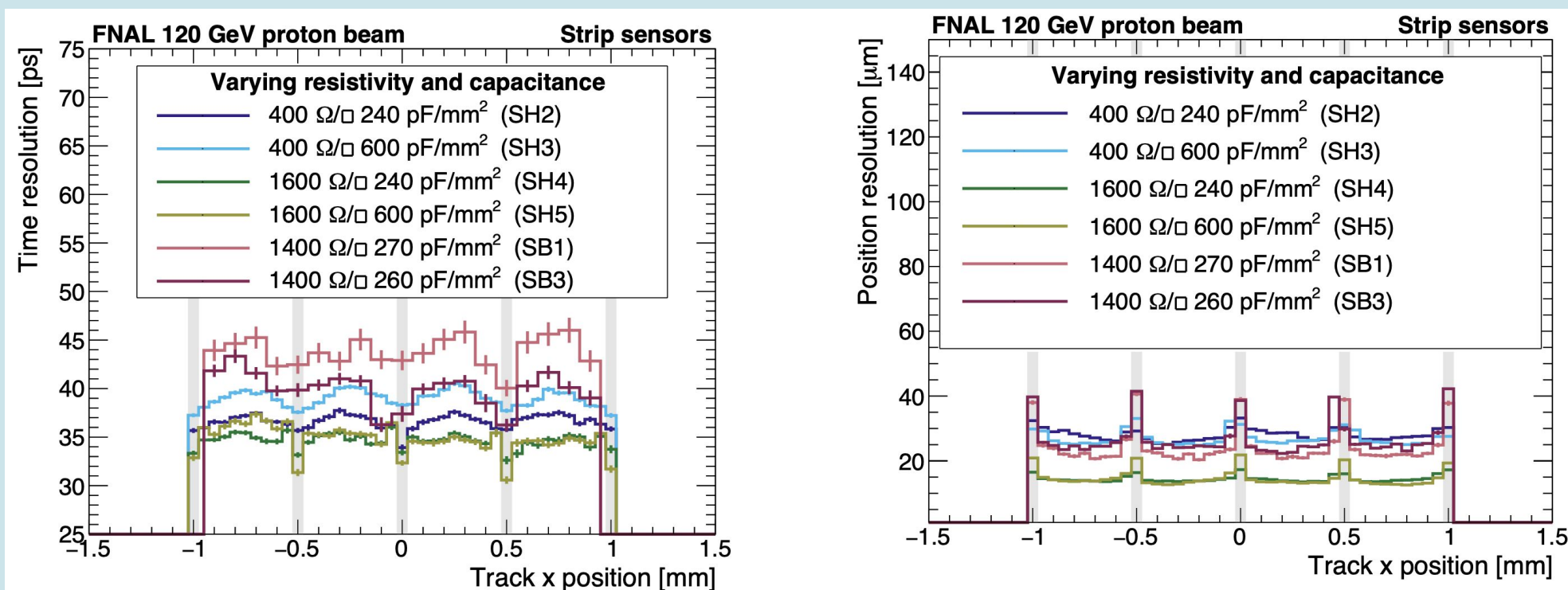
- BTOF uses strip-type and FTOF/FF use pixel-type sensors
- Cooling strategy and support structure of FF is different from BTOF/FTOF due to spatial limitation
- Doses are ~1e2 smaller than LHC levels for the ePIC environment

https://wiki.bnl.gov/EPIC/index.php?title=Radiation_Doses

AC-LGAD performance

- eRD112 presented FY24 report and FY25 plan
- Previous test beam campaign has been finalized
 - Timing resolution of 35 ~ 45 ps, and spatial resolution of 15 ~ 30 μm are achieved by BNL and HPK prototypes
 - The results are under control and the next prototype will be improved

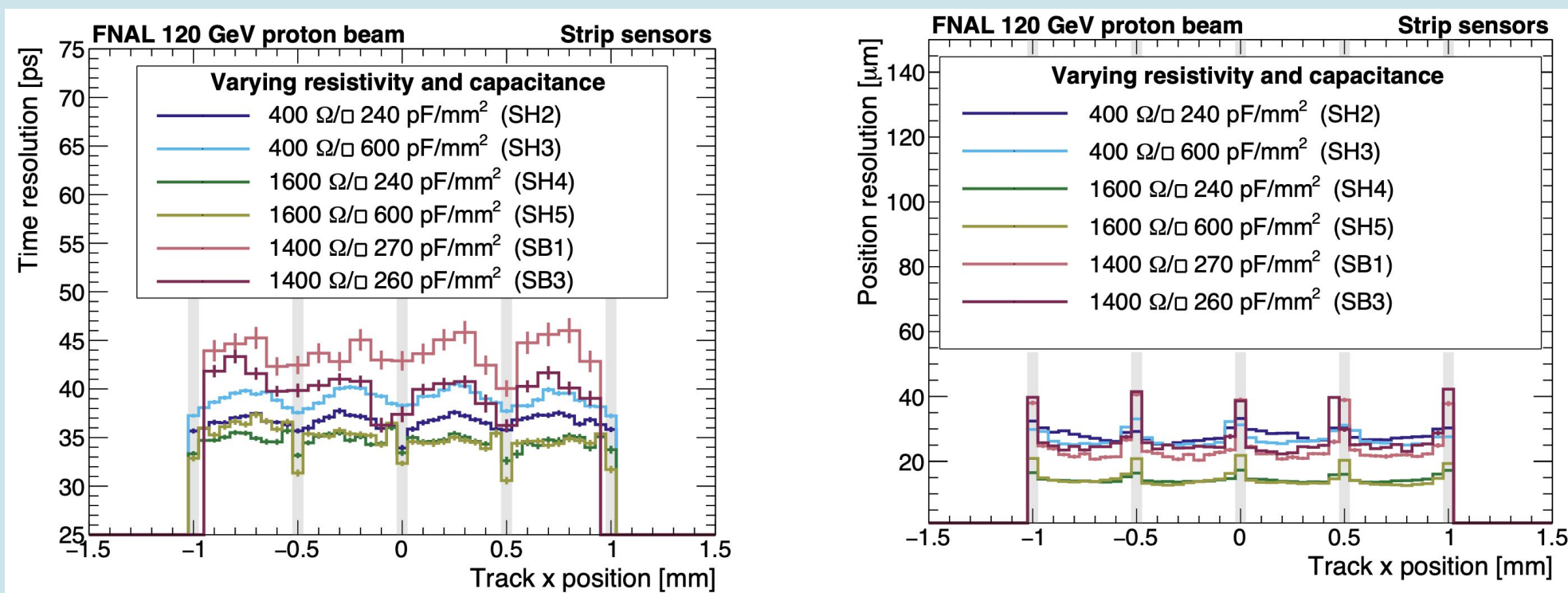
Beam test @ FNAL results



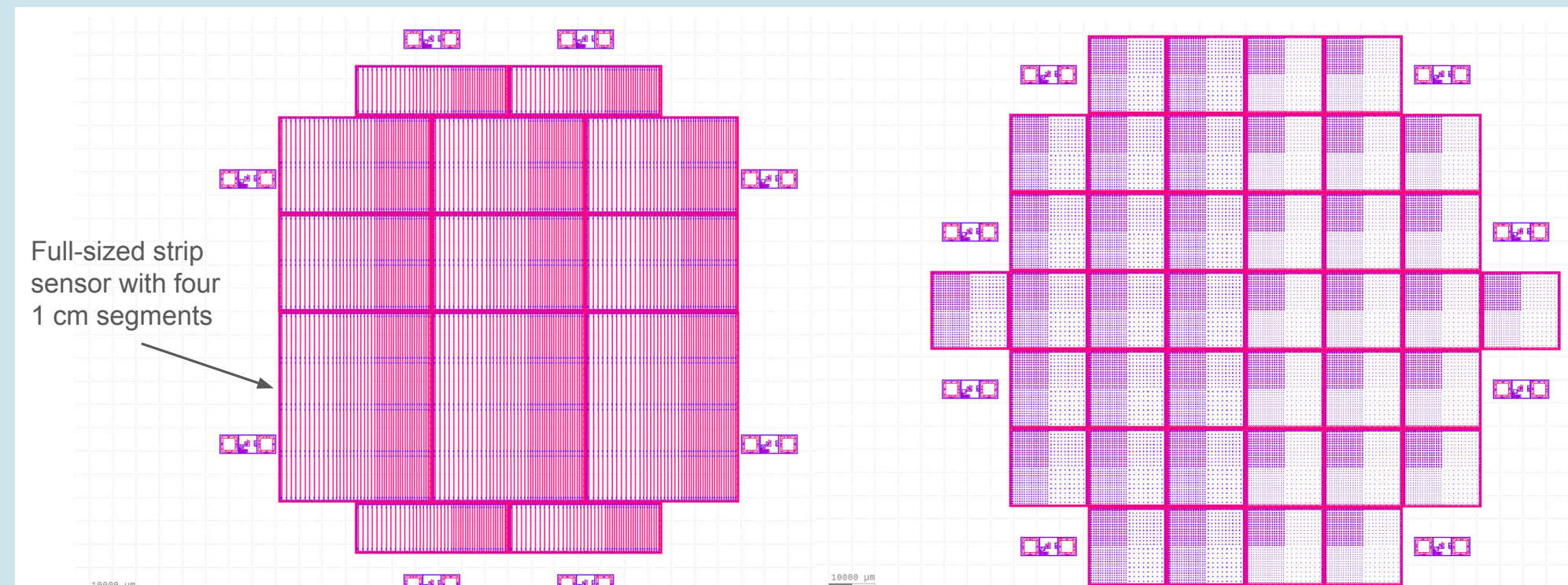
AC-LGAD performance

- eRD112 presented FY24 report and FY25 plan
- Previous test beam campaign has been finalized
 - Timing resolution of 35 ~ 45 ps, and spatial resolution of 15 ~ 30 μm are achieved by BNL and HPK prototypes
 - The results are under control and the next prototype will be improved
- Next prototype will include full-size sensors by HPK and we will receive strip-type sensors in a few months

Beam test @ FNAL results



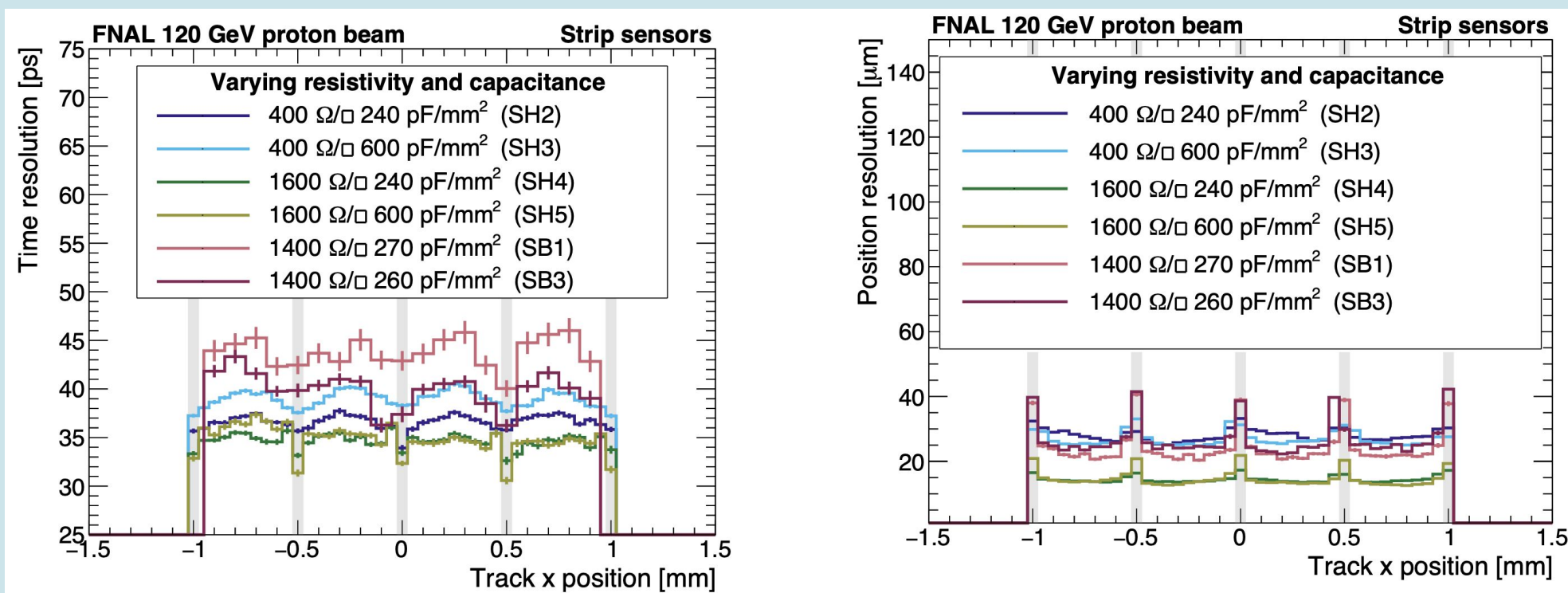
Next prototype scheme



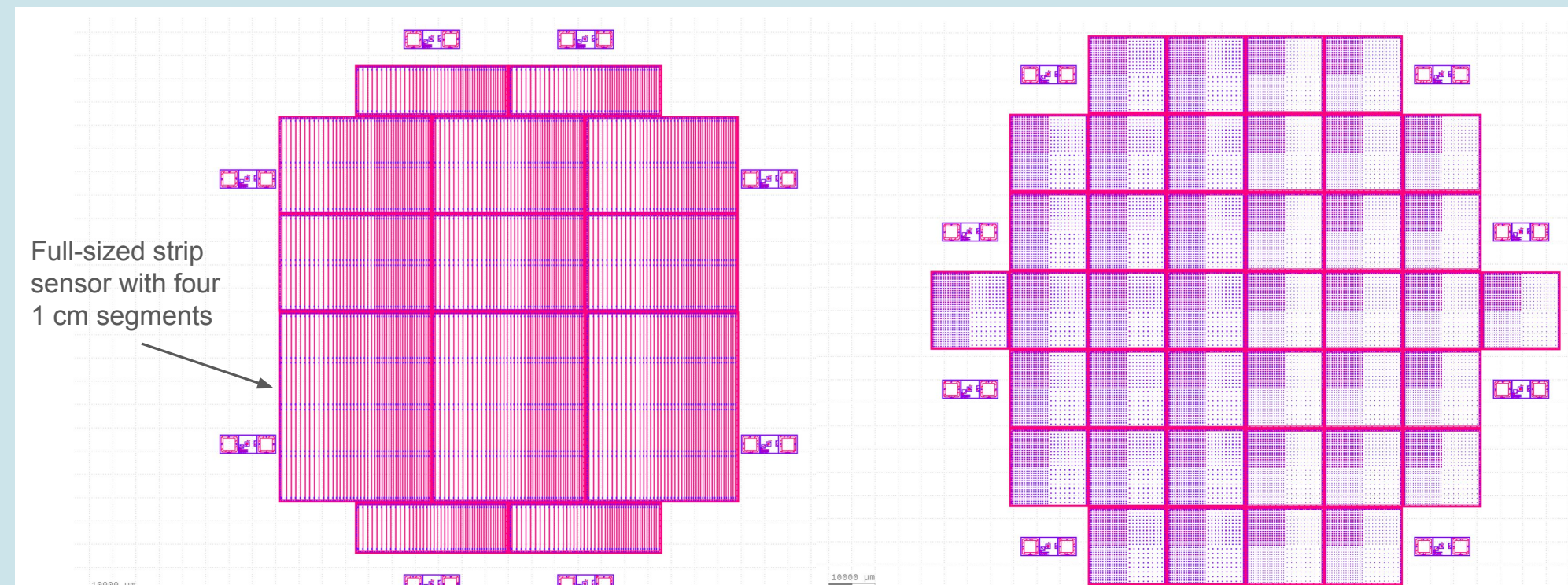
AC-LGAD performance

- eRD112 presented FY24 report and FY25 plan
- Previous test beam campaign has been finalized
 - Timing resolution of 35 ~ 45 ps, and spatial resolution of 15 ~ 30 μm are achieved by BNL and HPK prototypes
 - The results are under control and the next prototype will be improved
- Next prototype will include full-size sensors by HPK and we will receive strip-type sensors in a few months
- Readout board from SCIPP will be used to characterization these sensors

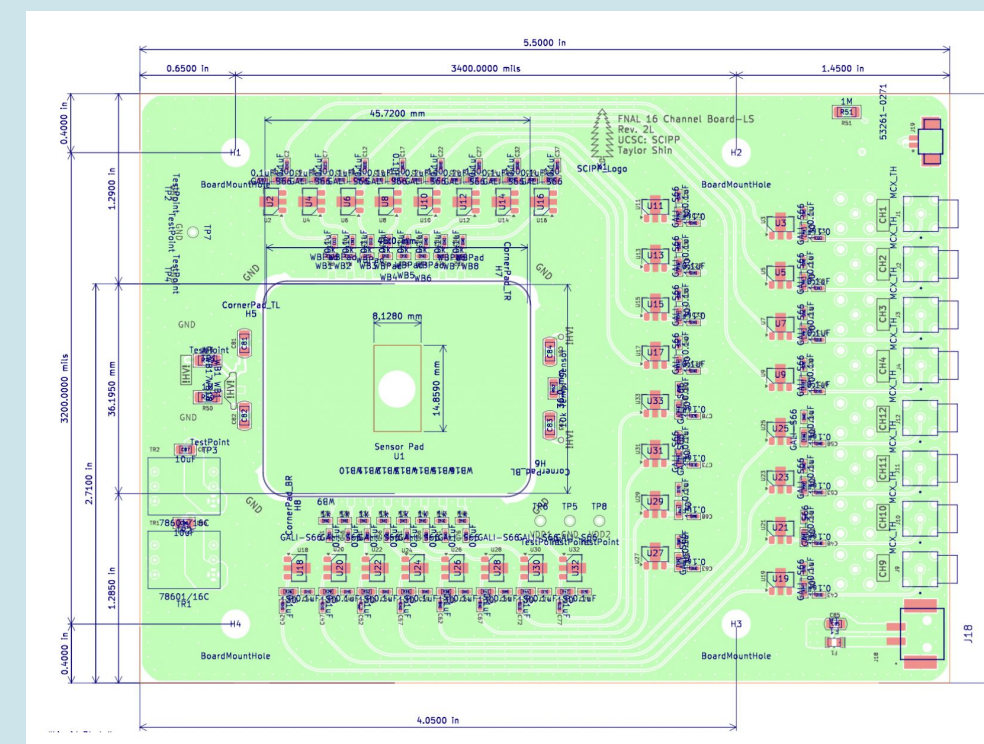
Beam test @ FNAL results



Next prototype scheme



SCIPP RDO blueprint



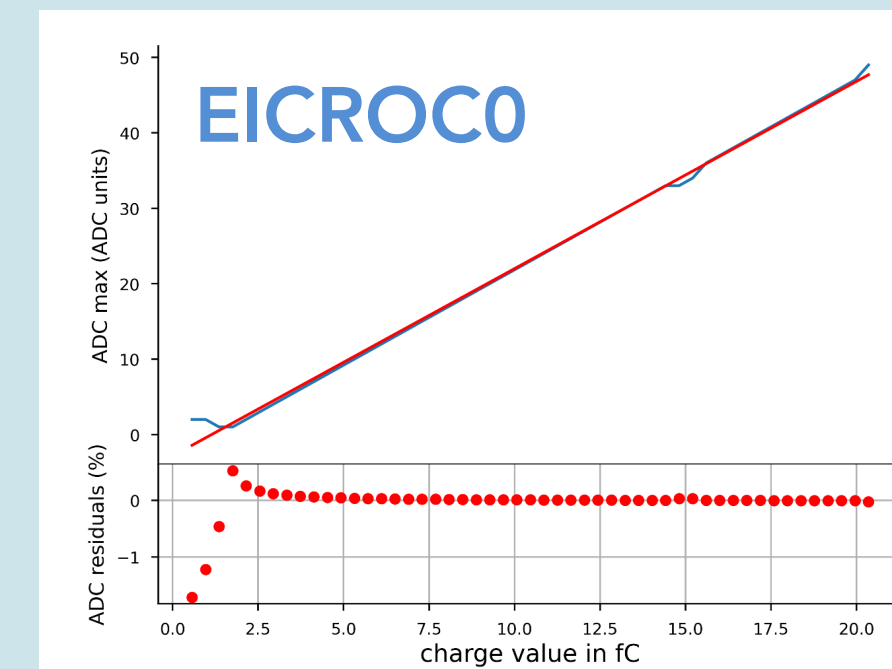
ASIC performance

- EICROC has been designed to be used for the pixel-type sensor readout
 - EICROC0 is available with 4x4 geometry

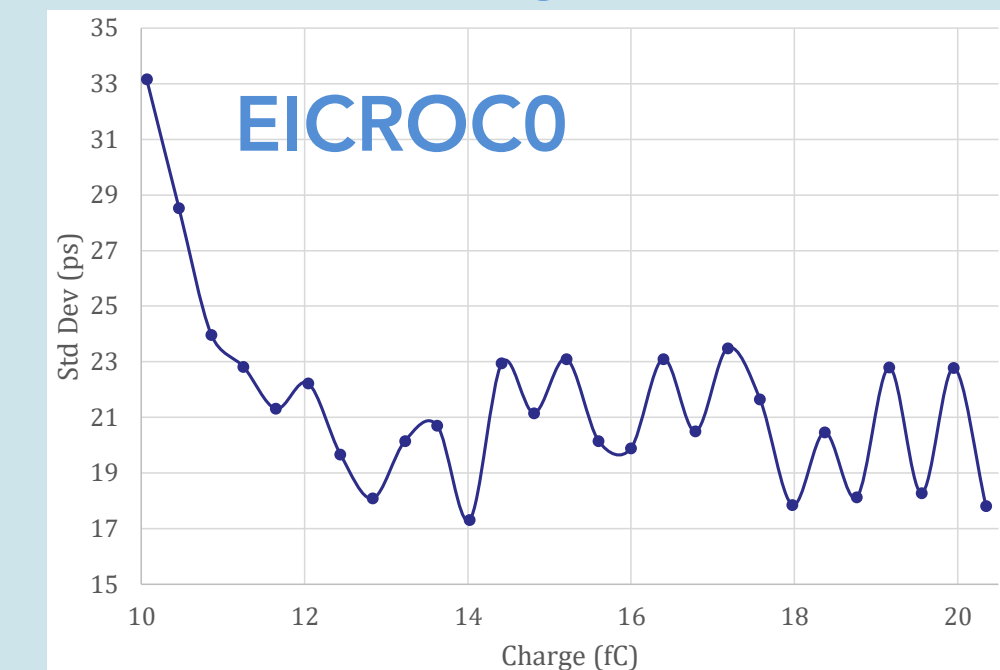
ASIC performance

- EICROC has been designed to be used for the pixel-type sensor readout
 - EICROC0 is available with 4x4 geometry
- Digital block of ADC and TDC results were shown
 - The significant jitter issue by the clock delay block on the FPGA has been fixed this June
 - Linear trend in injected charge and ADC has been observed
 - TDC jitter of 33 (17.5) ps and 20 (12.5) ps at 10 fC and 20 fC w/ (w/o) sensor have been observed

Charge v.s. ADC



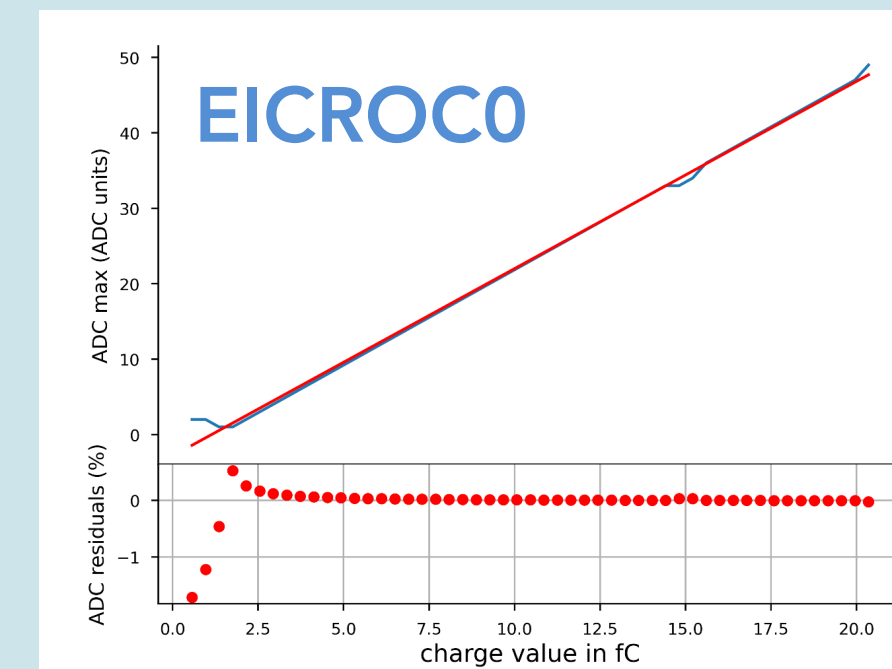
TDC jitter



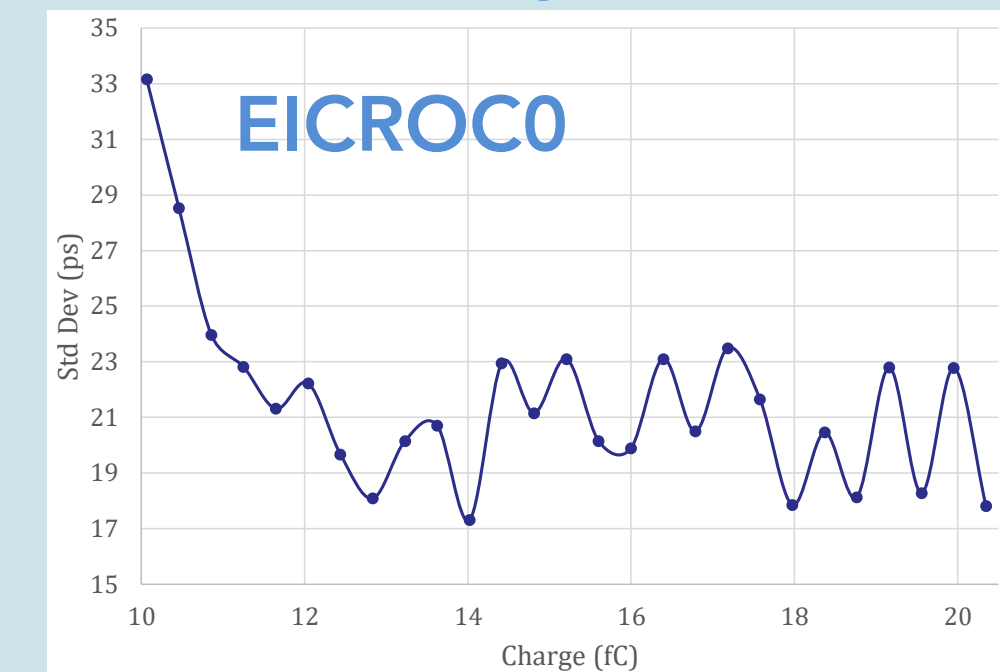
ASIC performance

- EICROC has been designed to be used for the pixel-type sensor readout
 - EICROC0 is available with 4x4 geometry
- Digital block of ADC and TDC results were shown
 - The significant jitter issue by the clock delay block on the FPGA has been fixed this June
 - Linear trend in injected charge and ADC has been observed
 - TDC jitter of 33 (17.5) ps and 20 (12.5) ps at 10 fC and 20 fC w/ (w/o) sensor have been observed
- EICROC1 will address a larger demonstration 4x16 or 8x16 or 4x32 or 8x32
 - Submission @ the end of 2024

Charge v.s. ADC



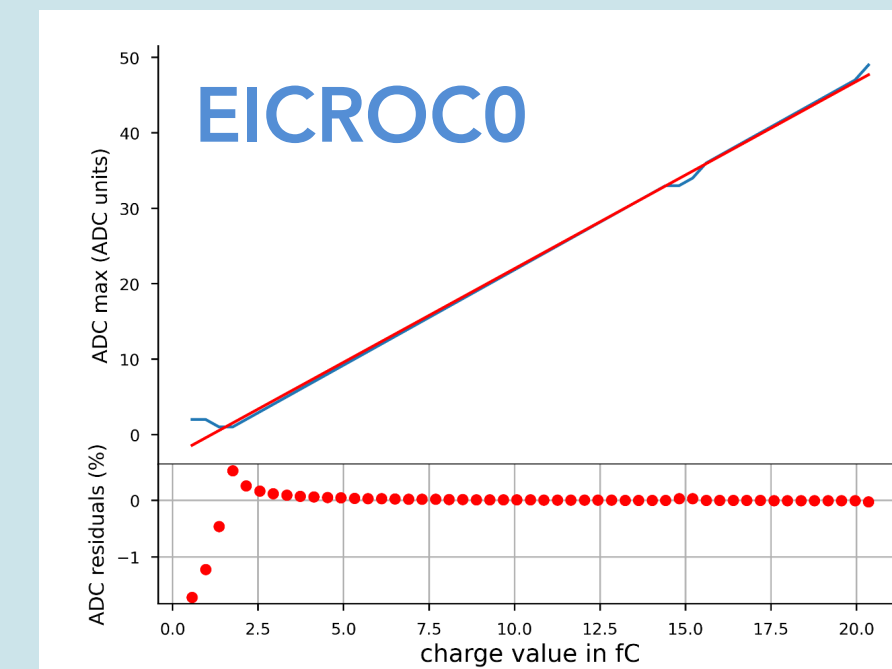
TDC jitter



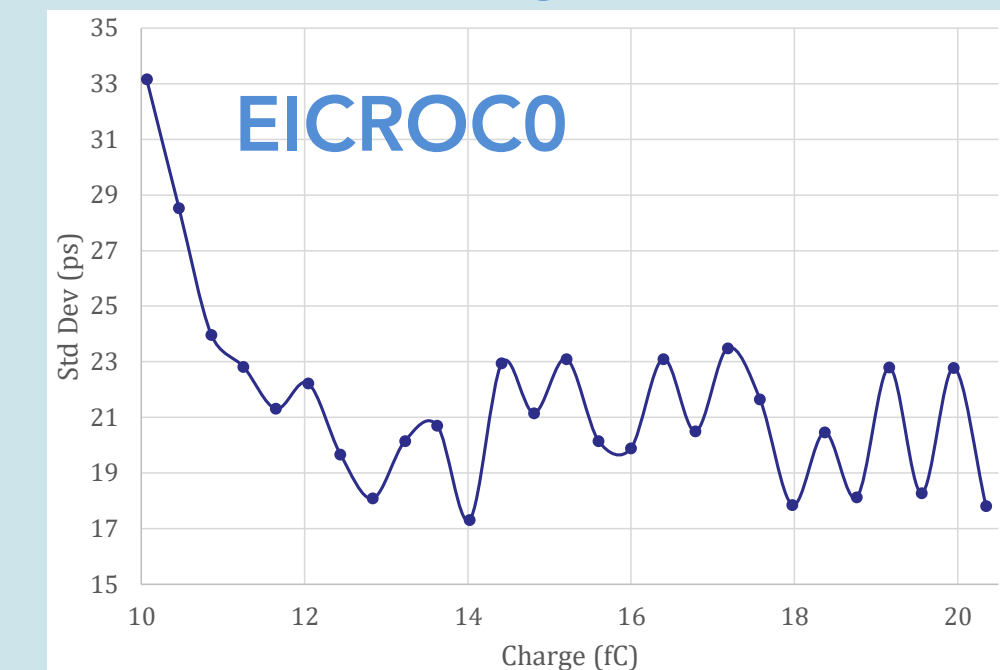
ASIC performance

- EICROC has been designed to be used for the pixel-type sensor readout
 - EICROC0 is available with 4x4 geometry
- Digital block of ADC and TDC results were shown
 - The significant jitter issue by the clock delay block on the FPGA has been fixed this June
 - Linear trend in injected charge and ADC has been observed
 - TDC jitter of 33 (17.5) ps and 20 (12.5) ps at 10 fC and 20 fC w/ (w/o) sensor have been observed
- EICROC1 will address a larger demonstration 4x16 or 8x16 or 4x32 or 8x32
 - Submission @ the end of 2024
- FCFD which is one option for the strip-type sensor readout analog block results with the test beam attached to AC-LGAD was presented
 - The timing resolution of the FCFD + sensor is 55 ps without corrections has been reported
 - The performance is affected by the AC-LGAD larger input capacitance than expected
 - After matching the input capacitance, 35 ps timing resolution is expected

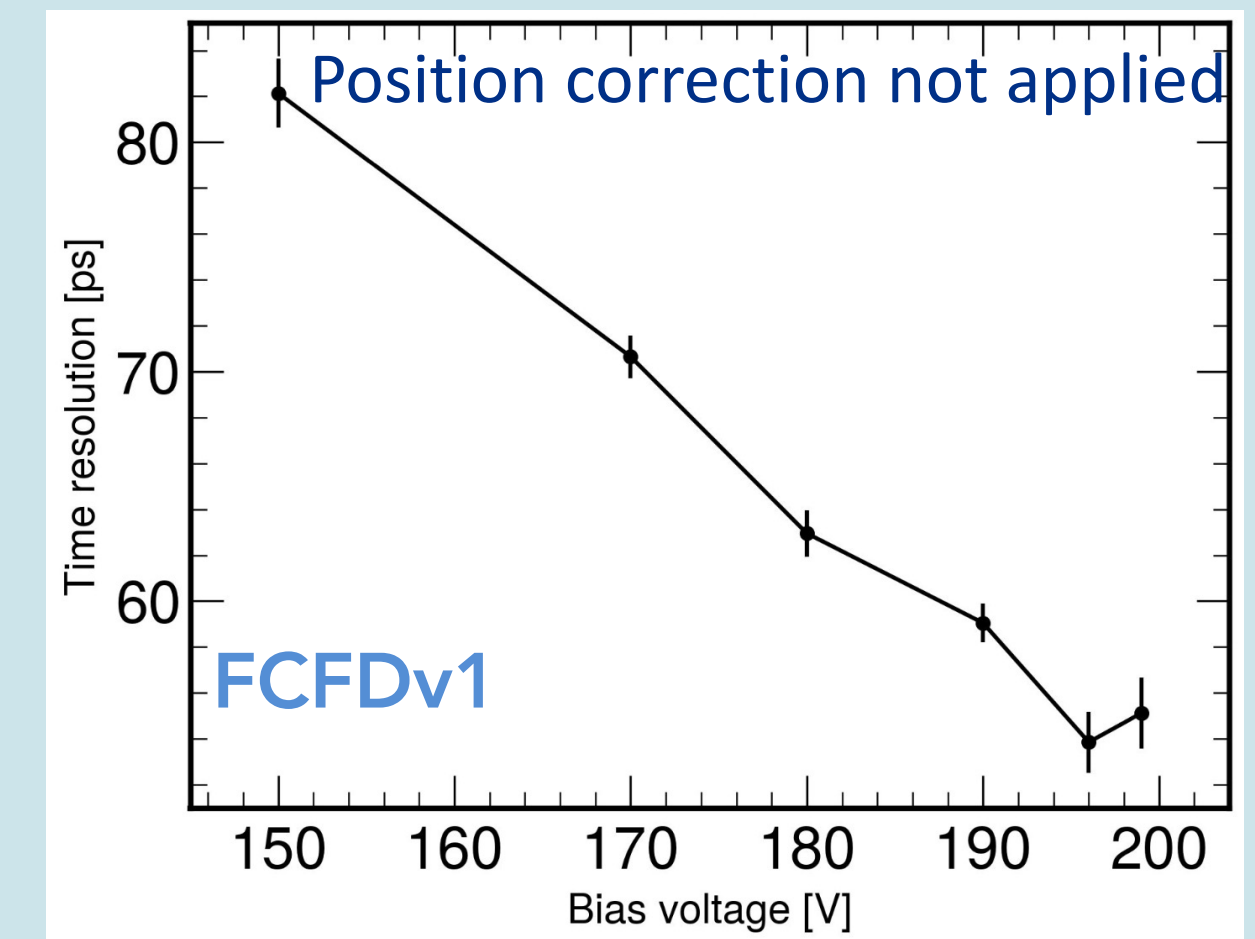
Charge v.s. ADC



TDC jitter



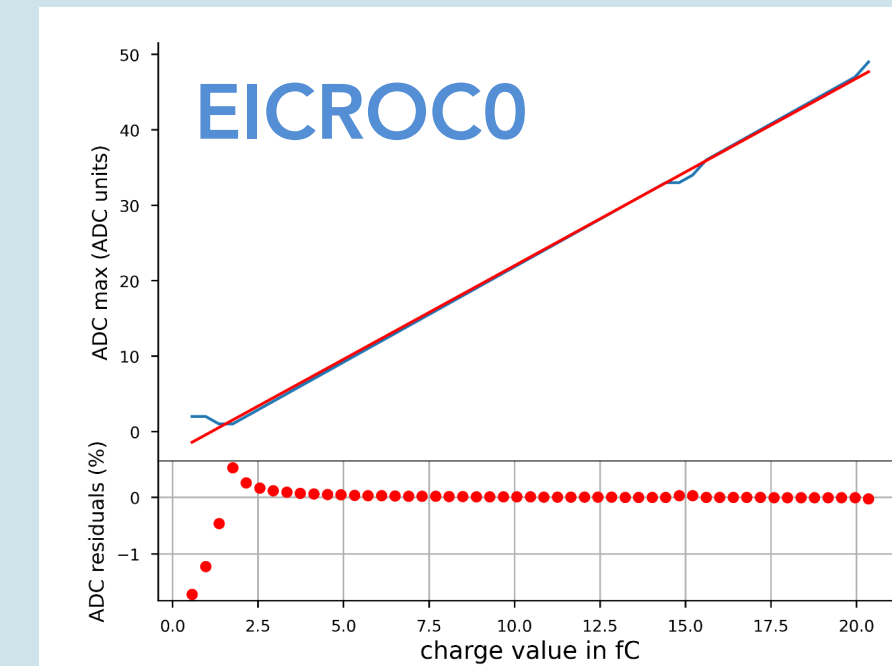
Timing reso. w/ AC-LGAD



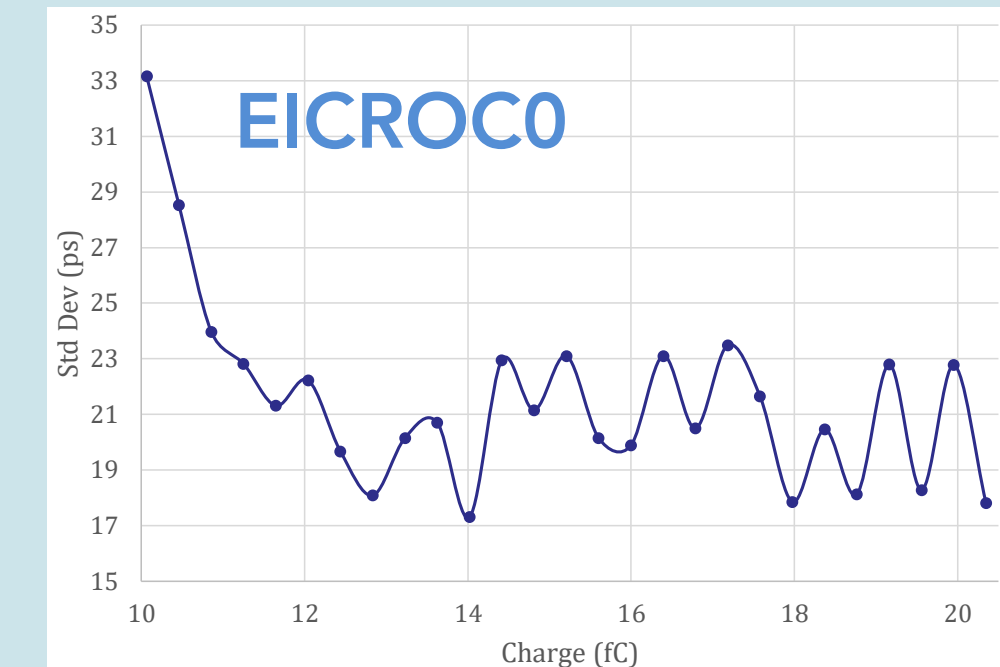
ASIC performance

- EICROC has been designed to be used for the pixel-type sensor readout
 - EICROC0 is available with 4x4 geometry
- Digital block of ADC and TDC results were shown
 - The significant jitter issue by the clock delay block on the FPGA has been fixed this June
 - Linear trend in injected charge and ADC has been observed
 - TDC jitter of 33 (17.5) ps and 20 (12.5) ps at 10 fC and 20 fC w/ (w/o) sensor have been observed
- EICROC1 will address a larger demonstration 4x16 or 8x16 or 4x32 or 8x32
 - Submission @ the end of 2024
- FCFD which is one option for the strip-type sensor readout analog block results with the test beam attached to AC-LGAD was presented
 - The timing resolution of the FCFD + sensor is 55 ps without corrections has been reported
 - The performance is affected by the AC-LGAD larger input capacitance than expected
 - After matching the input capacitance, 35 ps timing resolution is expected
- FCFDv2 with a digital block full-size prototype will be obtained @ end of 2025

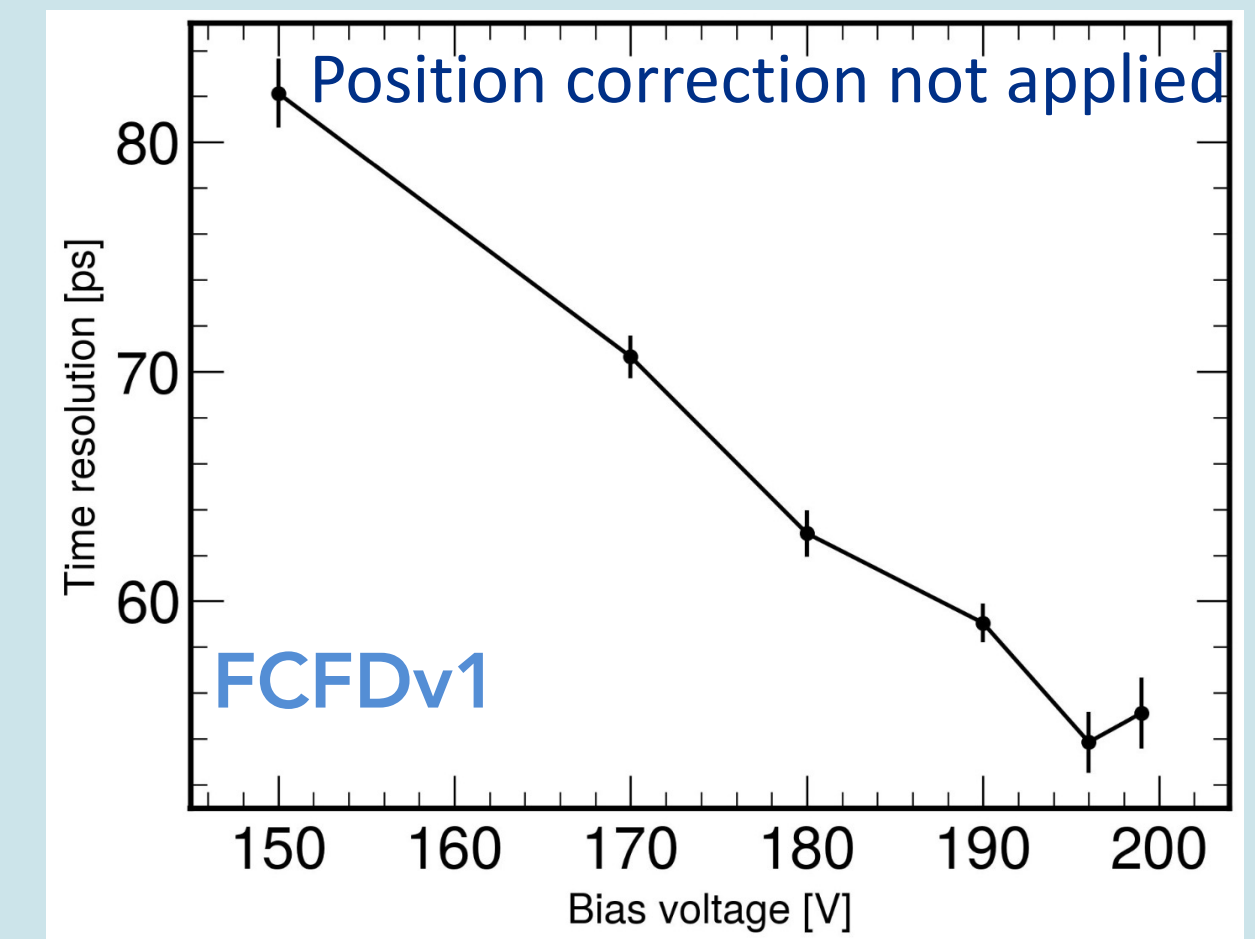
Charge v.s. ADC



TDC jitter



Timing reso. w/ AC-LGAD



Front-end electronics

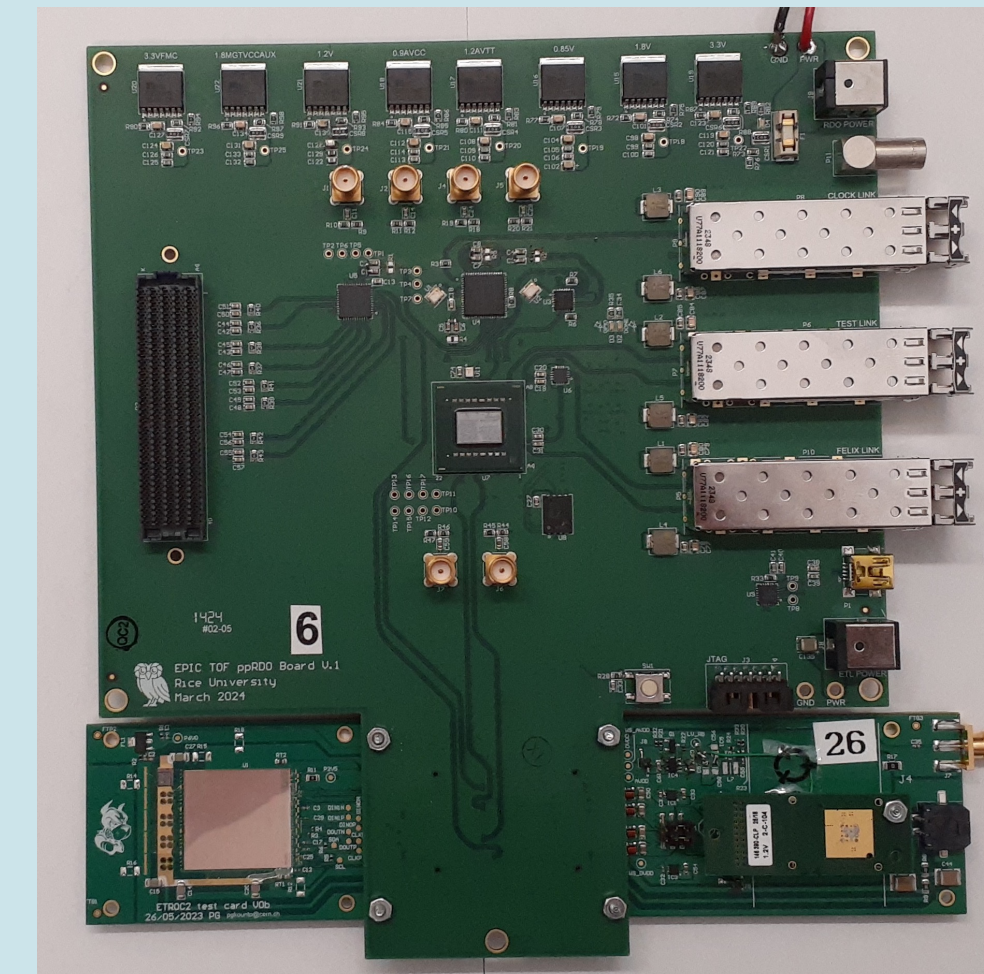
- Pre-prototype readout board (ppRDO) has been made with ETROC2 ASIC
 - 6 boards are available
- Several tests are ongoing
 - FPGA firmware development
 - Readout test with ETROC2
 - Evaluation of power consumption



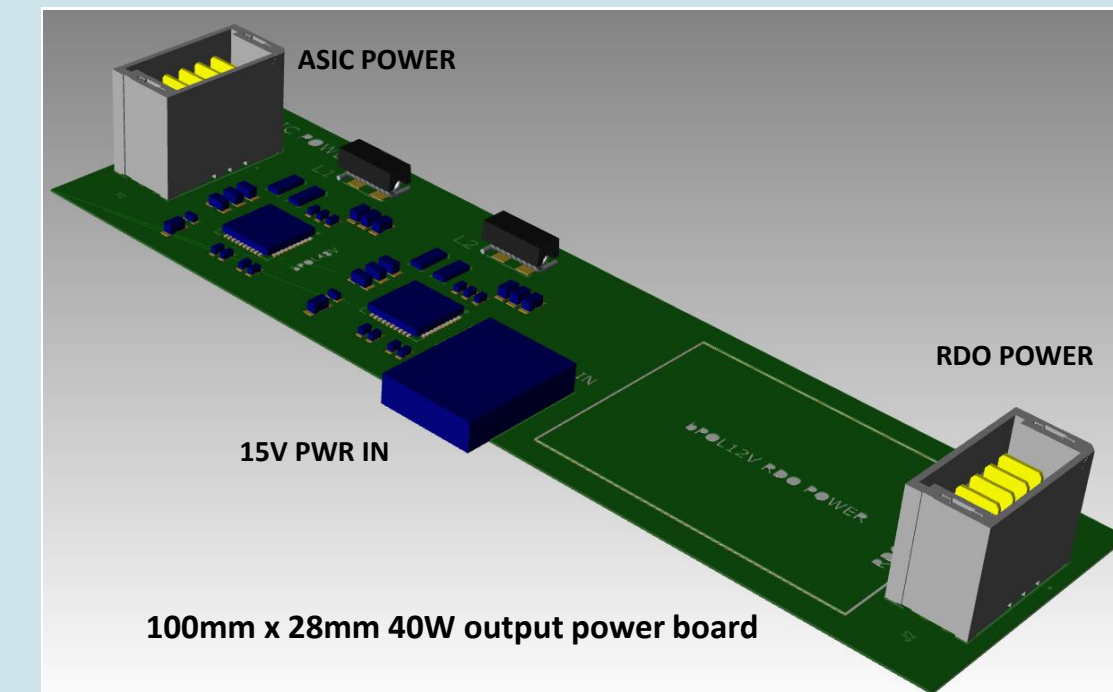
Front-end electronics

- Pre-prototype readout board (ppRDO) has been made with ETROC2 ASIC
 - 6 boards are available
- Several tests are ongoing
 - FPGA firmware development
 - Readout test with ETROC2
 - Evaluation of power consumption
- Power board (PB) design is ongoing
 - PB supplies 5 different voltages
 - ASIC: 1.2 V (EICROC case)
 - FPGA: 1.8, 1.2, 0.9, 0.85 V
 - SFP+: 3.3 V
 - Several options for DC-DC converters are being tested

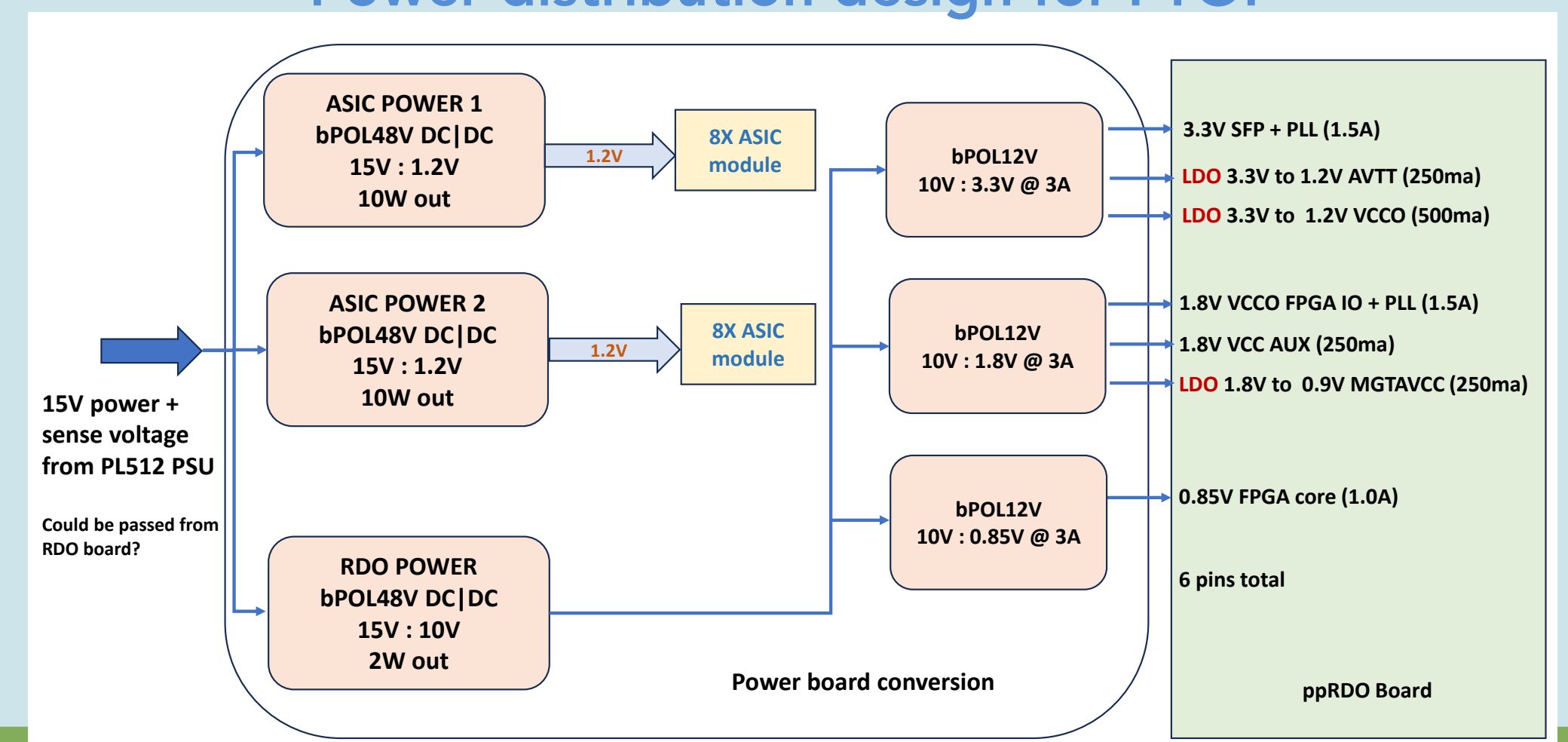
ppRDO



PB design



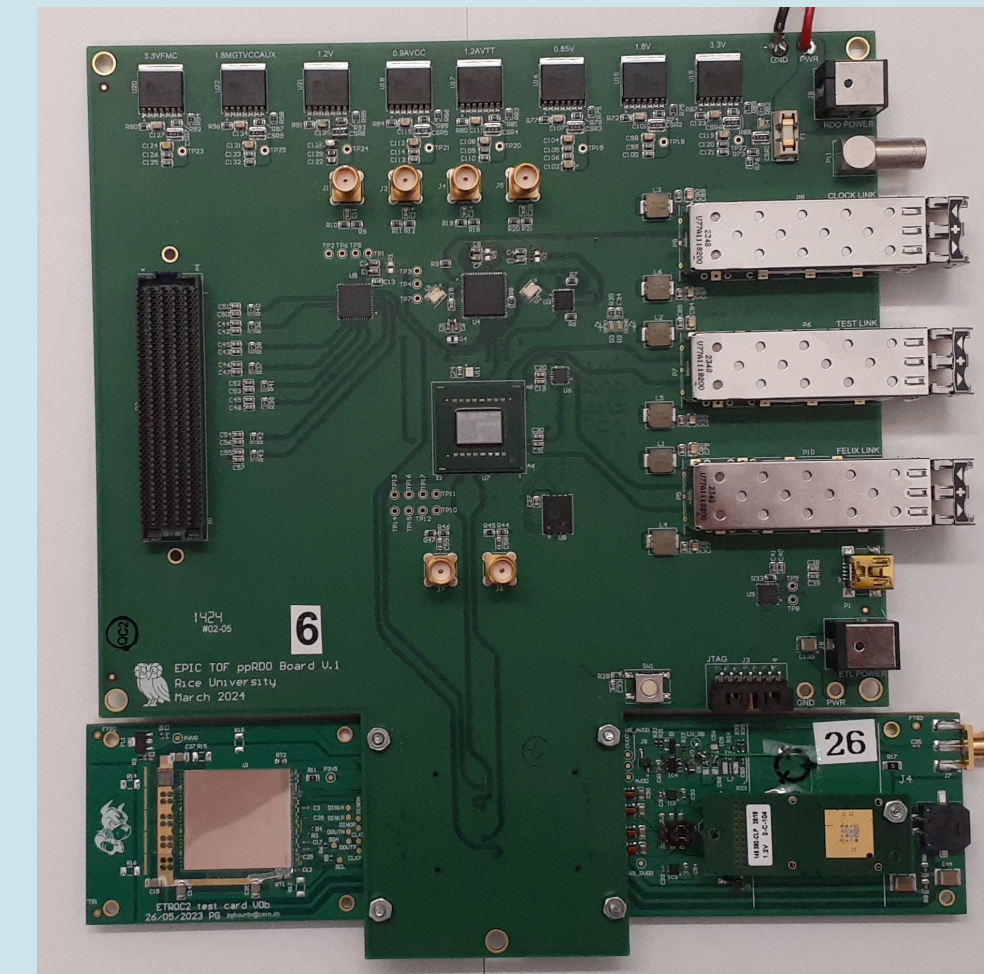
Power distribution design for FTOF



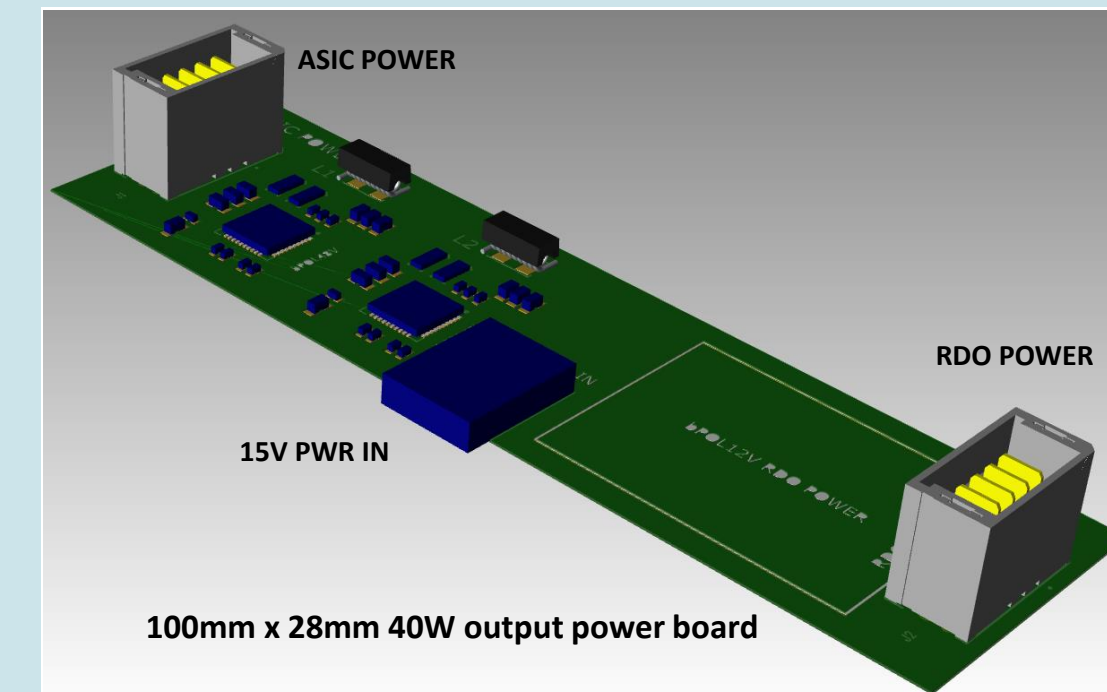
Front-end electronics

- Pre-prototype readout board (ppRDO) has been made with ETROC2 ASIC
 - 6 boards are available
- Several tests are ongoing
 - FPGA firmware development
 - Readout test with ETROC2
 - Evaluation of power consumption
- Power board (PB) design is ongoing
 - PB supplies 5 different voltages
 - ASIC: 1.2 V (EICROC case)
 - FPGA: 1.8, 1.2, 0.9, 0.85 V
 - SFP+: 3.3 V
 - Several options for DC-DC converters are being tested

ppRDO



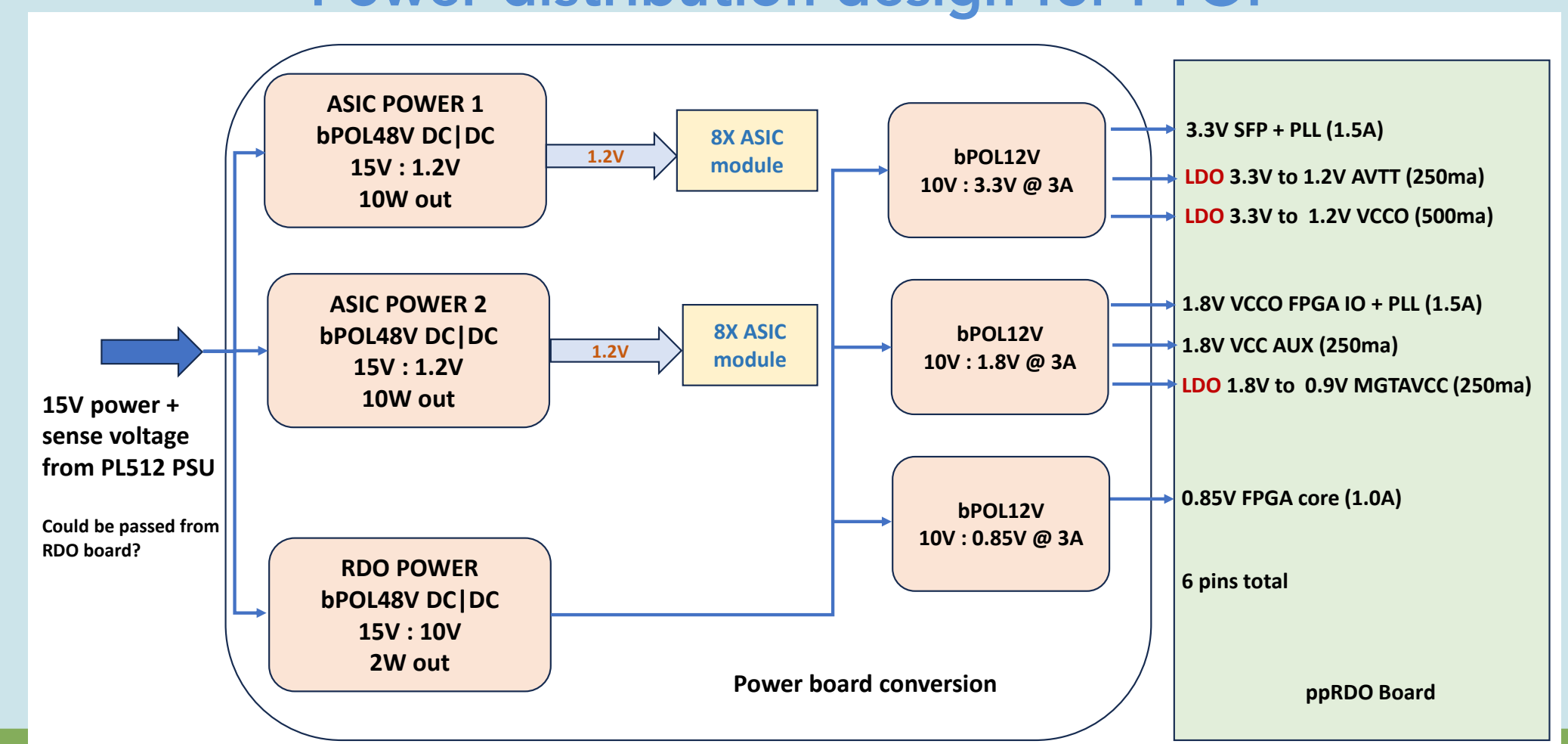
PB design



Roadmap and timeline of SH development

- 2024: **Prototype v0** (pre-prototype): establish all essential functionalities and readout chain.
- 2025: **Prototype v1**: first prototype with realistic dimensions, and meeting requirements/constraints for FTOF and BTOF, and other AC-LGADs subsystems.
 - Focusing on FTOF first
- 2026: **Prototype v2**: final prototype

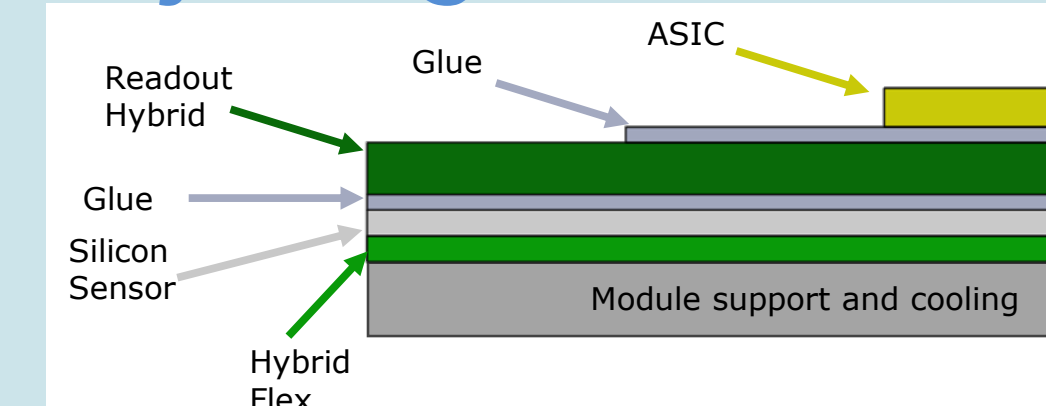
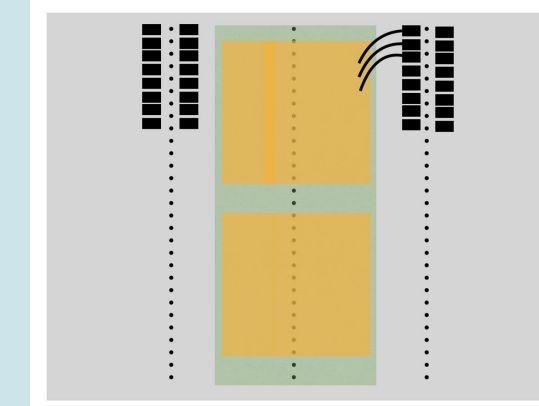
Power distribution design for FTOF



Mechanics, cooling, and FPC

- The idea of BTOF module assembly has matured
 - Wire length is uniform, but worse cooling power due to many layers between ASIC and cooling pipe (support structure)

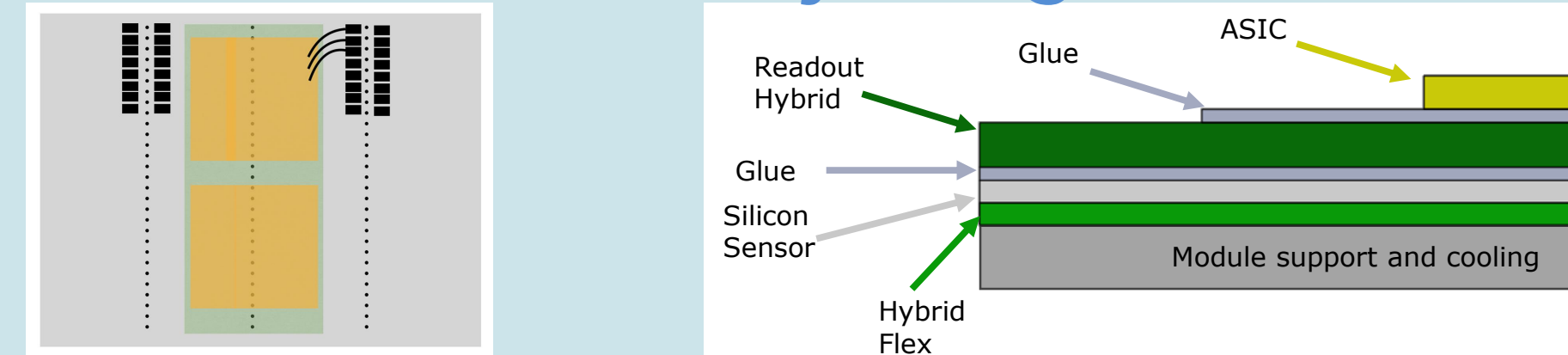
Module assembly design



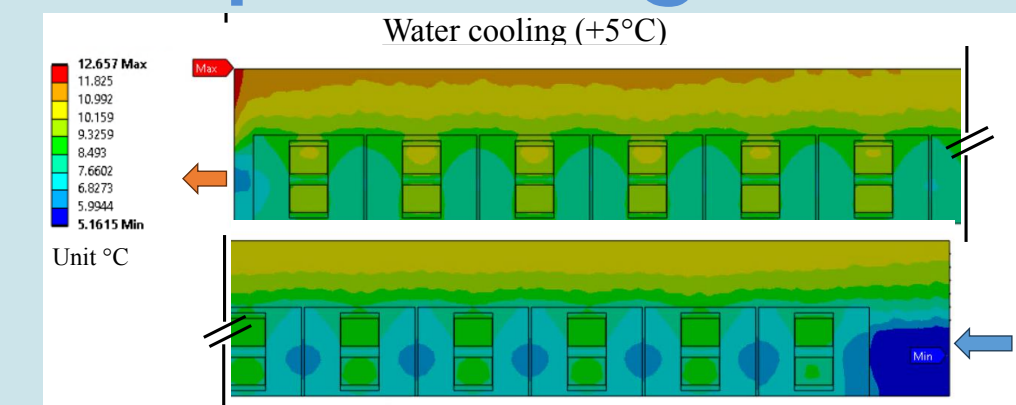
Mechanics, cooling, and FPC

- The idea of BTOF module assembly has matured
 - Wire length is uniform, but worse cooling power due to many layers between ASIC and cooling pipe (support structure)
 - Difficulties in maintaining temperature uniformity in a stave are found in the thermal conductivity simulation
 - The design working well or not depends on ASIC power consumption

Module assembly design



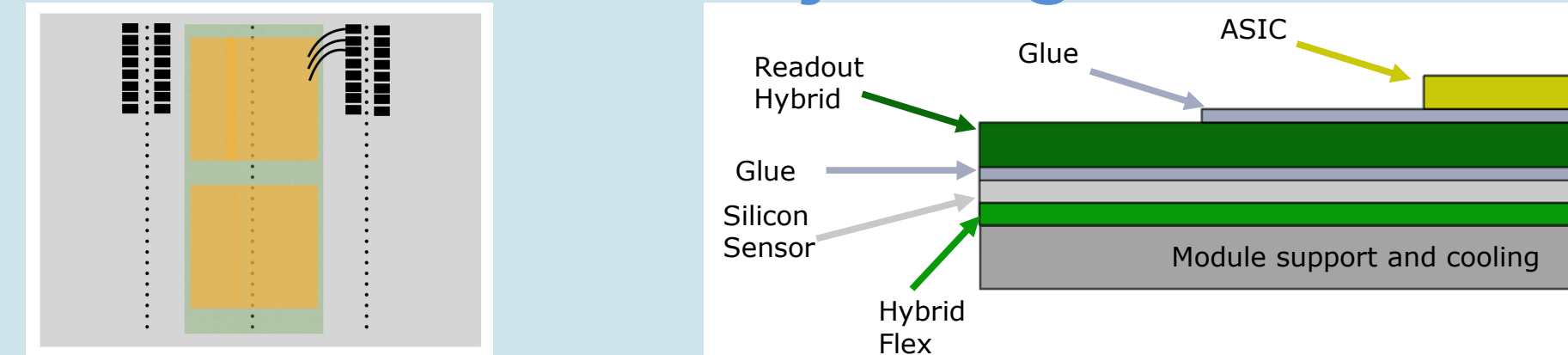
Temperature gradient



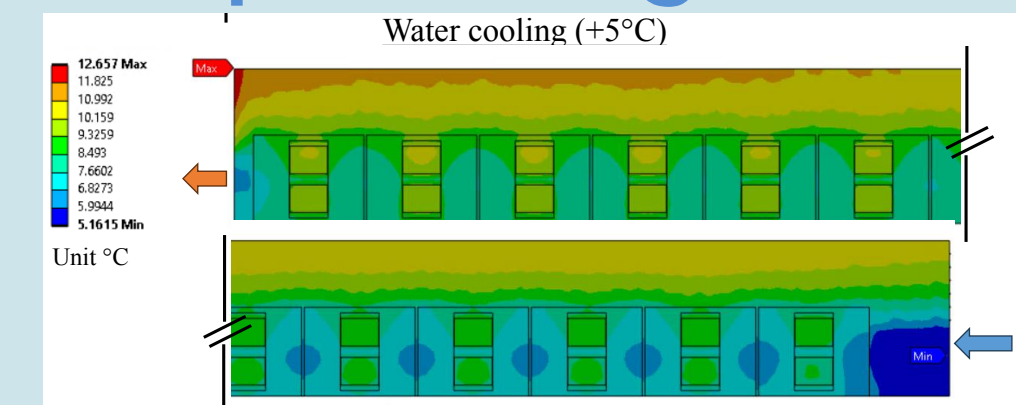
Mechanics, cooling, and FPC

- The idea of BTOF module assembly has matured
 - Wire length is uniform, but worse cooling power due to many layers between ASIC and cooling pipe (support structure)
 - Difficulties in maintaining temperature uniformity in a stave are found in the thermal conductivity simulation
 - The design working well or not depends on ASIC power consumption
- New alternative idea of double side stave has been presented
 - Some advantages of no acceptance hole and easier cooling are claimed, but need to check if there is design showstopper

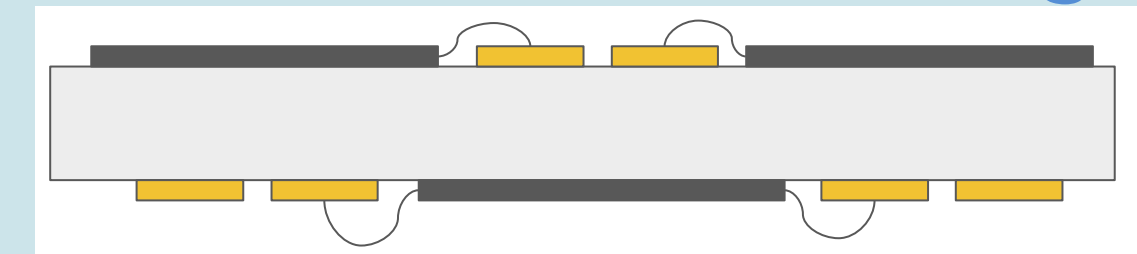
Module assembly design



Temperature gradient



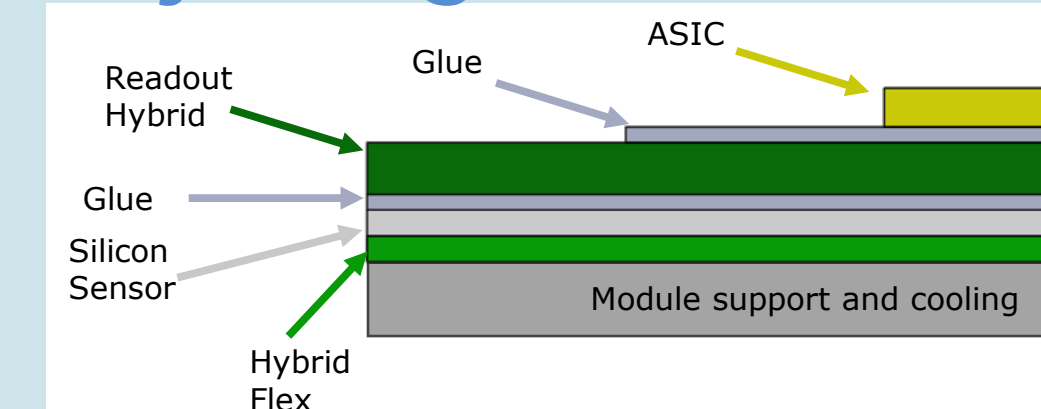
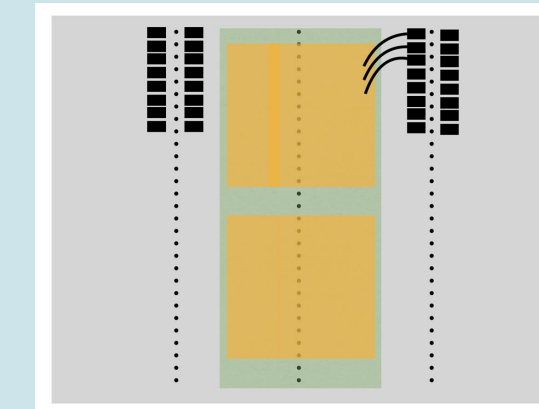
Double side stave design



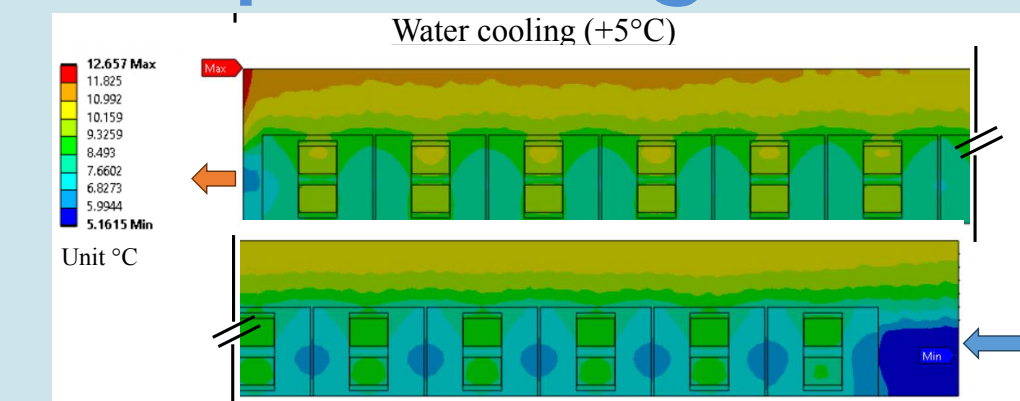
Mechanics, cooling, and FPC

- The idea of BTOF module assembly has matured
 - Wire length is uniform, but worse cooling power due to many layers between ASIC and cooling pipe (support structure)
 - Difficulties in maintaining temperature uniformity in a stave are found in the thermal conductivity simulation
 - The design working well or not depends on ASIC power consumption
- New alternative idea of double side stave has been presented
 - Some advantages of no acceptance hole and easier cooling are claimed, but need to check if there is design showstopper
- Support structure production process has been shown
 - Bonding and curing process

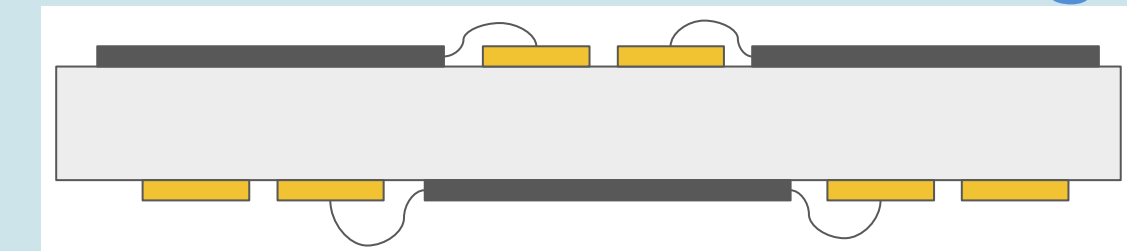
Module assembly design



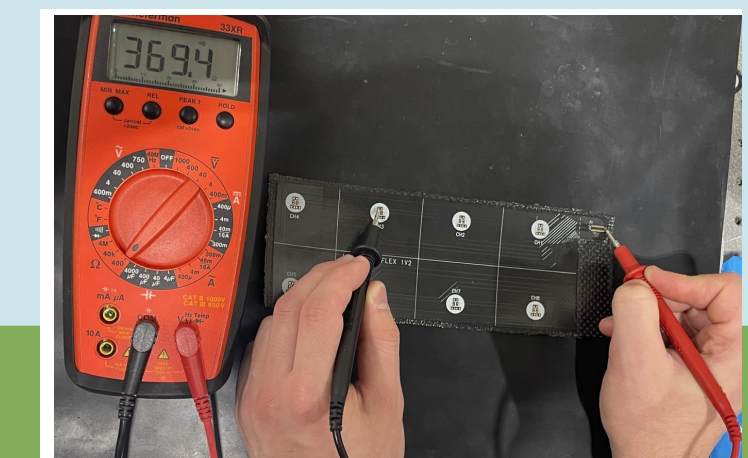
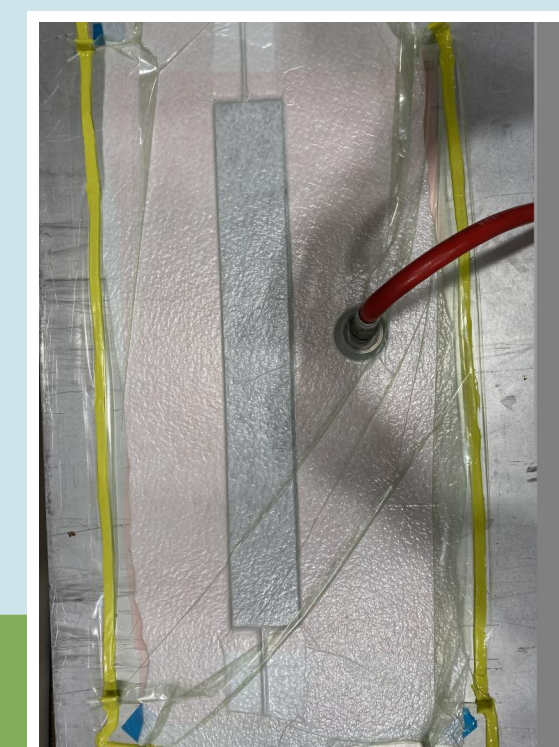
Temperature gradient



Double side stave design



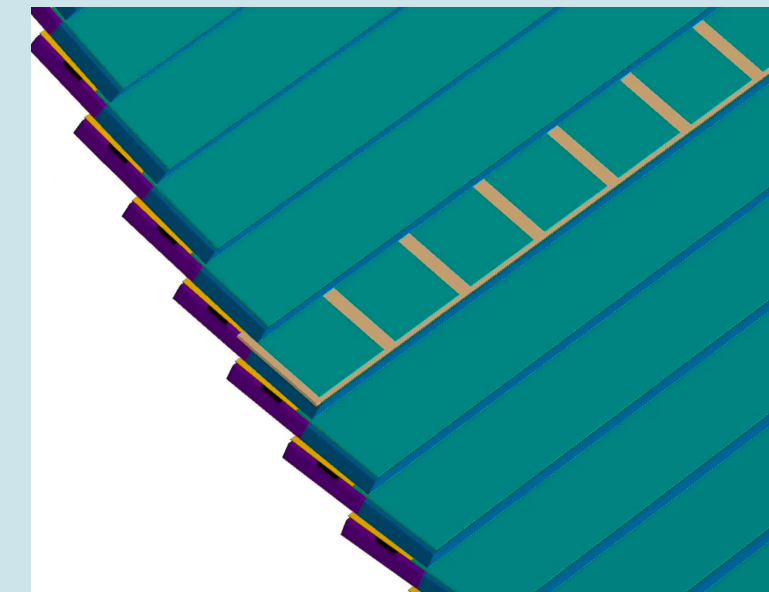
Support structure production process



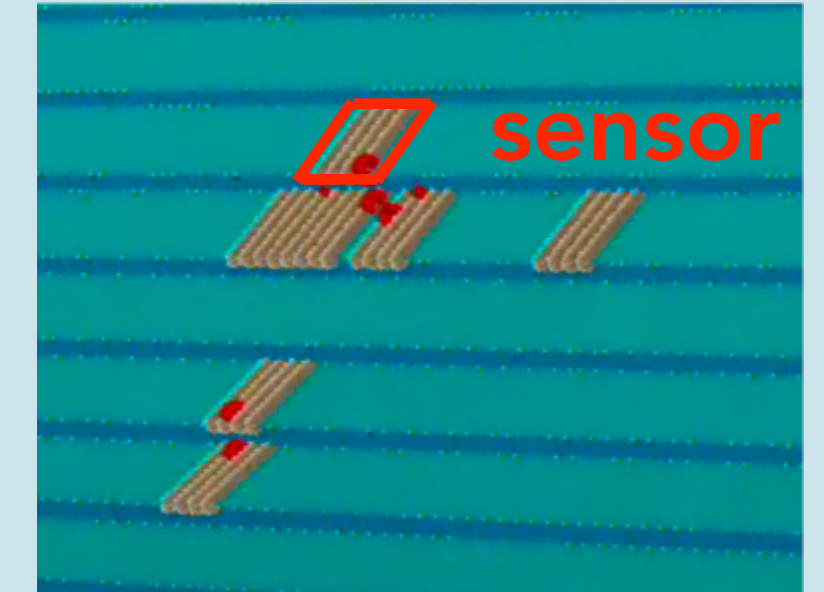
Simulation

- Realistic sensor segmentation has been implemented
 - Before one large sensor volume was on a stave, but now each sensor volume is implemented
 - Readout metals have been also implemented

New segment



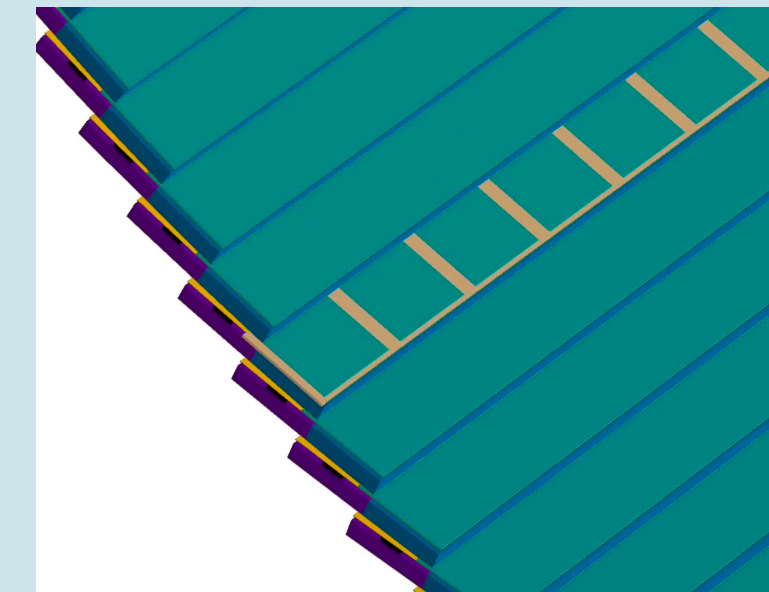
Strip visualization



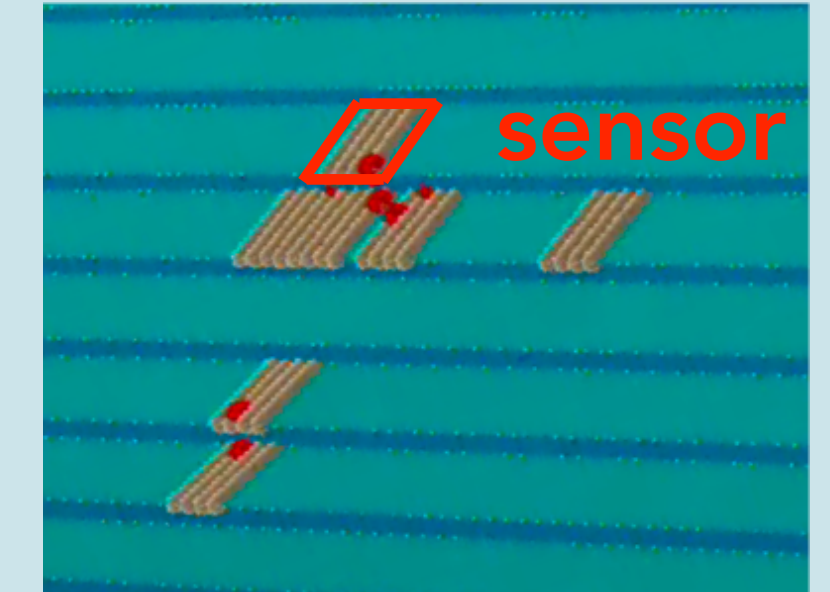
Simulation

- Realistic sensor segmentation has been implemented
 - Before one large sensor volume was on a stave, but now each sensor volume is implemented
 - Readout metals have been also implemented
- New functions of charge sharing and digitization have been implemented in the simulation
 - The signal strength and charge-sharing profile come from real sensor result

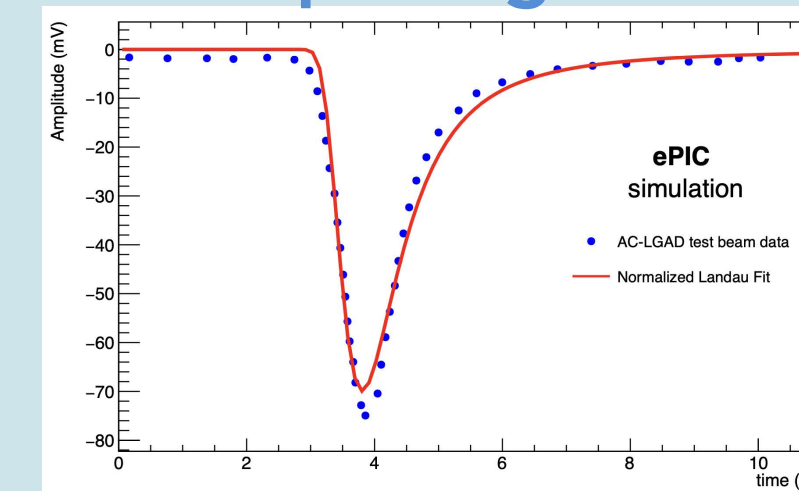
New segment



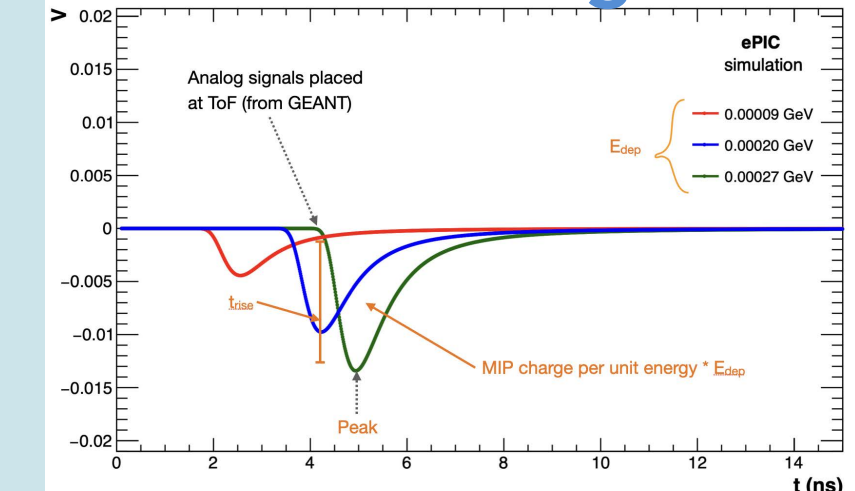
Strip visualization



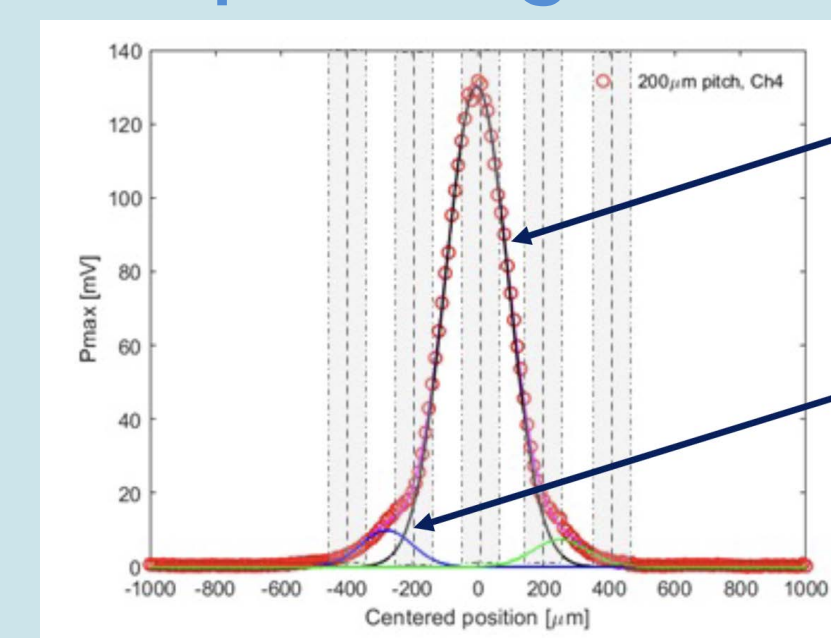
Input signal



Mimicked signal



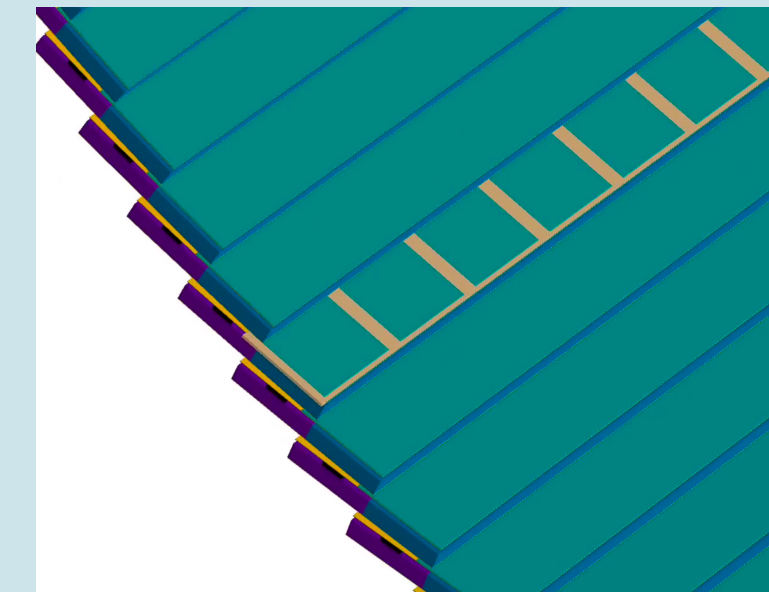
Input charge dist.



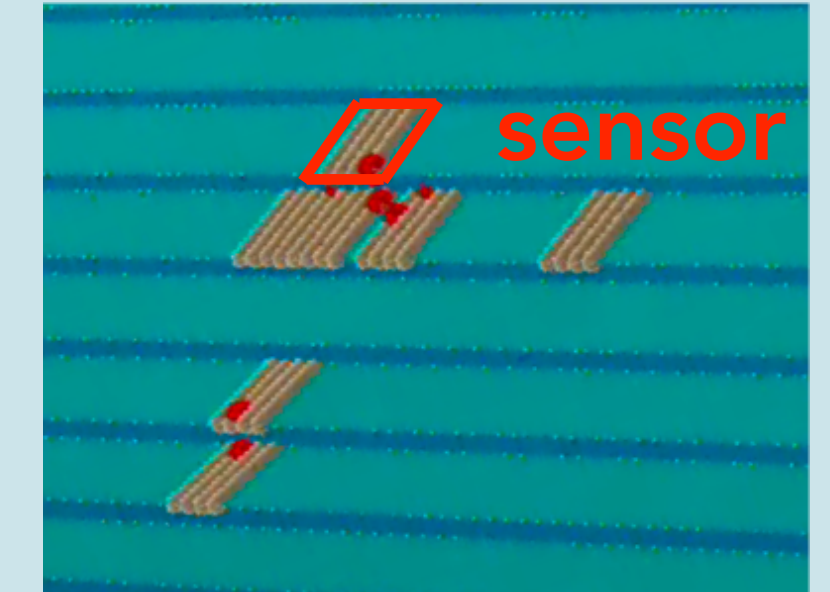
Simulation

- Realistic sensor segmentation has been implemented
 - Before one large sensor volume was on a stave, but now each sensor volume is implemented
 - Readout metals have been also implemented
- New functions of charge sharing and digitization have been implemented in the simulation
 - The signal strength and charge-sharing profile come from real sensor result
- The positional resolution depends on where the particles were incident relative to the position of the readout metal
 - Charge is not shared enough when a particle hits the corner of the sensor → worse spatial resolution
 - Possibly the required charge-sharing profile for finding the best spatial resolution can be extracted

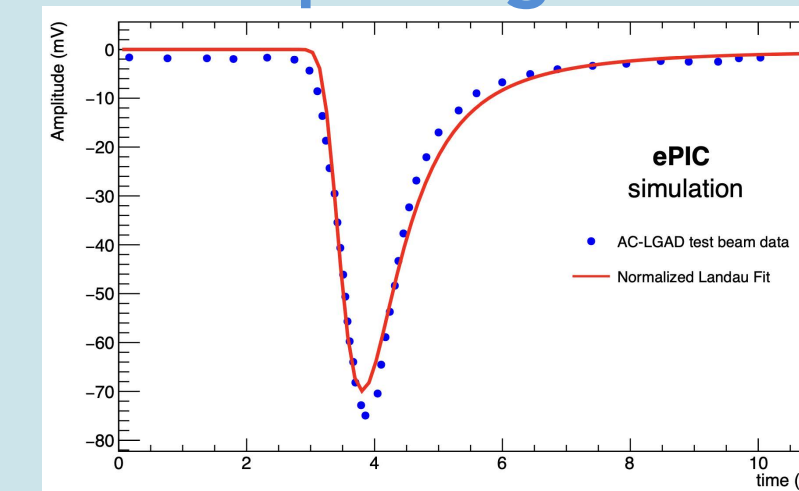
New segment



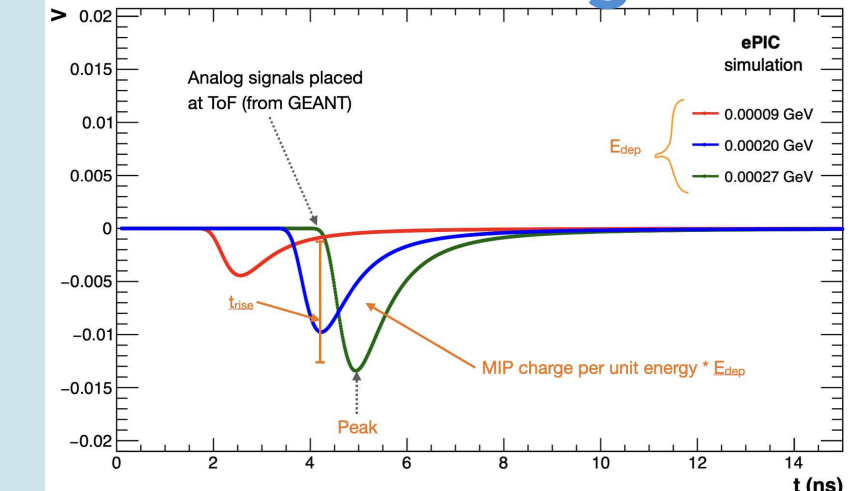
Strip visualization



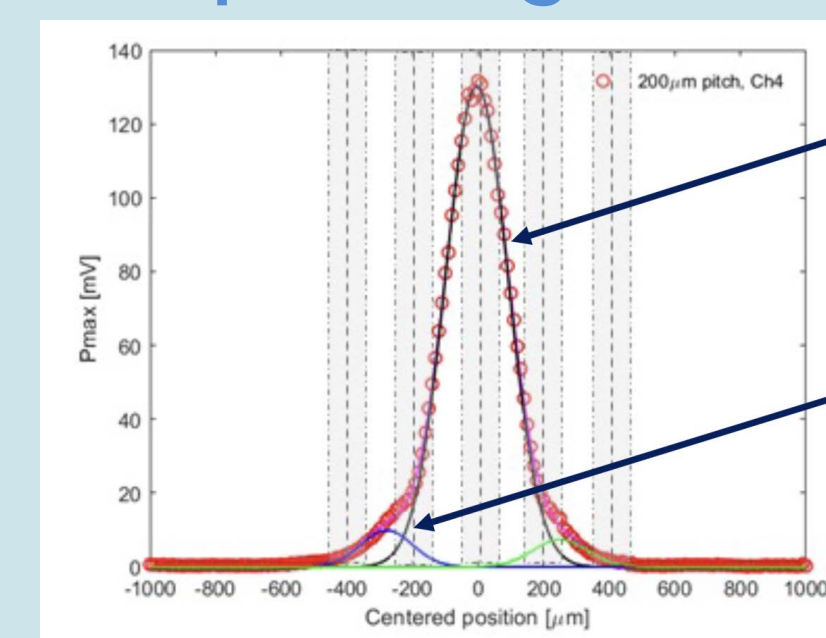
Input signal



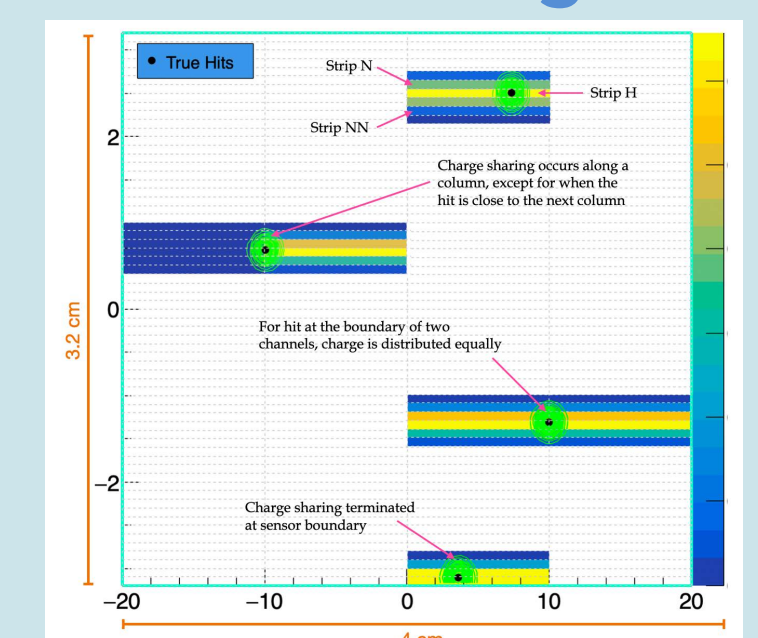
Mimicked signal



Input charge dist.



Mimicked charge dist.



Summary

- Finalize the last test beam campaign analysis and timing resolution of 35 ~ 45 ps, and spatial resolution of 15 ~ 30 μm are achieved by BNL and HPK
 - The performance is under control and better prototypes will be received
 - Full-size strip-type sensor of HPK will be received in a few months

Summary

- Finalize the last test beam campaign analysis and timing resolution of 35 ~ 45 ps, and spatial resolution of 15 ~ 30 μm are achieved by BNL and HPK
 - The performance is under control and better prototypes will be received
 - Full-size strip-type sensor of HPK will be received in a few months
- ASIC for the pixel-type sensor (EICROC) development is progressing well
 - The linear charge v.s. ADC and ~20 ps TDC resolution are measured

Summary

- Finalize the last test beam campaign analysis and timing resolution of 35 ~ 45 ps, and spatial resolution of 15 ~ 30 μm are achieved by BNL and HPK
 - The performance is under control and better prototypes will be received
 - Full-size strip-type sensor of HPK will be received in a few months
- ASIC for the pixel-type sensor (EICROC) development is progressing well
 - The linear charge v.s. ADC and ~20 ps TDC resolution are measured
- ASIC for the strip-type sensor (FCFD) analog block + AC-LGAD sensor performance is measured with test beam
 - The timing resolution of 55 ps is measured due larger capacitance of the strip-type sensor than expected

Summary

- Finalize the last test beam campaign analysis and timing resolution of 35 ~ 45 ps, and spatial resolution of 15 ~ 30 μm are achieved by BNL and HPK
 - The performance is under control and better prototypes will be received
 - Full-size strip-type sensor of HPK will be received in a few months
- ASIC for the pixel-type sensor (EICROC) development is progressing well
 - The linear charge v.s. ADC and ~20 ps TDC resolution are measured
- ASIC for the strip-type sensor (FCFD) analog block + AC-LGAD sensor performance is measured with test beam
 - The timing resolution of 55 ps is measured due larger capacitance of the strip-type sensor than expected
- Frontend electronics, mechanical support structure, cooling, and sensor-ASIC hybrid design are ongoing

Summary

- Finalize the last test beam campaign analysis and timing resolution of 35 ~ 45 ps, and spatial resolution of 15 ~ 30 μm are achieved by BNL and HPK
 - The performance is under control and better prototypes will be received
 - Full-size strip-type sensor of HPK will be received in a few months
- ASIC for the pixel-type sensor (EICROC) development is progressing well
 - The linear charge v.s. ADC and ~20 ps TDC resolution are measured
- ASIC for the strip-type sensor (FCFD) analog block + AC-LGAD sensor performance is measured with test beam
 - The timing resolution of 55 ps is measured due larger capacitance of the strip-type sensor than expected
- Frontend electronics, mechanical support structure, cooling, and sensor-ASIC hybrid design are ongoing
- New functions, realistic segmentation, digitization, and charge-sharing, have been implemented in the simulation
 - The best charge-sharing property can be measured by the new function

What was discussed

- We need ASICs with a digital block for the strip-type sensors
 - We are making steady progress toward strip-type sensor ASIC choice, but the inter-dependence on the ASIC makes it difficult to finalize FEE, FPC, and other components at this moment.
 - We need reference ideas for all designs (FCFD with digit. block will be received end of 2025)
 - HGCROC3 is one of the candidates, but modification is necessary
 - Large power consumption: HGCROC3 ~ 15 mW/ch, FCFD ~ 2 mW/ch, and EICROC ~ 1 mW/ch
 - HGCROC3 doesn't support streaming readout (need modification)

What was discussed

- We need ASICs with a digital block for the strip-type sensors
 - We are making steady progress toward strip-type sensor ASIC choice, but the inter-dependence on the ASIC makes it difficult to finalize FEE, FPC, and other components at this moment.
 - We need reference ideas for all designs (FCFD with digit. block will be received end of 2025)
 - HGCROC3 is one of the candidates, but modification is necessary
 - Large power consumption: HGCROC3 ~ 15 mW/ch, FCFD ~ 2 mW/ch, and EICROC ~ 1 mW/ch
 - HGCROC3 doesn't support streaming readout (need modification)
 - **We have to promote ASIC development for strip-type sensors more strongly**

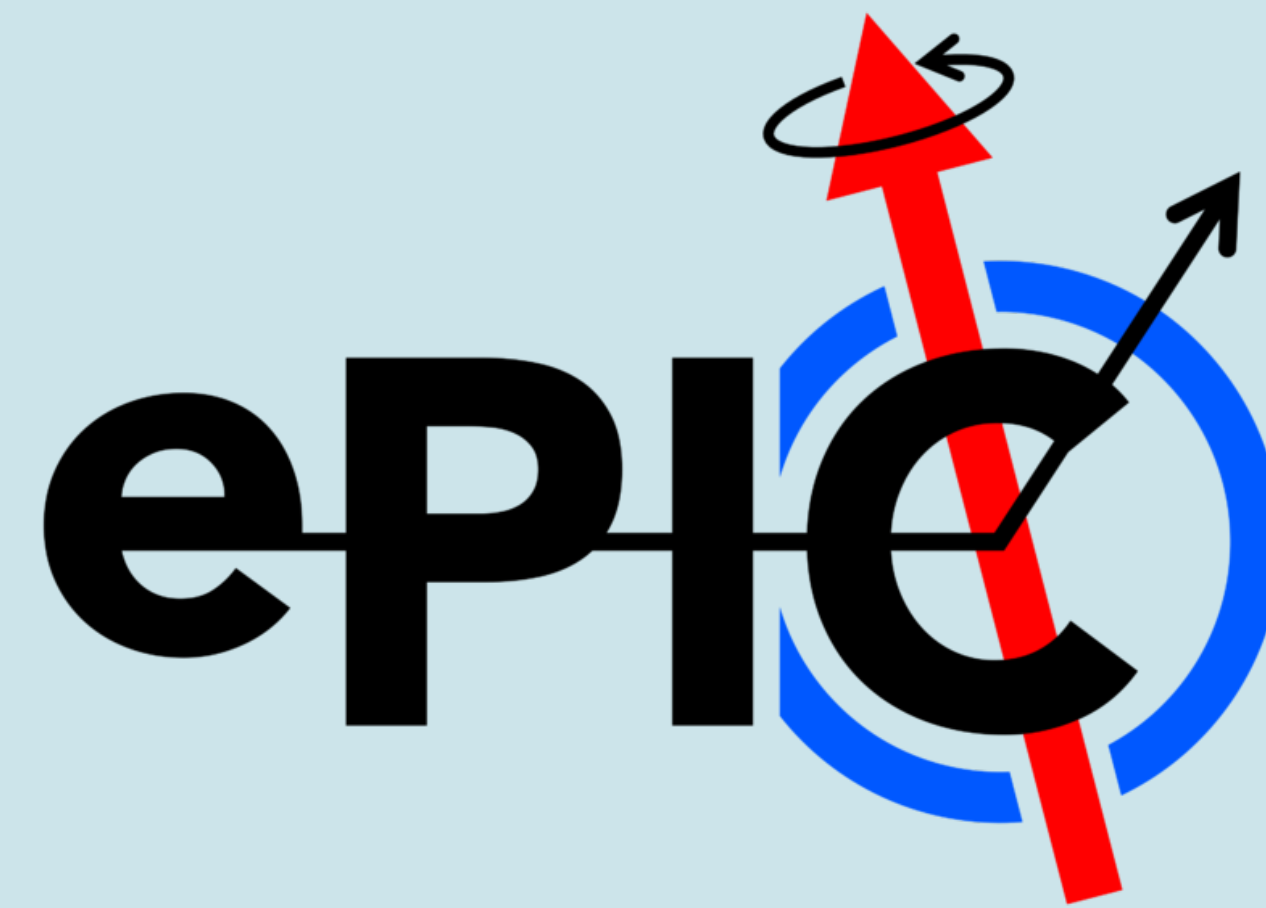
What was discussed

- We need ASICs with a digital block for the strip-type sensors
 - We are making steady progress toward strip-type sensor ASIC choice, but the inter-dependence on the ASIC makes it difficult to finalize FEE, FPC, and other components at this moment.
 - We need reference ideas for all designs (FCFD with digit. block will be received end of 2025)
 - HGCROC3 is one of the candidates, but modification is necessary
 - Large power consumption: HGCROC3 ~ 15 mW/ch, FCFD ~ 2 mW/ch, and EICROC ~ 1 mW/ch
 - HGCROC3 doesn't support streaming readout (need modification)
 - **We have to promote ASIC development for strip-type sensors more strongly**
- Long (135 cm) and low material (1% X/X_0) stave design is a key point in demonstrating the true ability of AC-LGAD
 - Temperature control (cooling system) design is one of the most important elements for BTOF
 - AC-LGAD sensor performance strongly depends on temperature
 - The design has a large impact on the temperature control of each sensor
 - Low material (1% X/X_0) long stave design requires a high-level technology and imposes significant limitations on functionality

What was discussed

- We need ASICs with a digital block for the strip-type sensors
 - We are making steady progress toward strip-type sensor ASIC choice, but the inter-dependence on the ASIC makes it difficult to finalize FEE, FPC, and other components at this moment.
 - We need reference ideas for all designs (FCFD with digit. block will be received end of 2025)
 - HGCROC3 is one of the candidates, but modification is necessary
 - Large power consumption: HGCROC3 ~ 15 mW/ch, FCFD ~ 2 mW/ch, and EICROC ~ 1 mW/ch
 - HGCROC3 doesn't support streaming readout (need modification)
 - **We have to promote ASIC development for strip-type sensors more strongly**
- Long (135 cm) and low material (1% X/X_0) stave design is a key point in demonstrating the true ability of AC-LGAD
 - Temperature control (cooling system) design is one of the most important elements for BTOF
 - AC-LGAD sensor performance strongly depends on temperature
 - The design has a large impact on the temperature control of each sensor
 - Low material (1% X/X_0) long stave design requires a high-level technology and imposes significant limitations on functionality
 - **It is necessary to continue to understand and optimize the material budget (1% BTOF and 5% FTOF) and its impacts on the design of FPC and cooling integration**

Backup slides



AC-LGAD TOF

Satoshi Yano (Hiroshima University)

ePIC Collaboration meeting @ Lehigh University

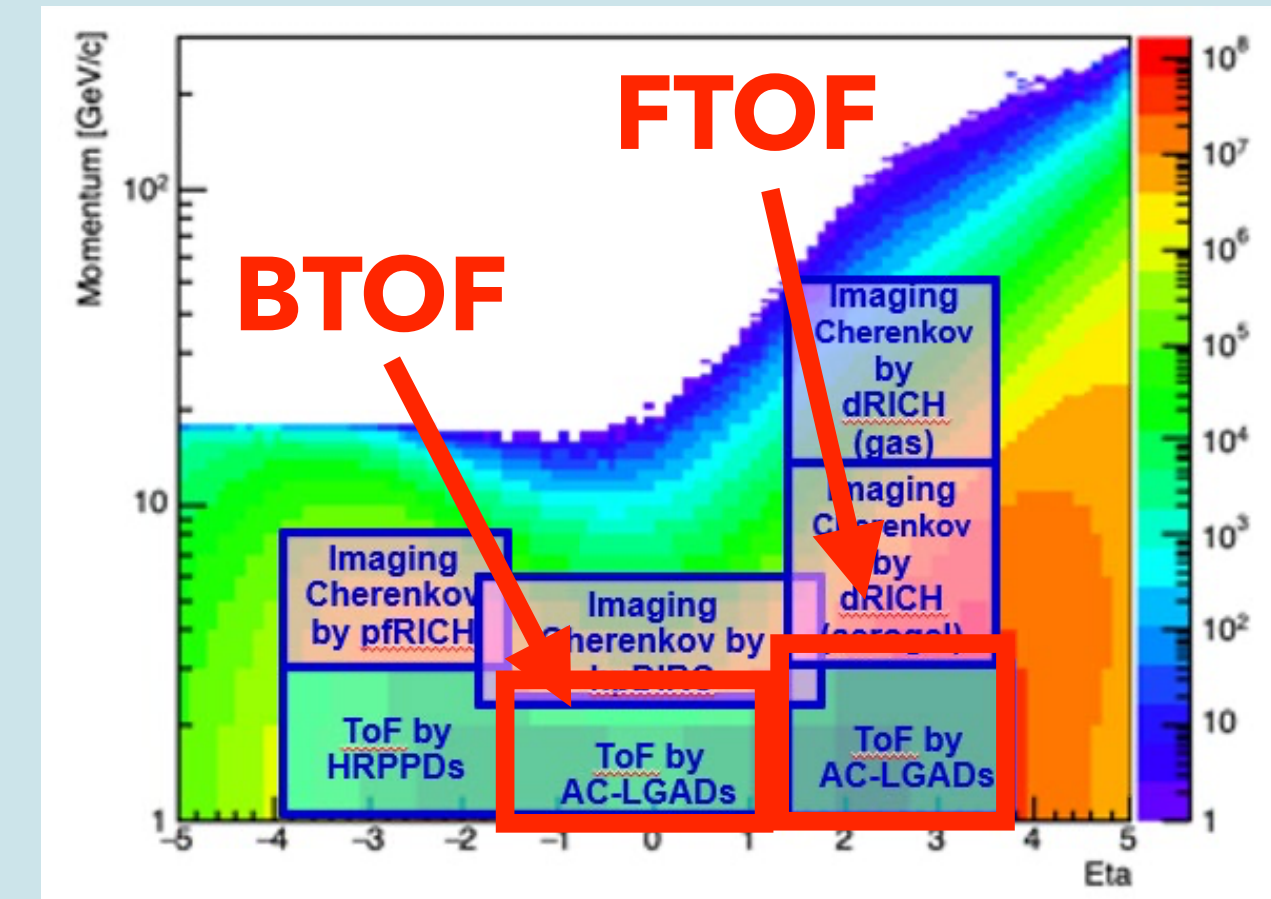
07/25/2024

Role of the TOF in the ePIC project

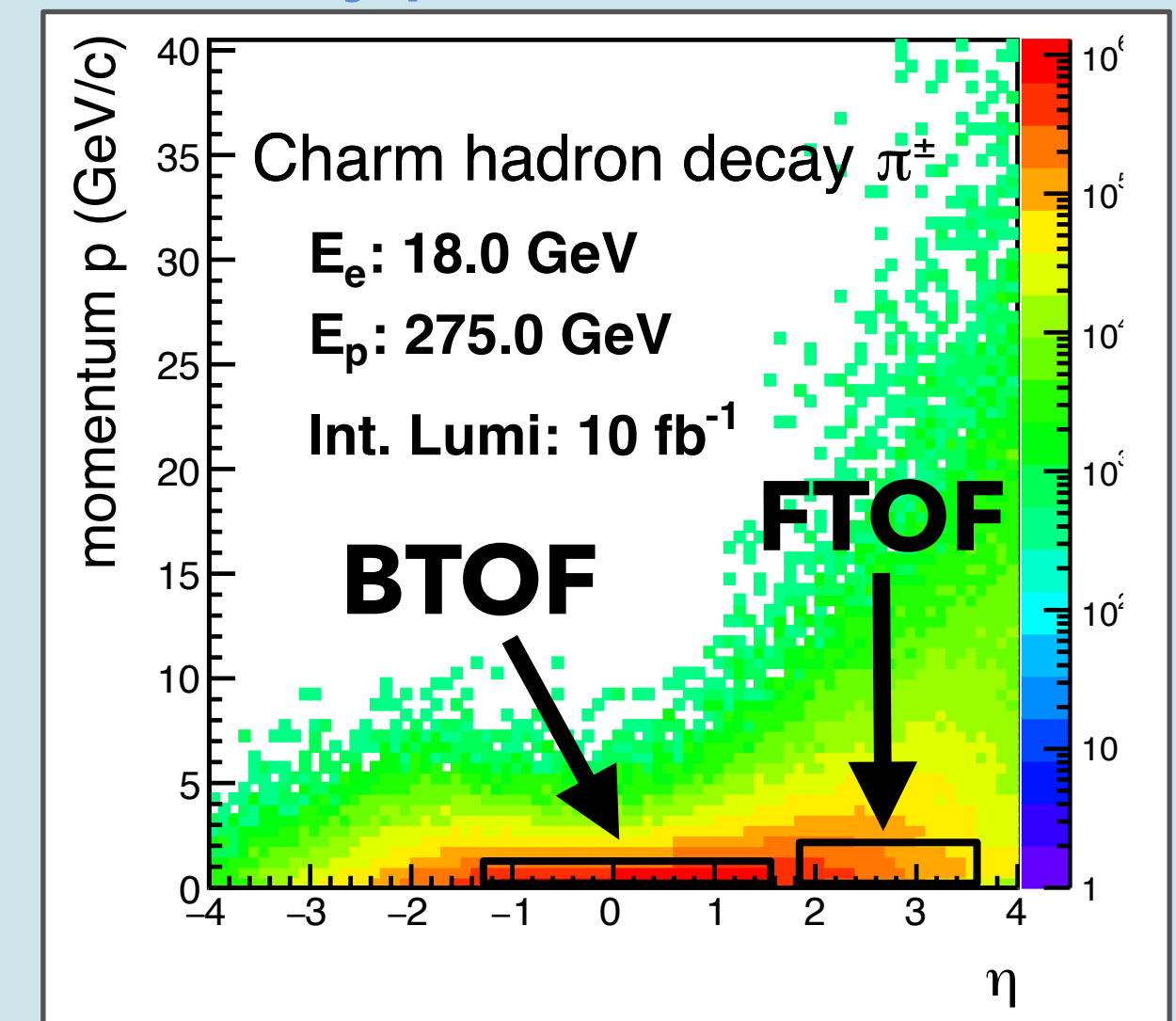
- BTOF covers midrapidity and FTOF covers forward rapidity
 - BTOF and FTOF cover $-1.42 < \eta < 1.77$ and $1.86 < \eta < 3.85$, respectively
- TOF has been assigned many important roles
 - Low p region PID at $p < 1.5$ GeV/c and $p < 2.5$ GeV/c for BTOF and FTOF, respectively with excellent timing information
 - Tracking with excellent spatial resolution
 - Machine-induced background rejection
- AC-LGAD is the most promising technology for TOF
 - High-timing resolution $\sigma_t = \sim 30$ ps
 - High-spatial resolution $\sigma_{xy} = \sim 30$ μ m
 - Space-saving design $\Delta D < 10$ cm
 - **but... no experiments have been used so far...**

TOF is one of the most important detectors for ePIC and also the most challenging detector.

Detectors for PID

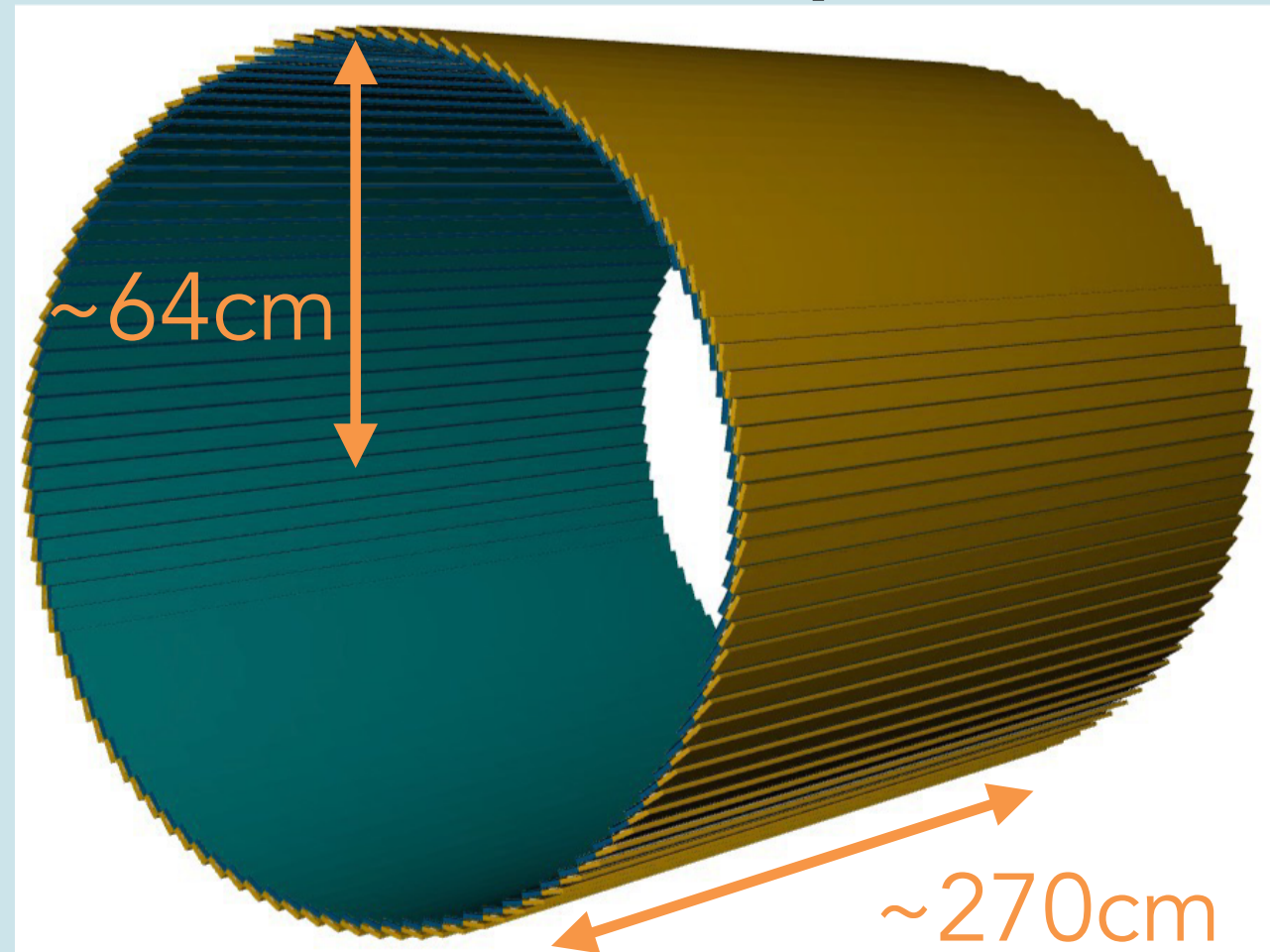


Decay particle kinematics

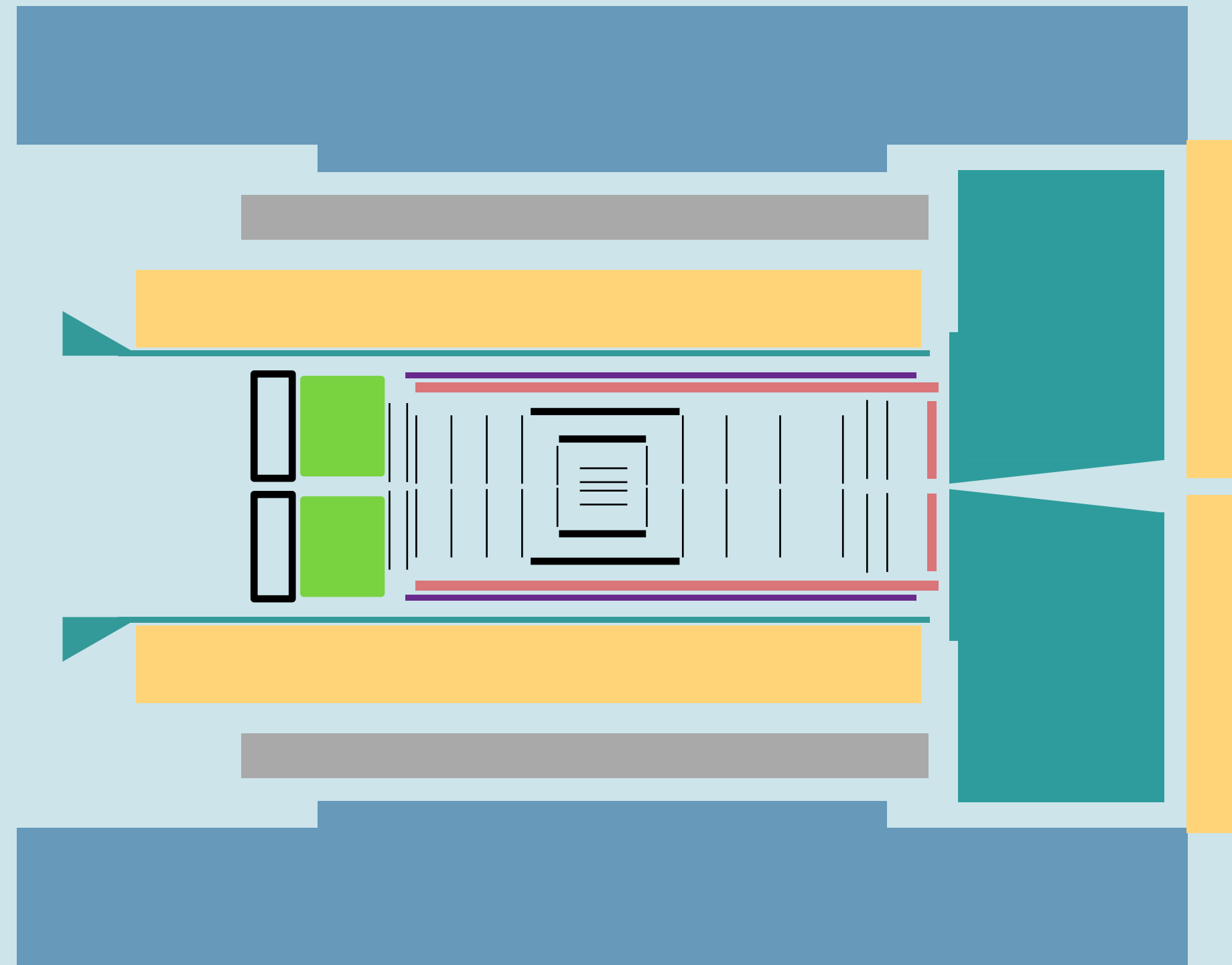
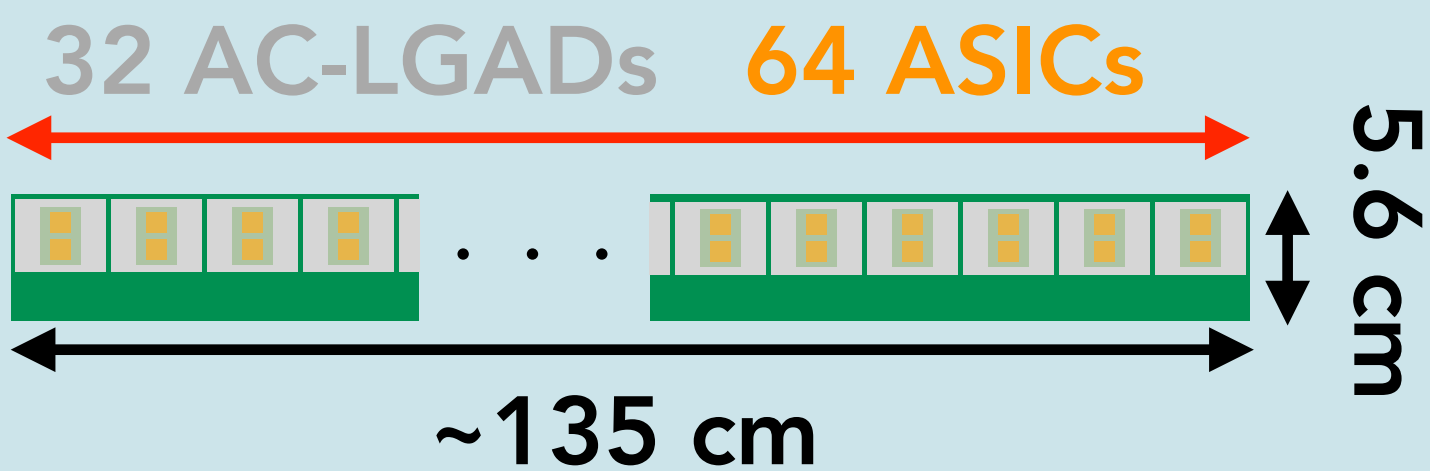


Recap of BTOF and FTOF

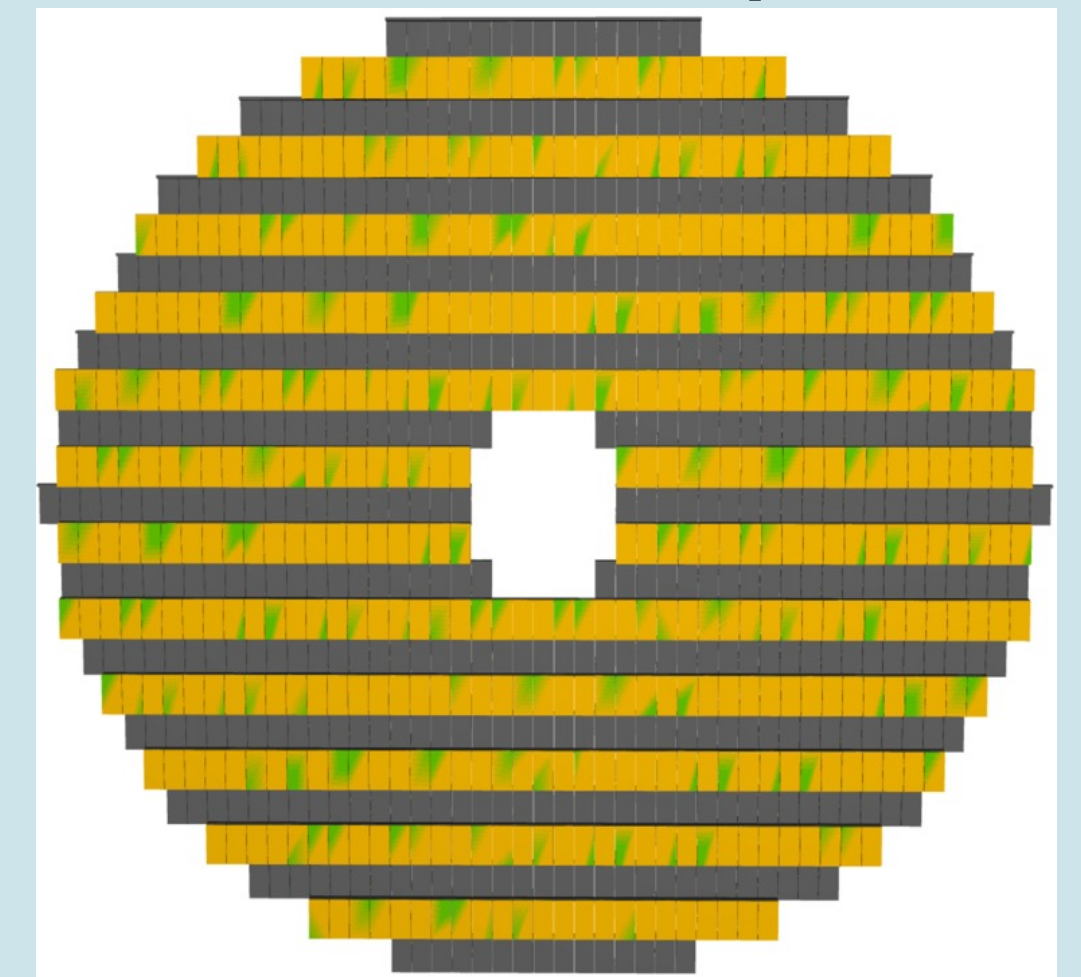
BTOF shape



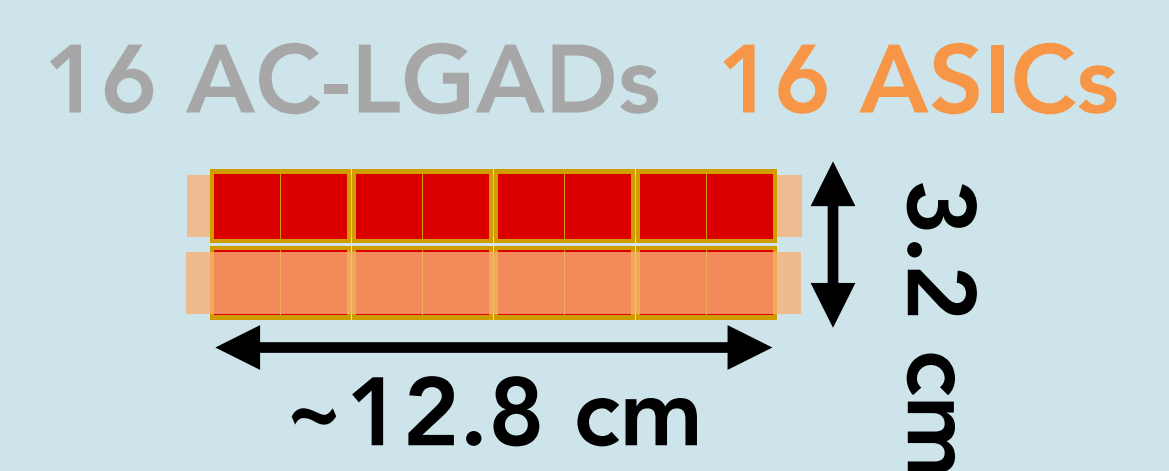
BTOF half Stave



FTOF shape



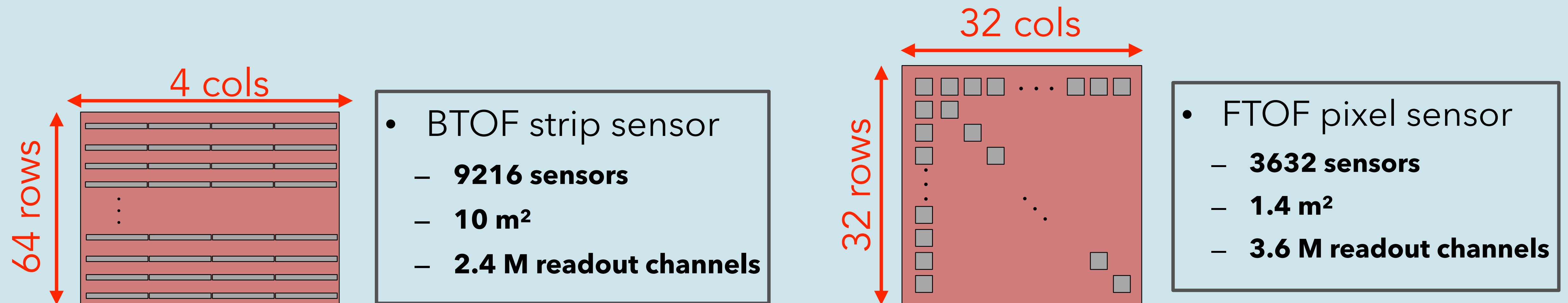
FTOF Module



- Strip-type and pixel-type AC-LGAD are used for BTOF and FTOF, respectively
- Different ASICs are used for BTOF and FTOF due to different sensor properties

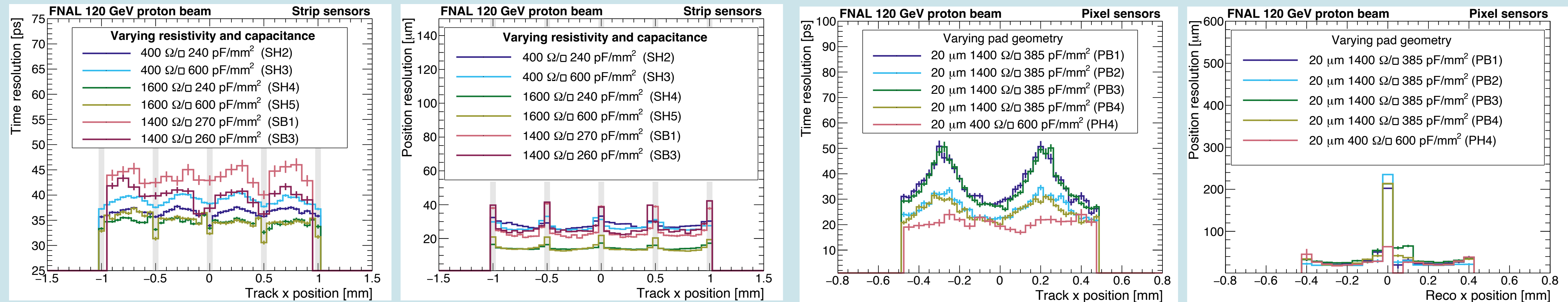
AC-LGAD for BTOF and FTOF

- **Strip-type** sensor, $3.2 \times 4 \text{ cm}^2$ sensor size with $0.05 \times 1 \text{ cm}^2$ metals, is used in **BTOF**
- The readout metal geometry is 64×4 and 256 channels in total each
- 2 ASICs are attached to each sensor with wire bonding
- **Pixel-type** AC-LGAD sensor, $1.6 \times 1.6 \text{ cm}^2$ sensor size with $0.05 \times 0.05 \text{ cm}^2$ metals, is used in **FTOF**
- The readout metal geometry is 32×32 and 1024 channels in total each
- 1 ASIC (2D 32×32) is attached to the one sensor



Latest sensor performance

Beam test result at FNAL (from FY24 report by FNAL, LBNL and UIC)

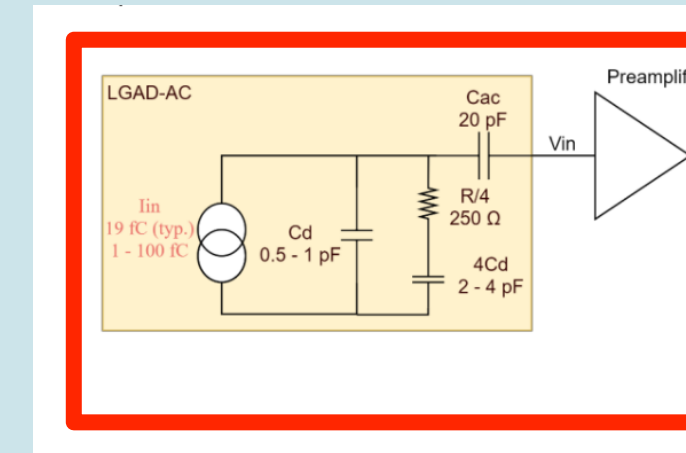


- HPK and BNL sensors show reasonable results in both strip and pixel types with the “BEST” bias voltage
 - Performance redundancy should be considered
- The performances are under control and the next prototypes will have higher performance
- The sensors are still smaller than the sensors used in the experiment
- The full-size sensors will be shipped in a few months and gain uniformity will be checked
- Sensor temperature dependence study is mandatory and ongoing

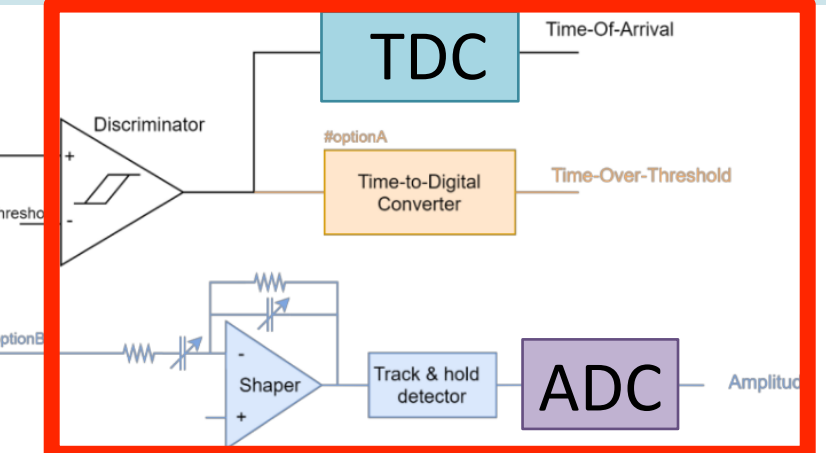
TOF ASIC

- EICROC (32x32 = 1024ch) is one of the common ASICs used in ePIC
 - Design suits to pixel-type AC-LGAD readout (for low input capacitance)
 - 10-bit TDC and 8-bit ADC is now available (EICROC0)

Analog block

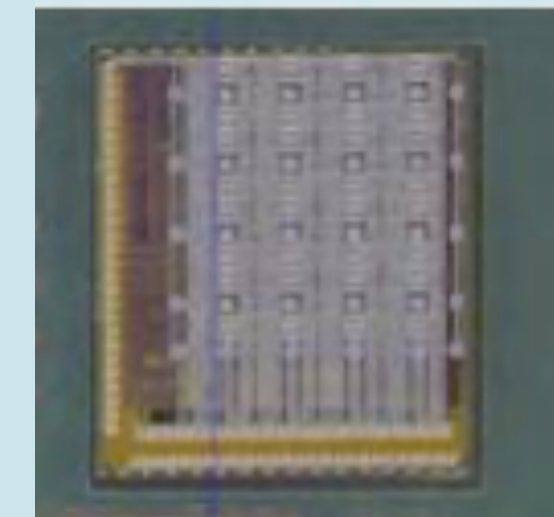


Digital block

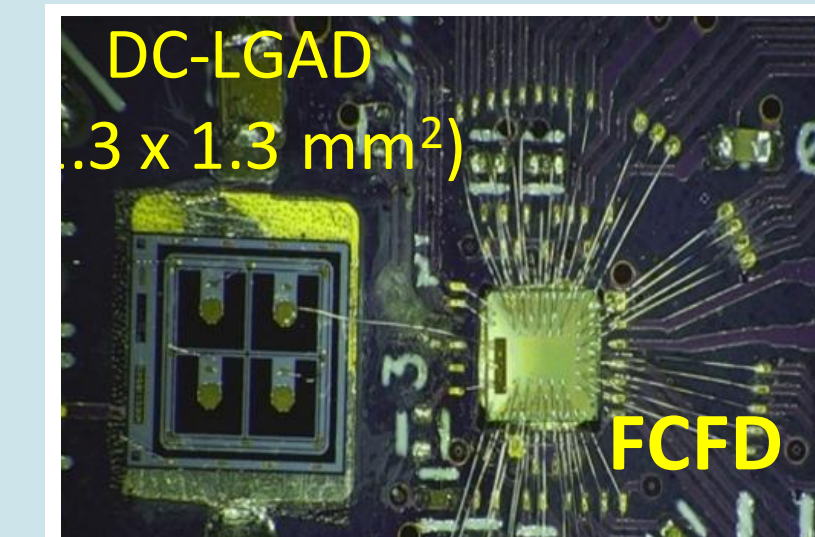


- We have several options for the strip-type AC-LGAD readout
 - The strip type has a large input capacitance of ~10 pF
 - “Standard” EICROC should be modified if it is used for the strip type
 - FCFD, HGCROC, and “Modified”-EICROC are the candidates
 - FCFDv1 with the analog block is available and FCFDv2 with digital block will be available beginning of next year
 - HGCROC has been developed for CMS Calorimeter and is ready
 - EICROC tuned for a larger input capacitance is being considered
- The possibility of third-party ASICs has begun to be discussed
 - ASROC and HPSoC are one of the options

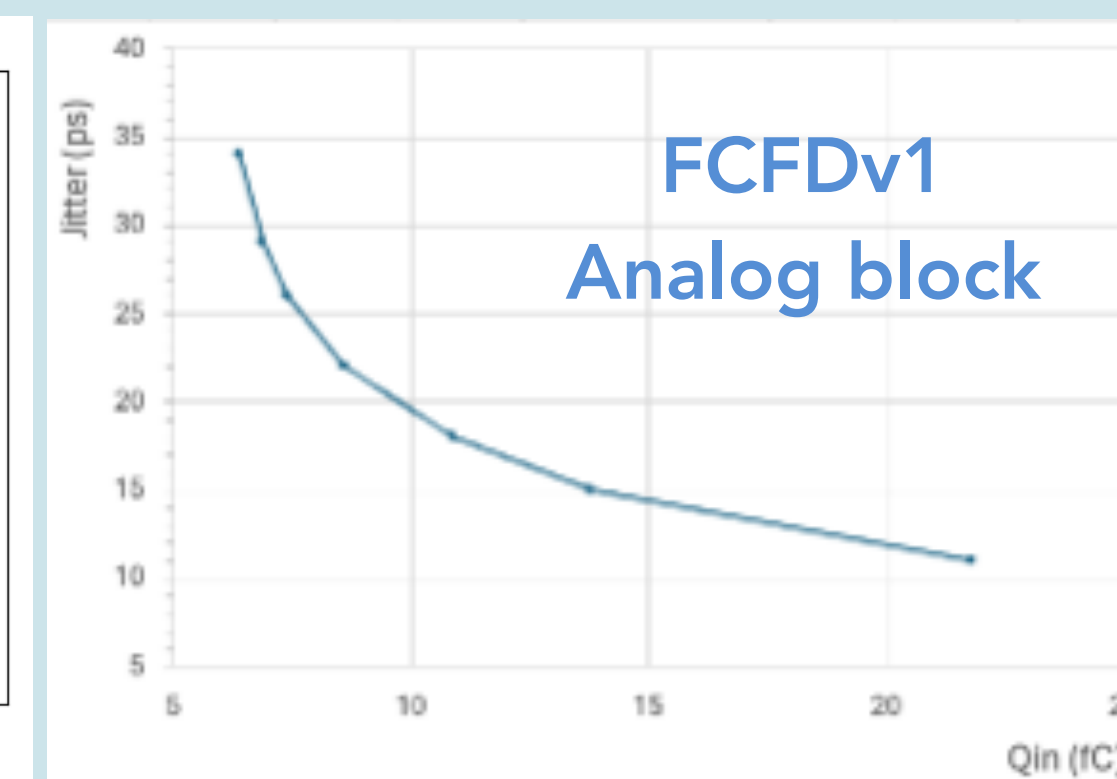
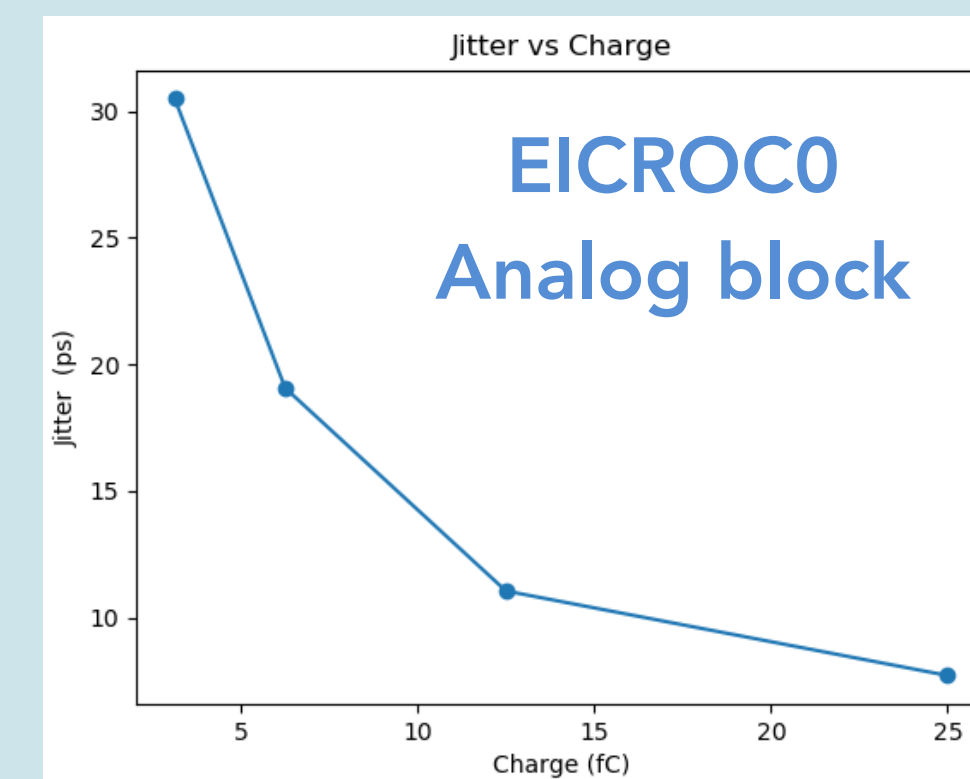
EICROC0



FCFDv1

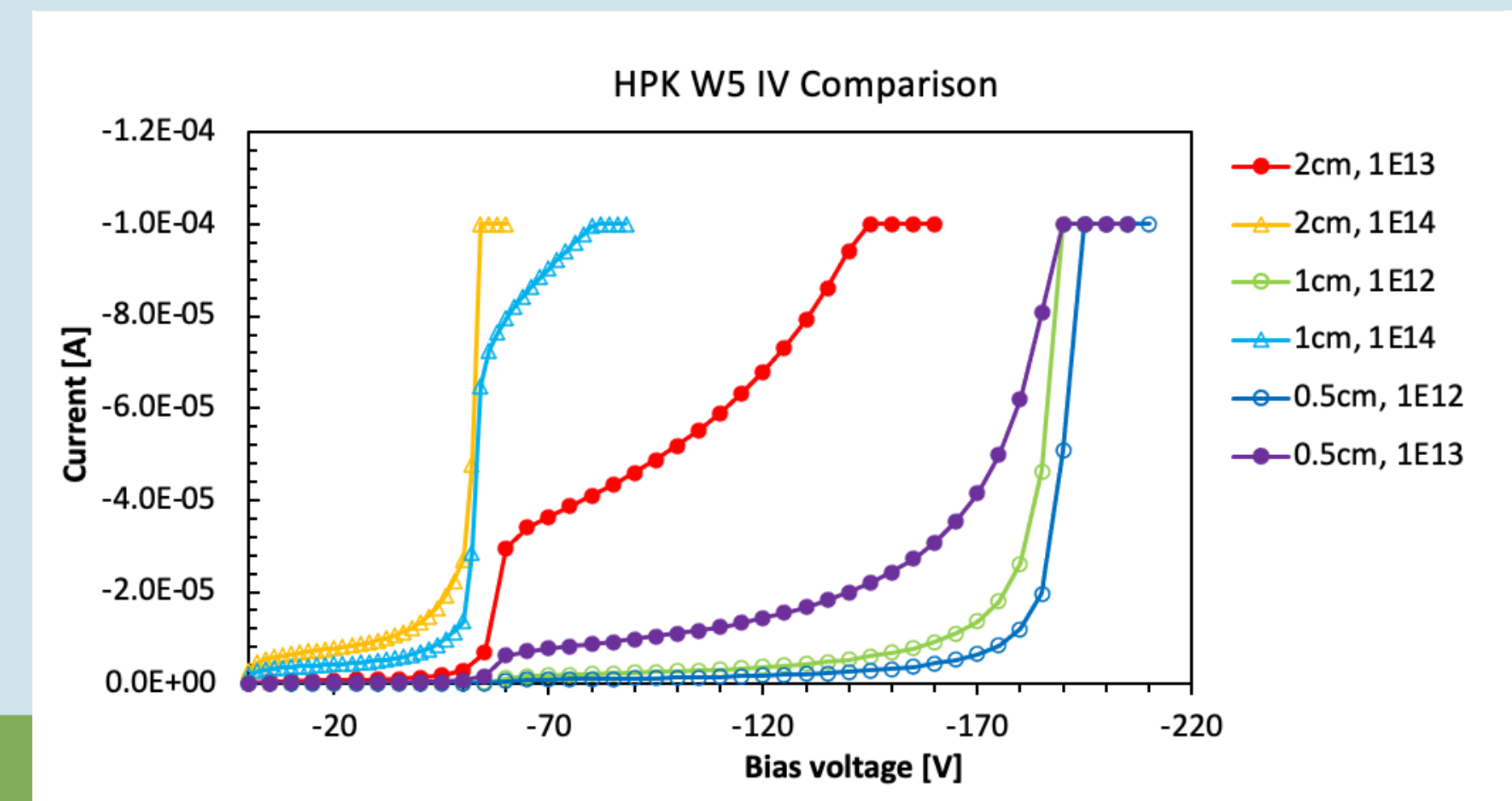
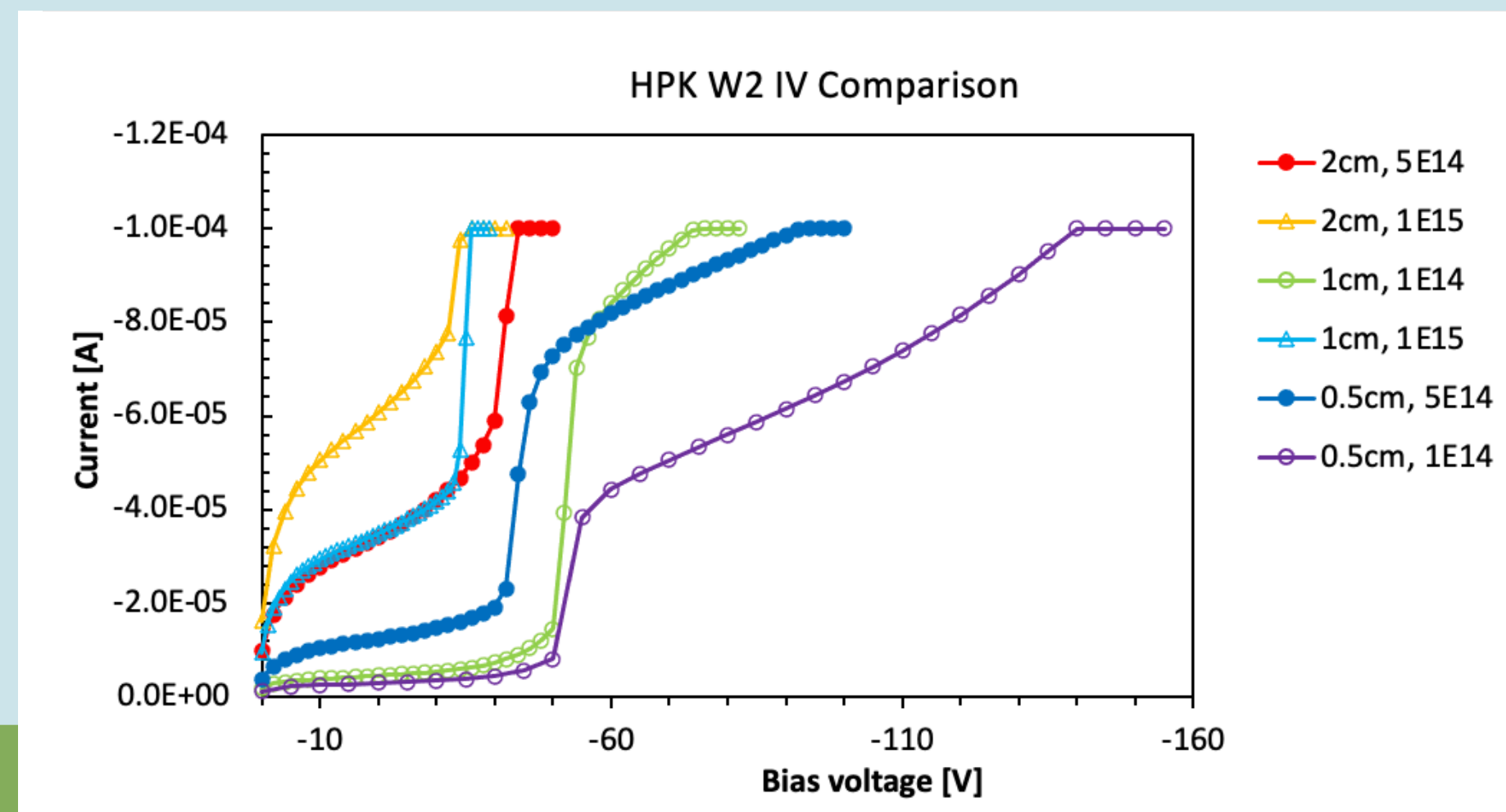
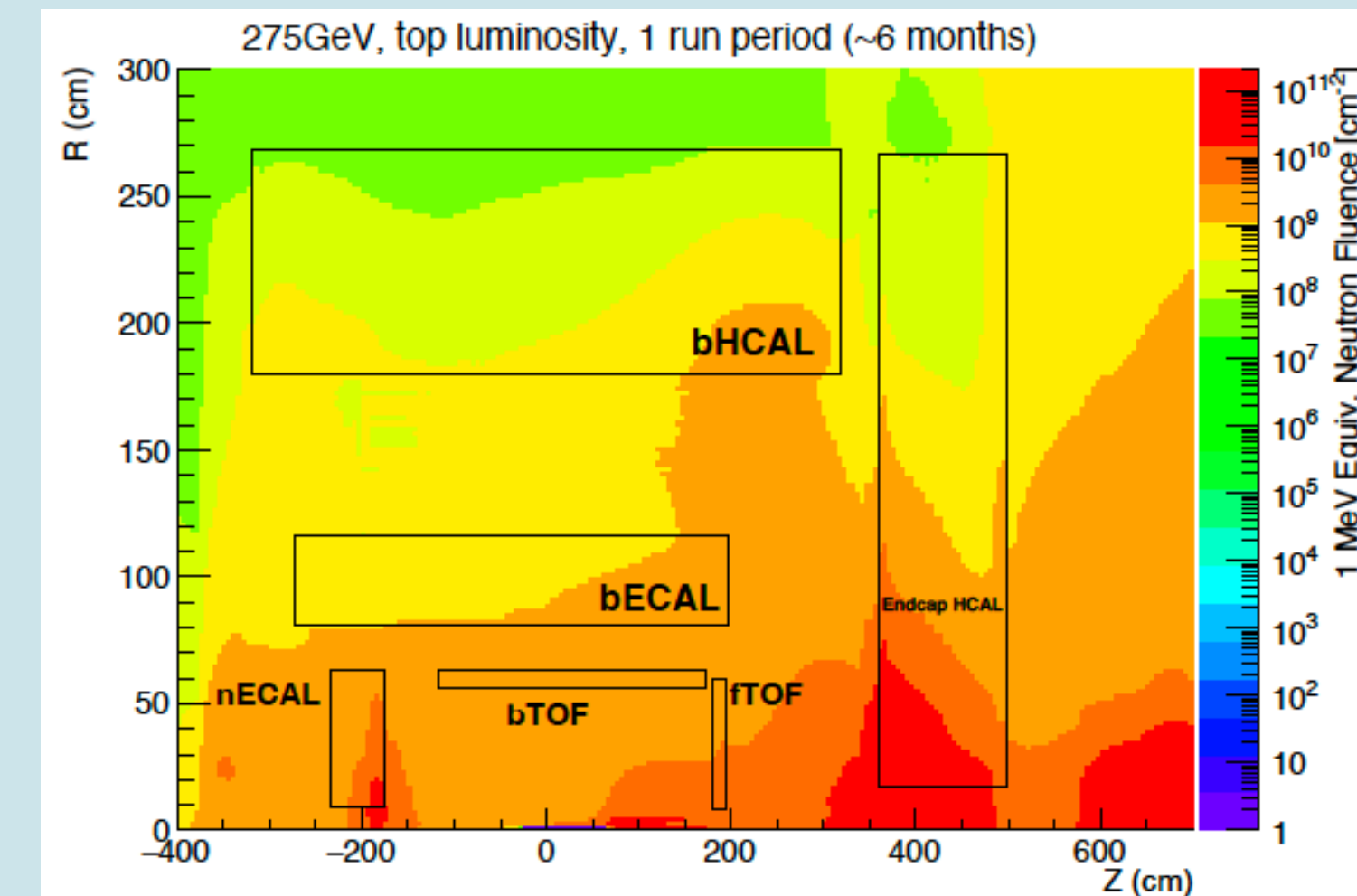


HGCROC3



Sensor irradiation test

- Not very large radiation is expected at both BTOF and FTOF (10^9 - $10^{10}n_{eq}/cm^2$)
- Irradiation test of strip sensor has been done at IJS with 1 MeV neutron
- All devices were annealed for 80 min at $60^\circ C$ to avoid rapid change in sensor behavior
- Testing done at room temperature with a probe station, the current is higher for high irradiation devices
- The irradiation effects should be corrected in the experiment



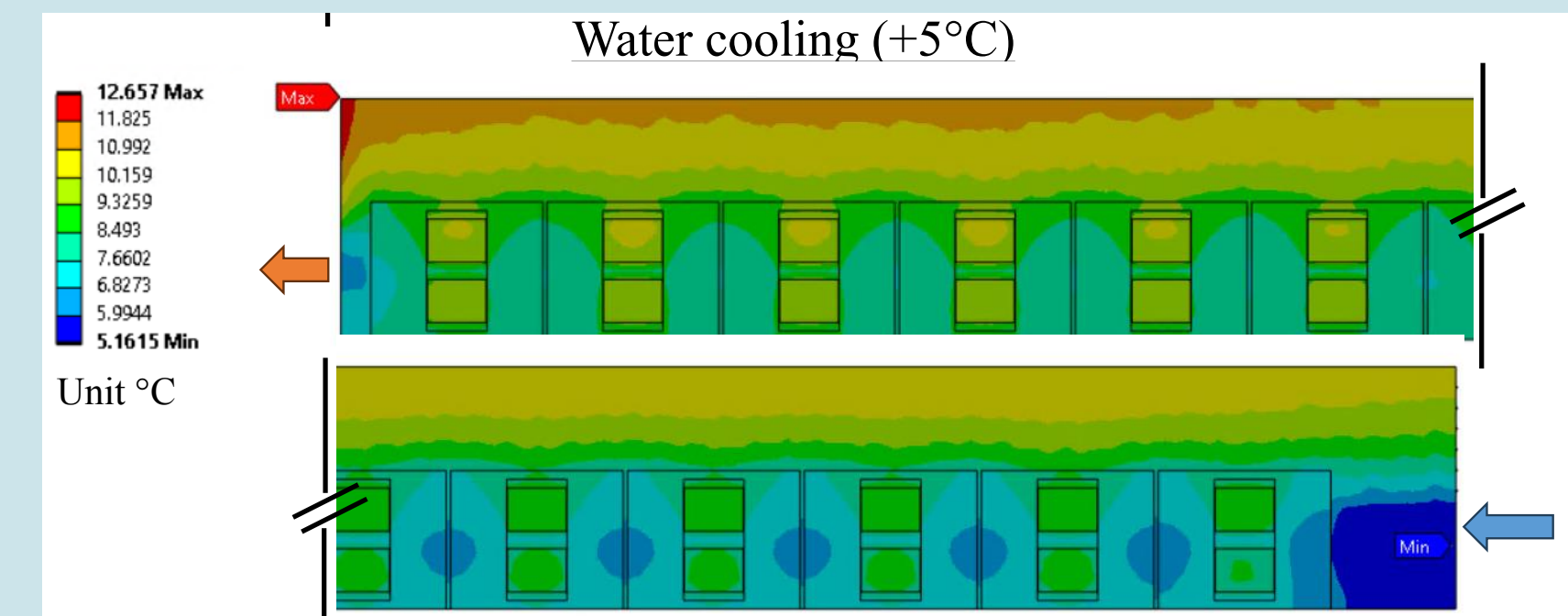
Support structure and temperature control

- BTOF consists of long staves with a lower material support structure than ever before
- Low material (1% X/X₀) long FPC design requires a high-level technology and imposes significant limitations on functionality
 - sPHENIX INTT team has the experience of making such a long FPC
- The thermal conductivity of the stave is under investigation
 - Full-size stave (270 cm) thermal conductivity is being studied with simulation
 - Mini-size support structure (30 cm) thermal conductivity is being studied under several conditions
 - Middle-size support structure (100 cm) is available now and the results will be out soon

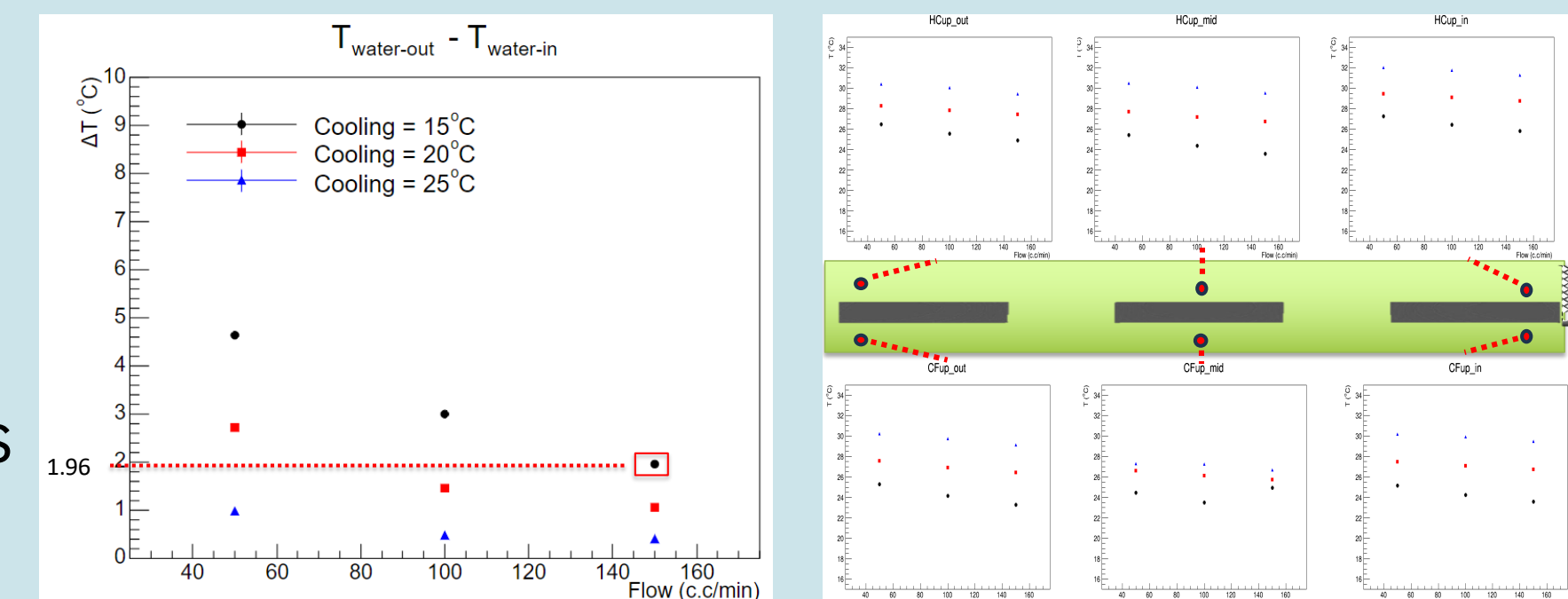
sPHENIX INTT FPC



Full-size stave test with simulation



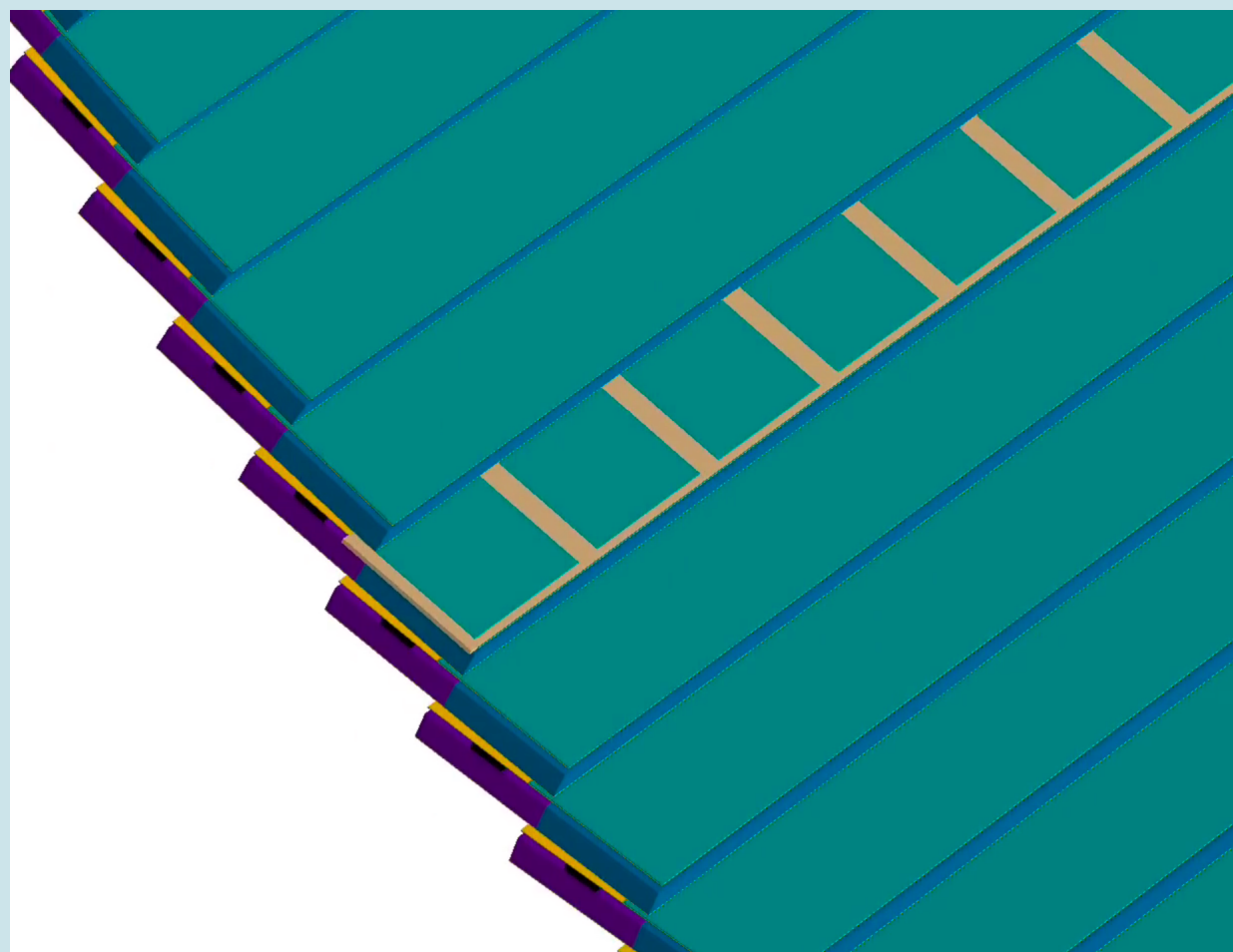
Mini-size stave test results



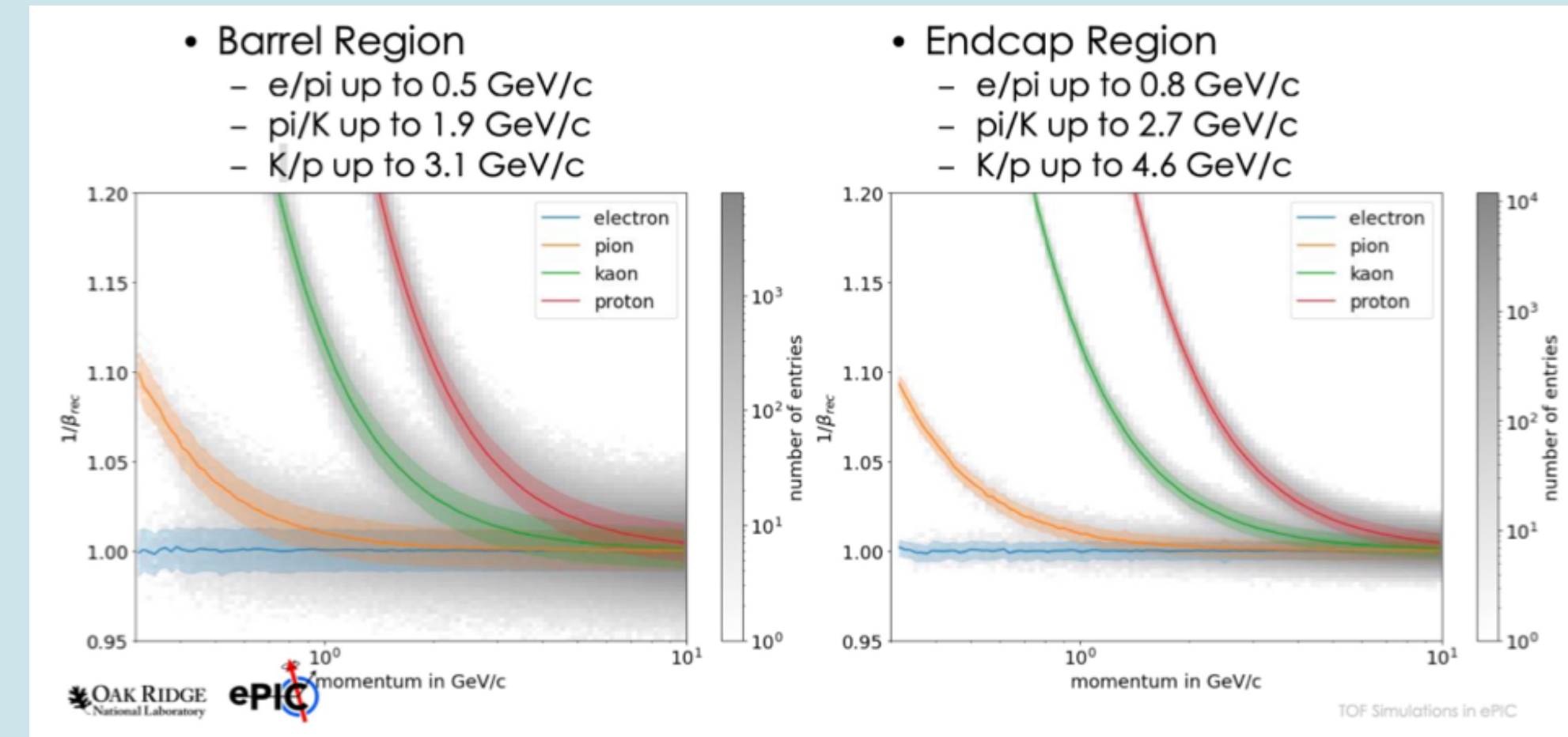
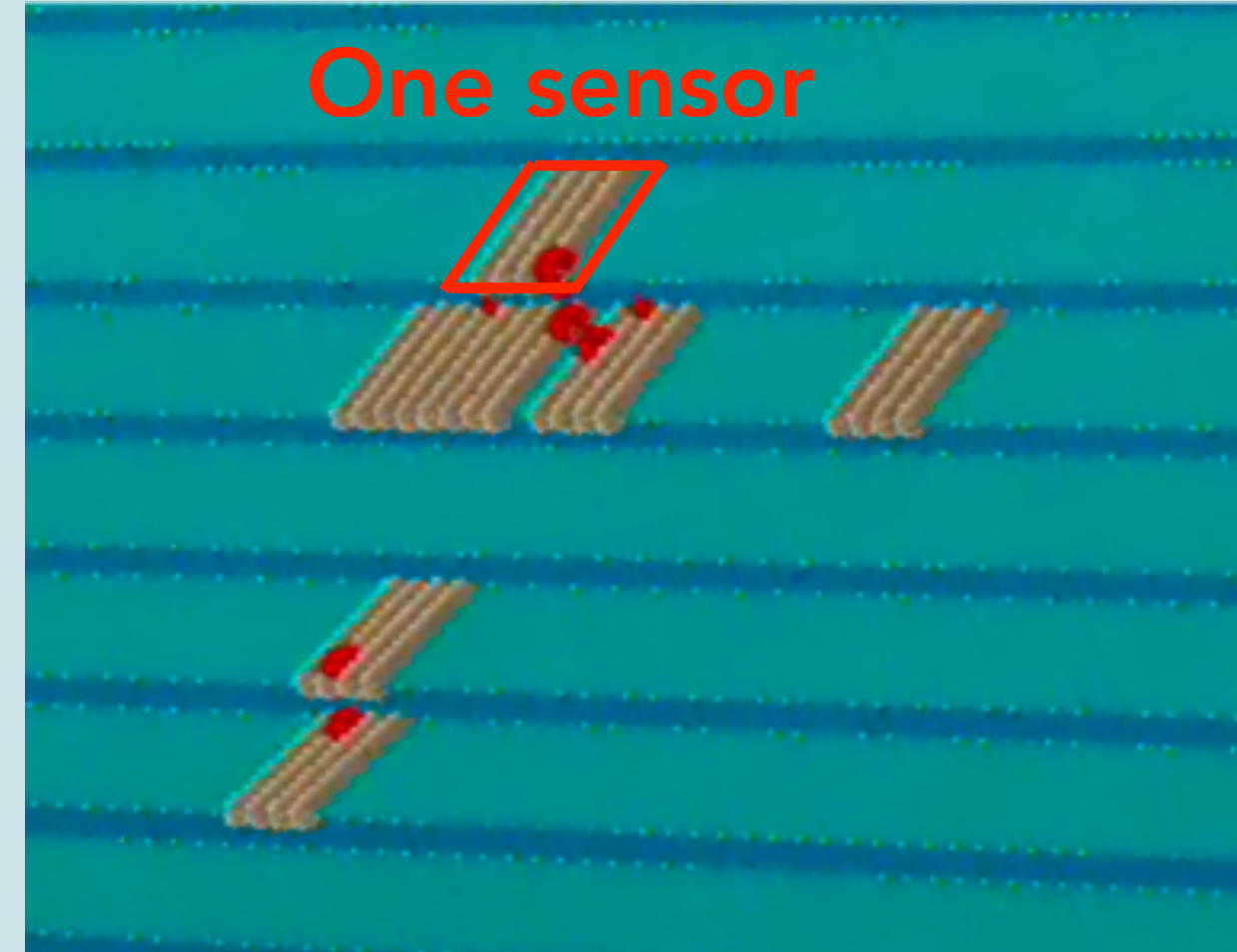
Simulation development

- The LUT PID has been implemented into the official simulation
- More realistic sensor segmentation is being implemented in the simulation
- Digitization mimicking charge sharing has been implemented in the simulation
- Material budget effect on the outer detectors by BTOF is under evaluation

Sensor segment



Readout metal visualization



RawTrackerHitCollection

- Energy deposited
 - Time of Flight
 - Cell ID
- rawhits

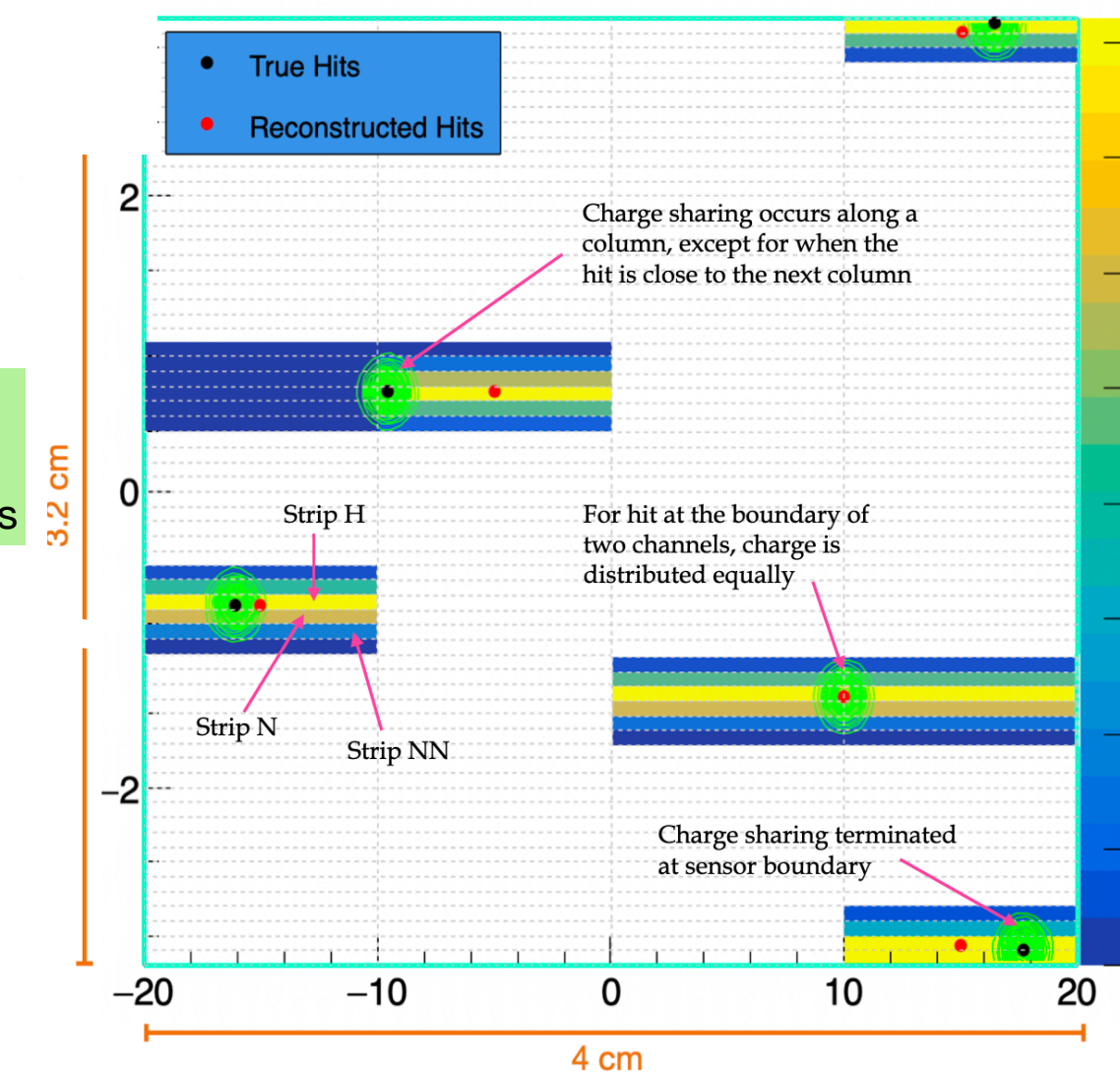
Analog signal generation

Reference clock
Delay cells
Threshold voltages

BTOFHitDigi (on git but not main branch)

Resides in [EICrecon/src/detectors/BTOF](#)

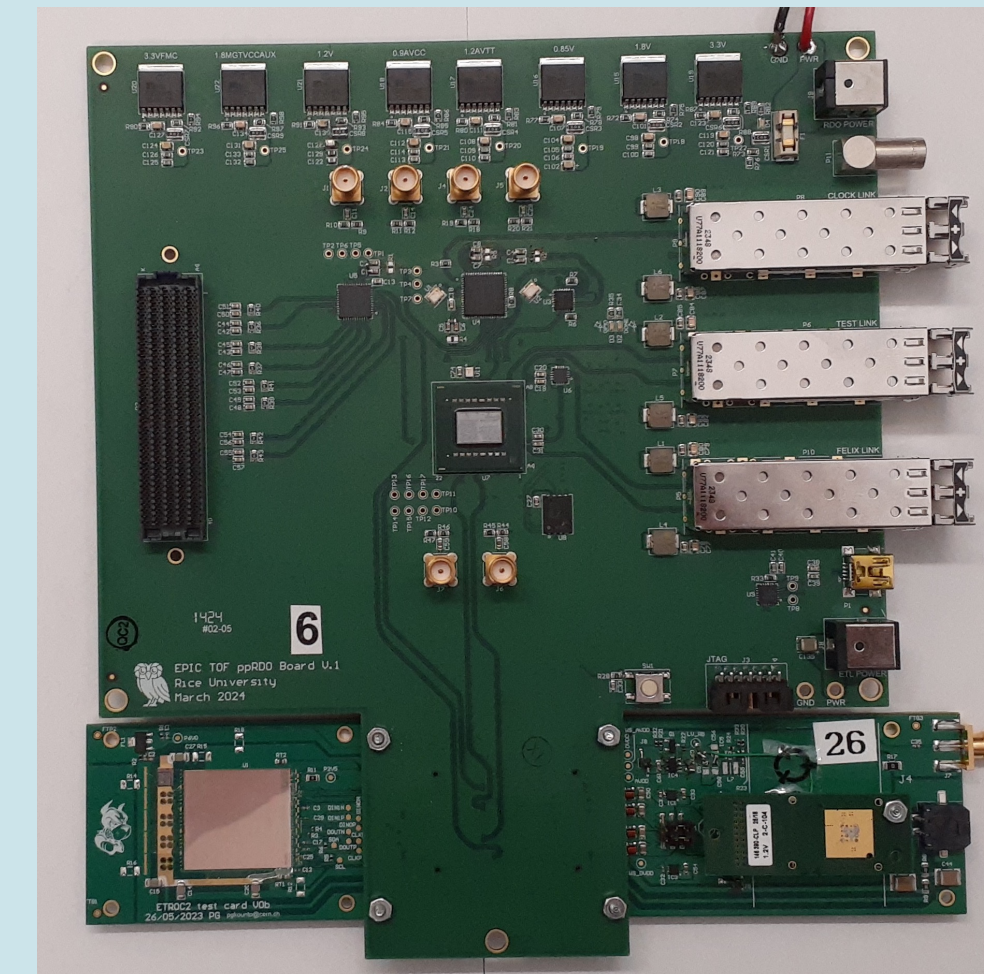
- ADC (8-bit)
 - TDC (10-bit)
 - Cell ID
 - Sensor ID
- digi



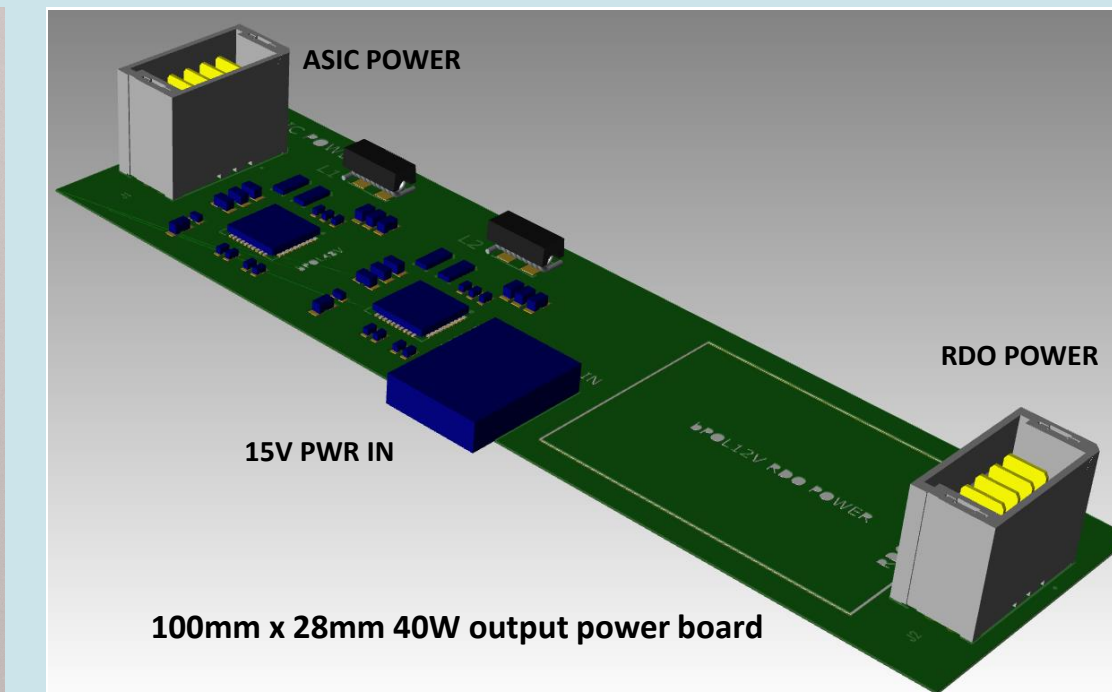
Front-end electronics

- Pre-prototype readout board (ppRDO) has been made with ETROC2 ASIC
 - 6 boards are available
- Several tests are ongoing
 - FPGA firmware development
 - Readout test with ETROC2
 - Evaluation of power consumption
- Power board (PB) design is ongoing
 - PB supplies 5 different voltages
 - ASIC: 1.2 V (EICROC case)
 - FPGA: 1.8, 1.2, 0.9, 0.85 V
 - SFP+: 3.3 V
 - Several options for DC-DC converters are being tested

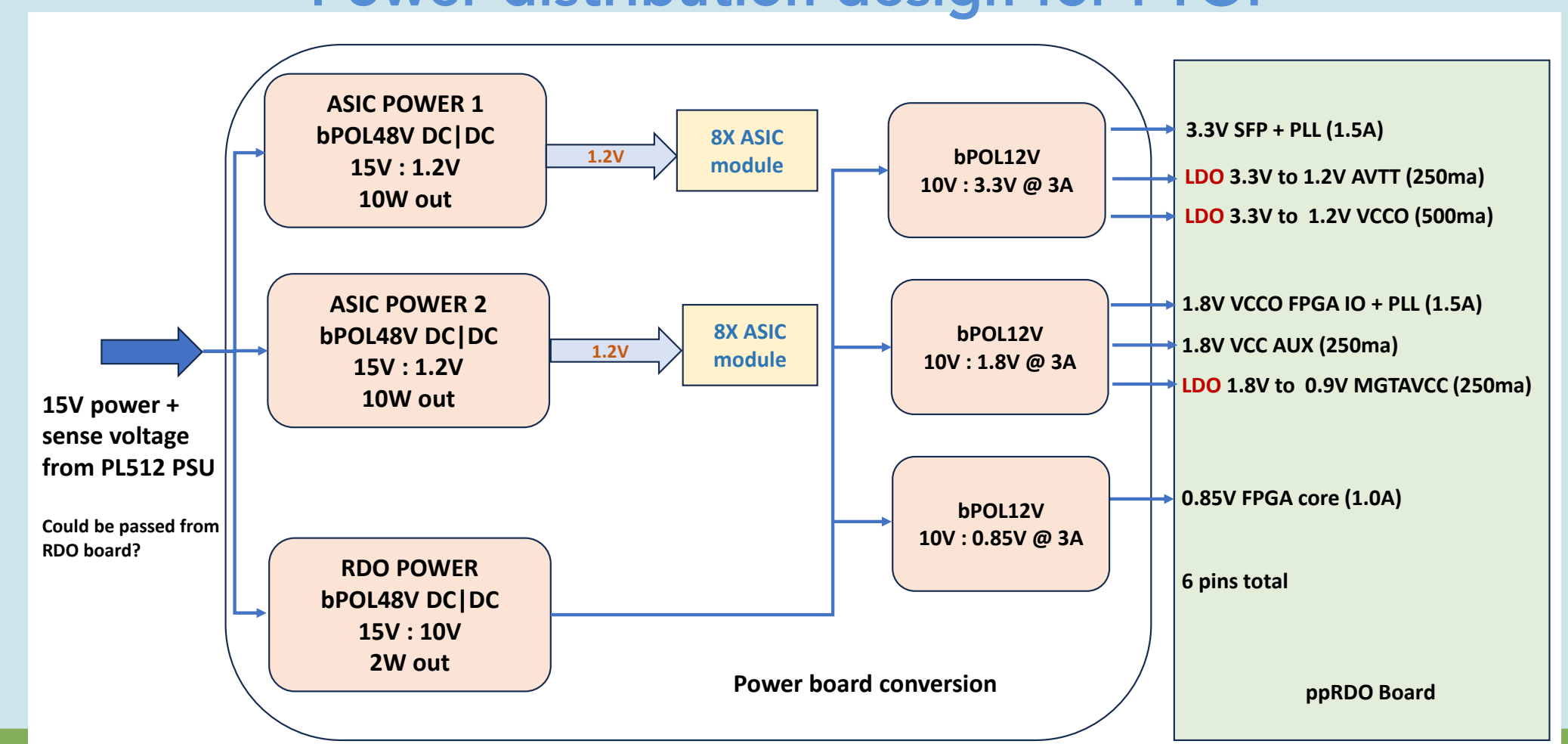
ppRDO



PB design



Power distribution design for FTOF



Summary

- AC-LGAD TOF is the key detector in the ePIC project for the PID at low p region and background rejection
- Prototypes of BNL and HPK fulfill the requirements, but it is under the BEST environment
 - Breakdown voltage is expected to depend on the temperature strongly
 - Performance redundancy should be considered
 - The first irradiation test with strip sensors has been done
- ASIC analog part performance of EICROC and FCFD meet the requirement
 - Not only ASIC but also AC-LGAD sensor + ASIC performance must be evaluated in the coming year
- Support structure thermal properties are being investigated with a 30 cm-long prototype
 - The first 100 cm prototype will be tested soon
- The prototype RDO is available and being tested with ETROC2

TOF project is making steady progress!







Backup slides

Institutes in TOF tasks (official)

- Brookhaven National Laboratory (USA)
- Fermi National Accelerator Laboratory (USA)
- Rice University (USA)
- Oak Ridge National Laboratory (USA)
- Ohio State University (USA)
- Purdue University (USA)
- University of California Santa Cruz (USA)
- University of Illinois at Chicago (USA)
- Hiroshima University (JP)
- RIKEN (JP)
- Shinshu University (JP)
- Nara Woman University (JP)
- National Chen-Kung University (TW)
- National Taiwan University (TW)
- IJCLab, OMEGA, CEA-Saclay (FR)

Tasks in BTOF






• AC-LGAD sensor

-  BNL
-  ORNL
-  Univ. of California, Santa Cruz
-  Univ. of Illinois, Chicago
-  Hiroshima University
-  Shinshu University


• Frontend ASIC

-  Fermilab
-  Rice University
-  ORNL
-  Hiroshima University
-  National Taiwan University
-  IJCLab/OMEGA/CEA-Saclay









• Sensor-ASIC integration

-  BNL
-  ORNL
-  Univ. of California, Santa Cruz
-  Univ. of Illinois, Chicago
-  National Taiwan University

• Module structure

-  Purdue University
-  National Cheng-Kung University

• Module assembly

-  BNL
-  ORNL
-  Ohio State University
-  Univ. of California, Santa Cruz
-  Hiroshima University
-  RIKEN
-  Nara Woman University
-  National Taiwan University

• Flex PCB

-  ORNL
-  Nara Woman University

• Service Hybrid

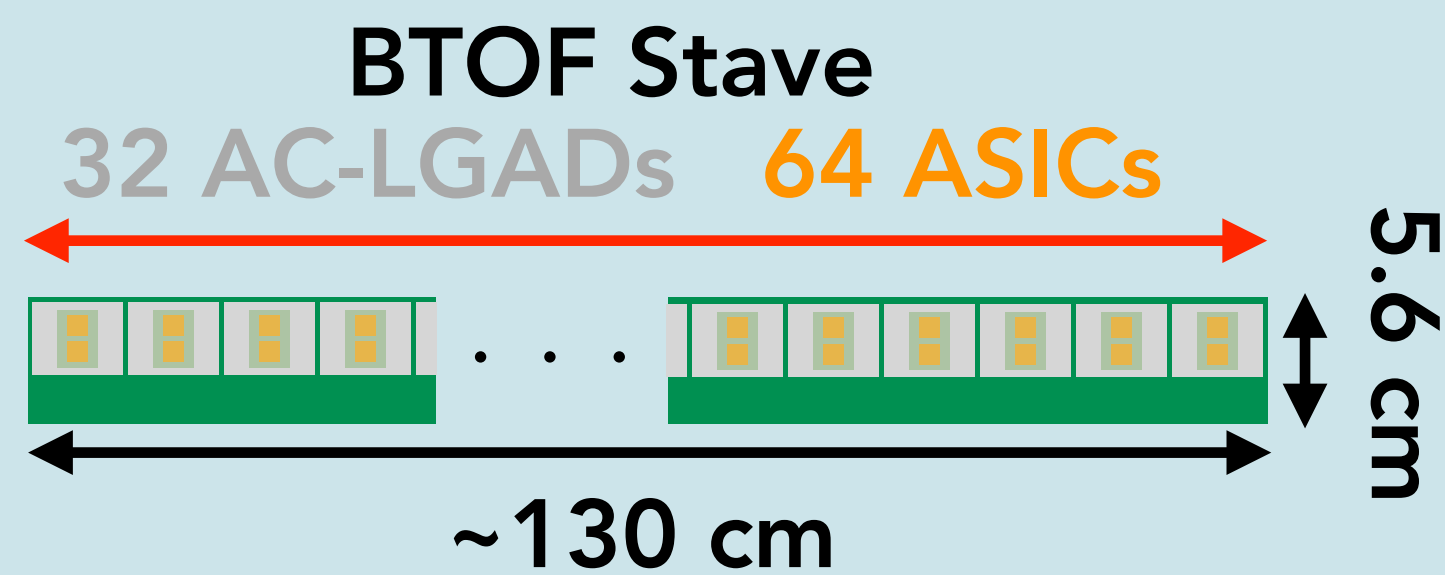
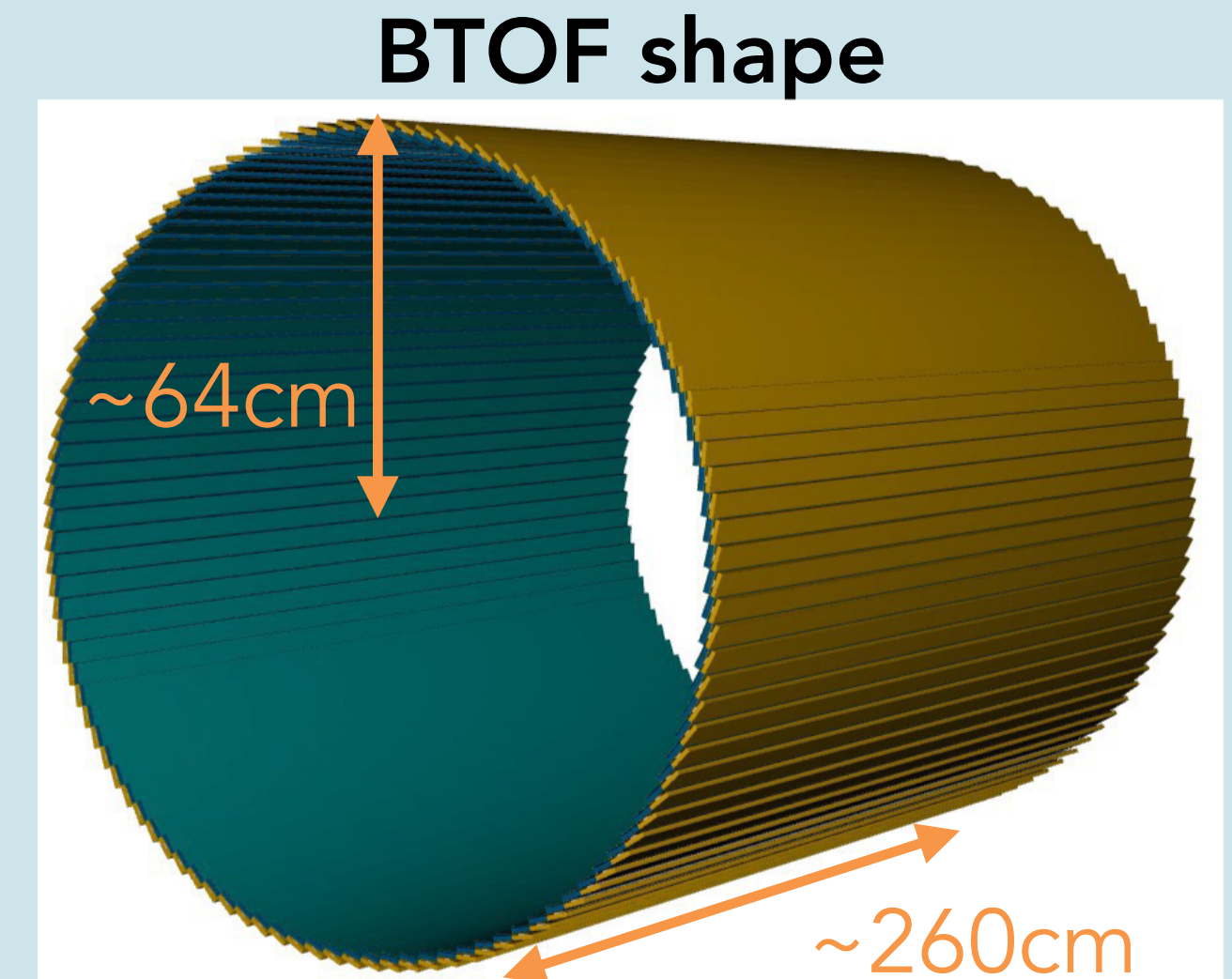
-  Rice University

• Backend electronics

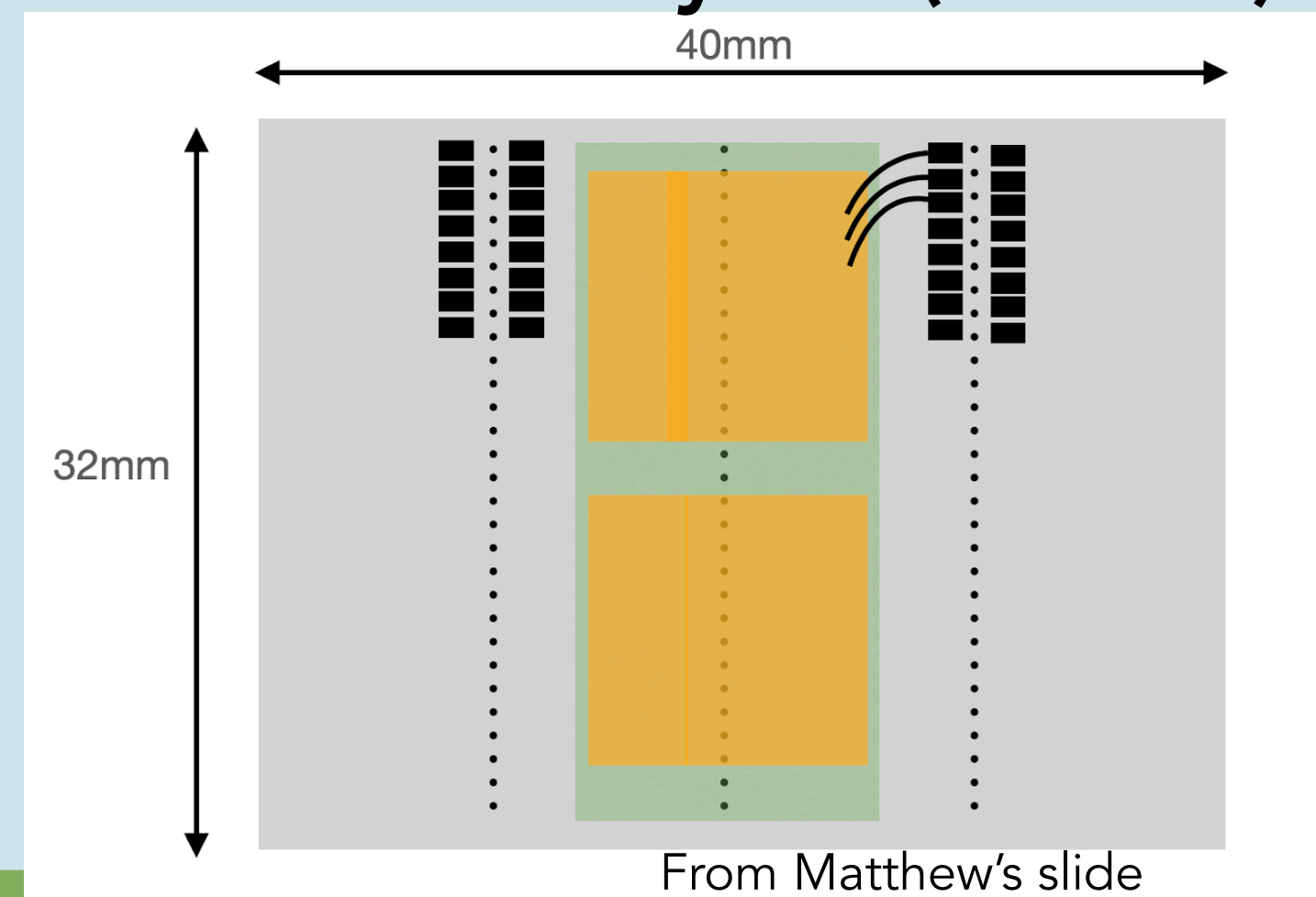
-  BNL

Detector Layout of BTOF

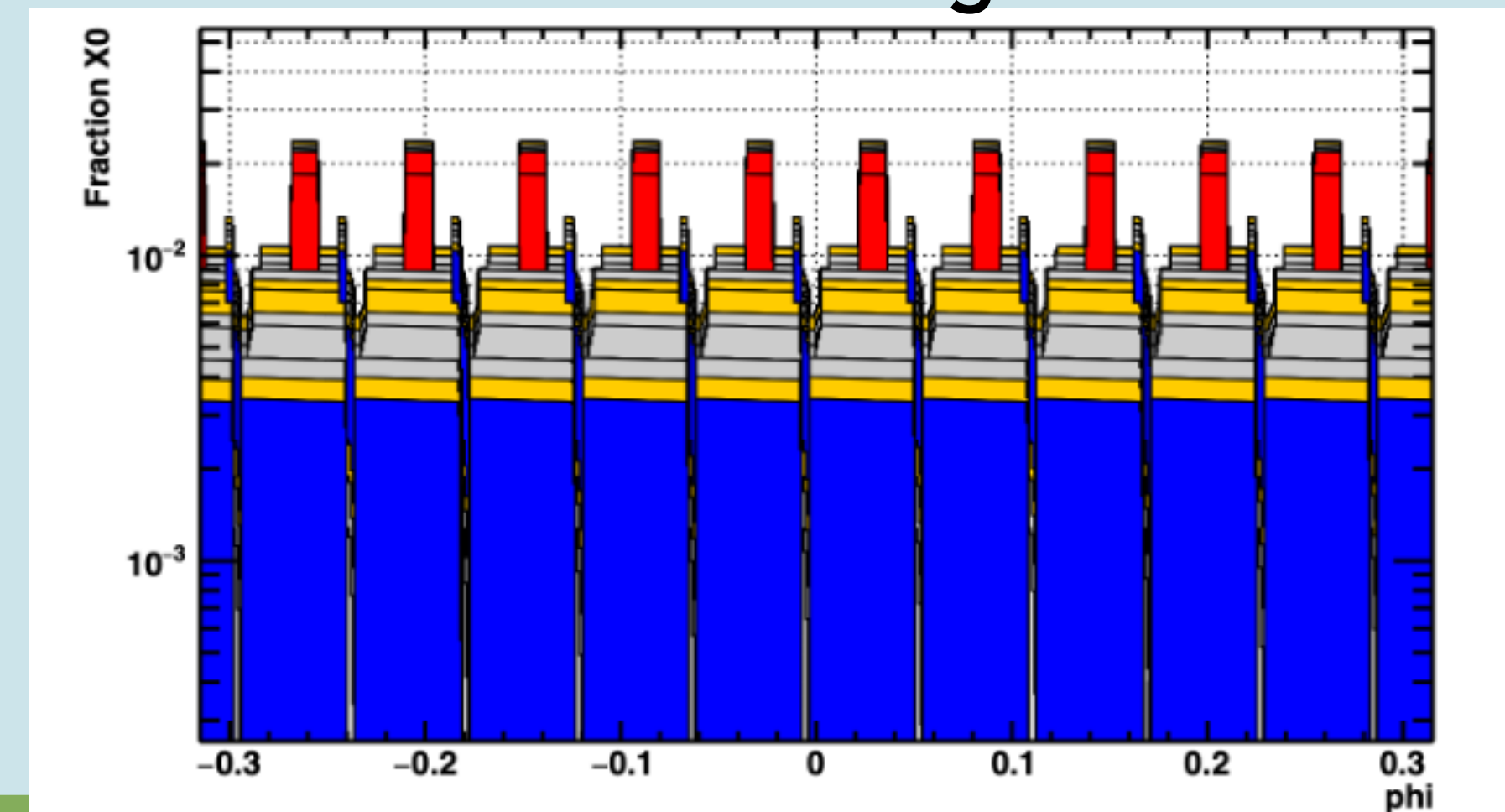
- BTOF is composed of 288 (2x144) staves to form a cylindrical shape
- 32 AC-LGAD **strip-type** sensors are attached to one stave
 - Two ASICs are placed just above one sensor
- Radius is 63 - 66 cm from the beam pipe covering $-1.42 < \eta < 1.77$
- Total material budget in acceptance is $\sim 0.01 X/X_0$



Sensor-ASIC hybrid (module)



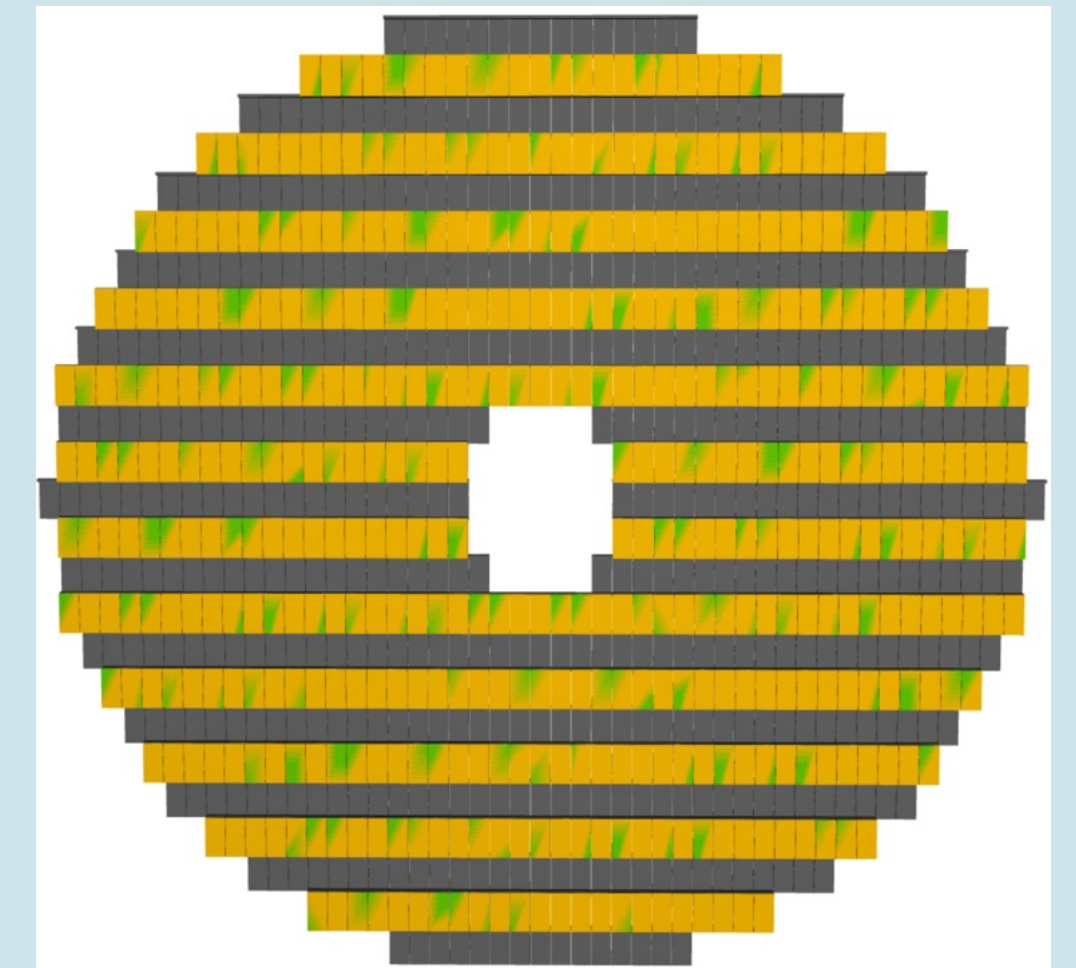
Material budget



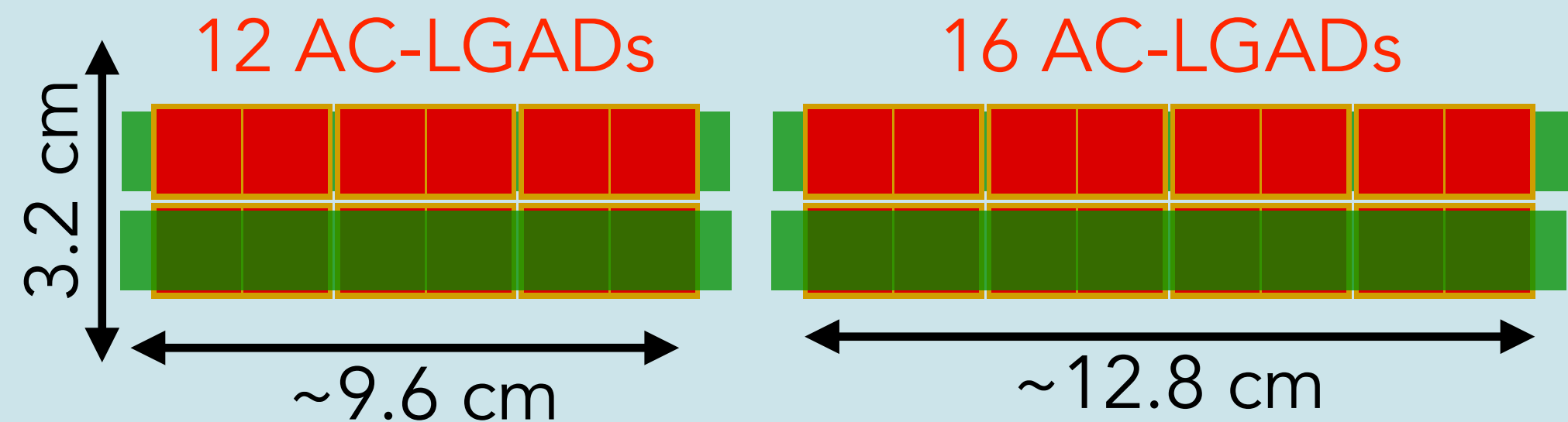
Detector Layout of FTOF

- FTOF is composed of 1816 modules to make a disk
- 12 or 16 AC-LGAD **pixel-type** sensors are attached to one module
 - One ASIC is used for one sensor
- Radius is 10.5 - 60 cm from the beam pipe covering $1.86 < \eta < 3.85$
- Service hybrid, readout board + power board, is placed in the acceptance
- Total material budget in acceptance is $\sim 0.05 X_0$

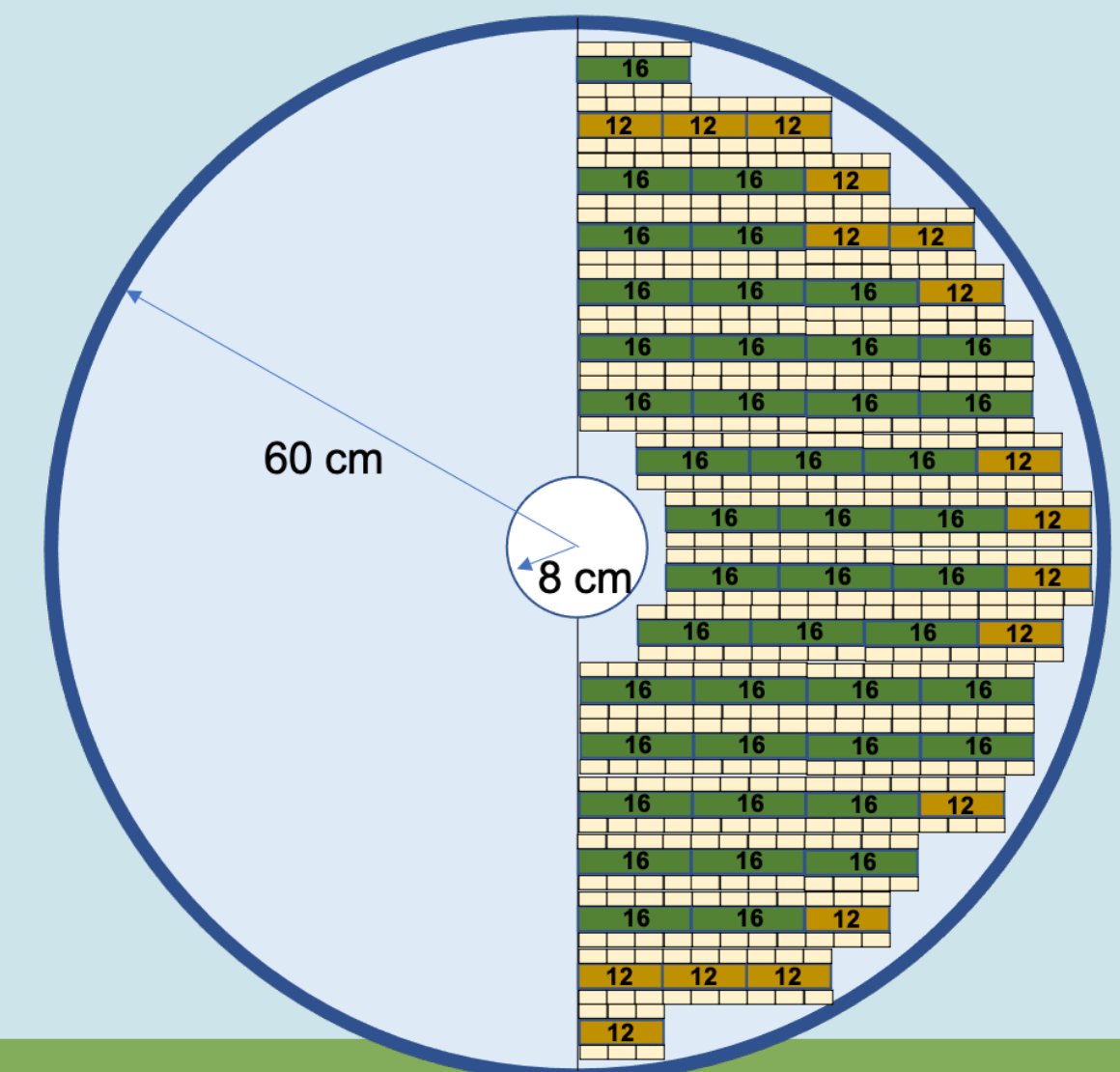
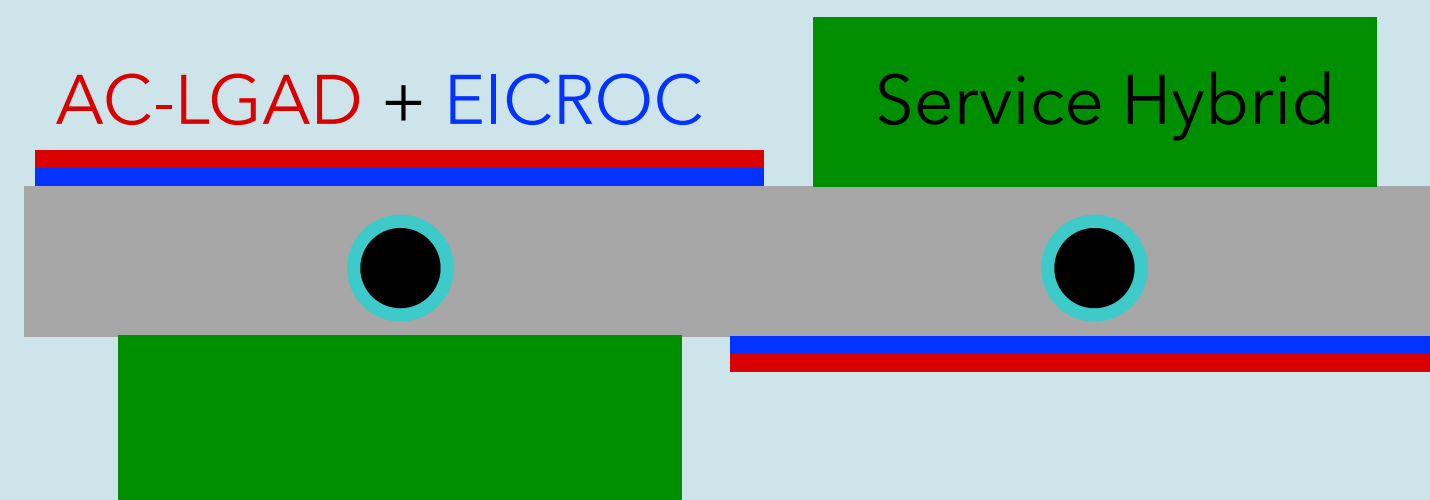
FTOF shape



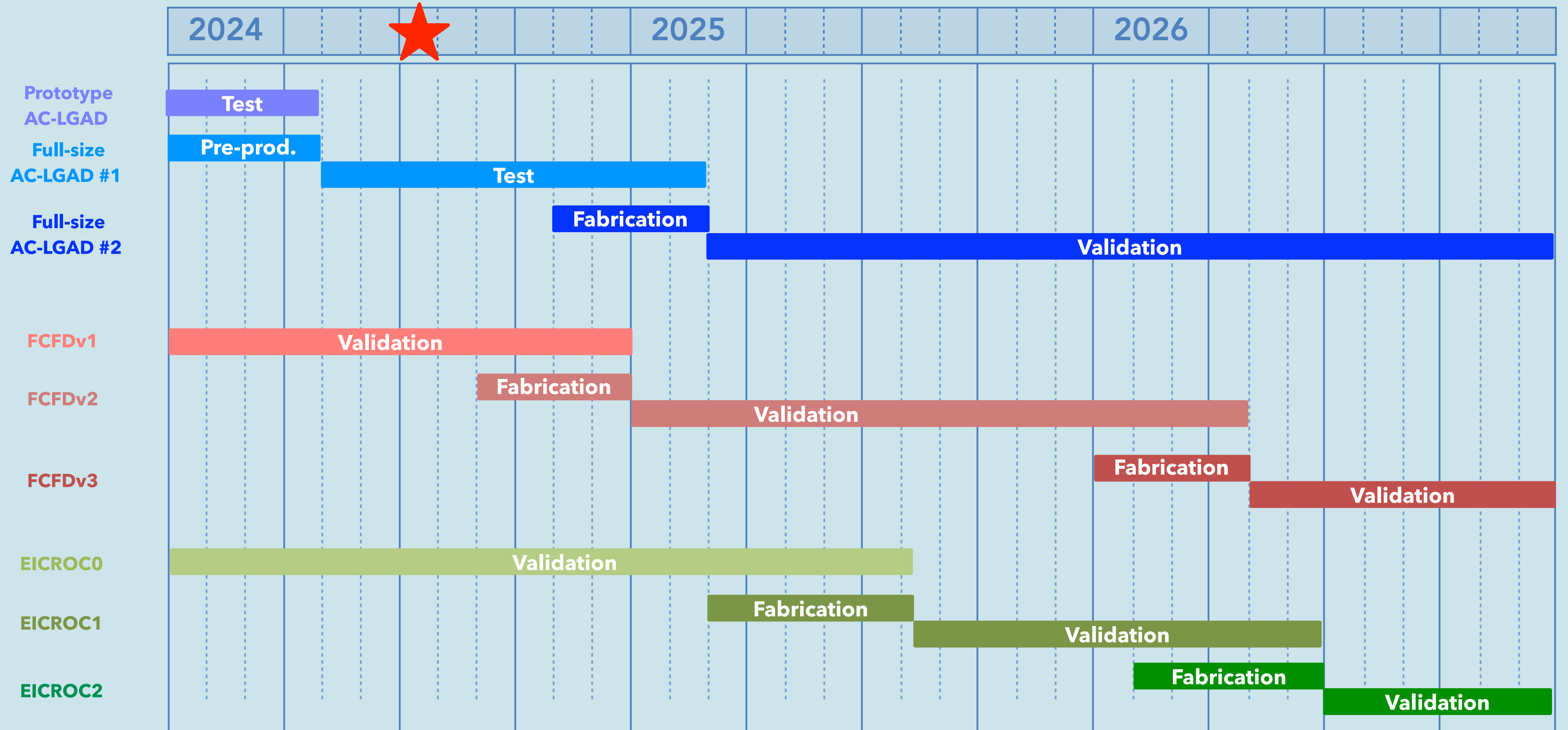
Module top view



Module cross section

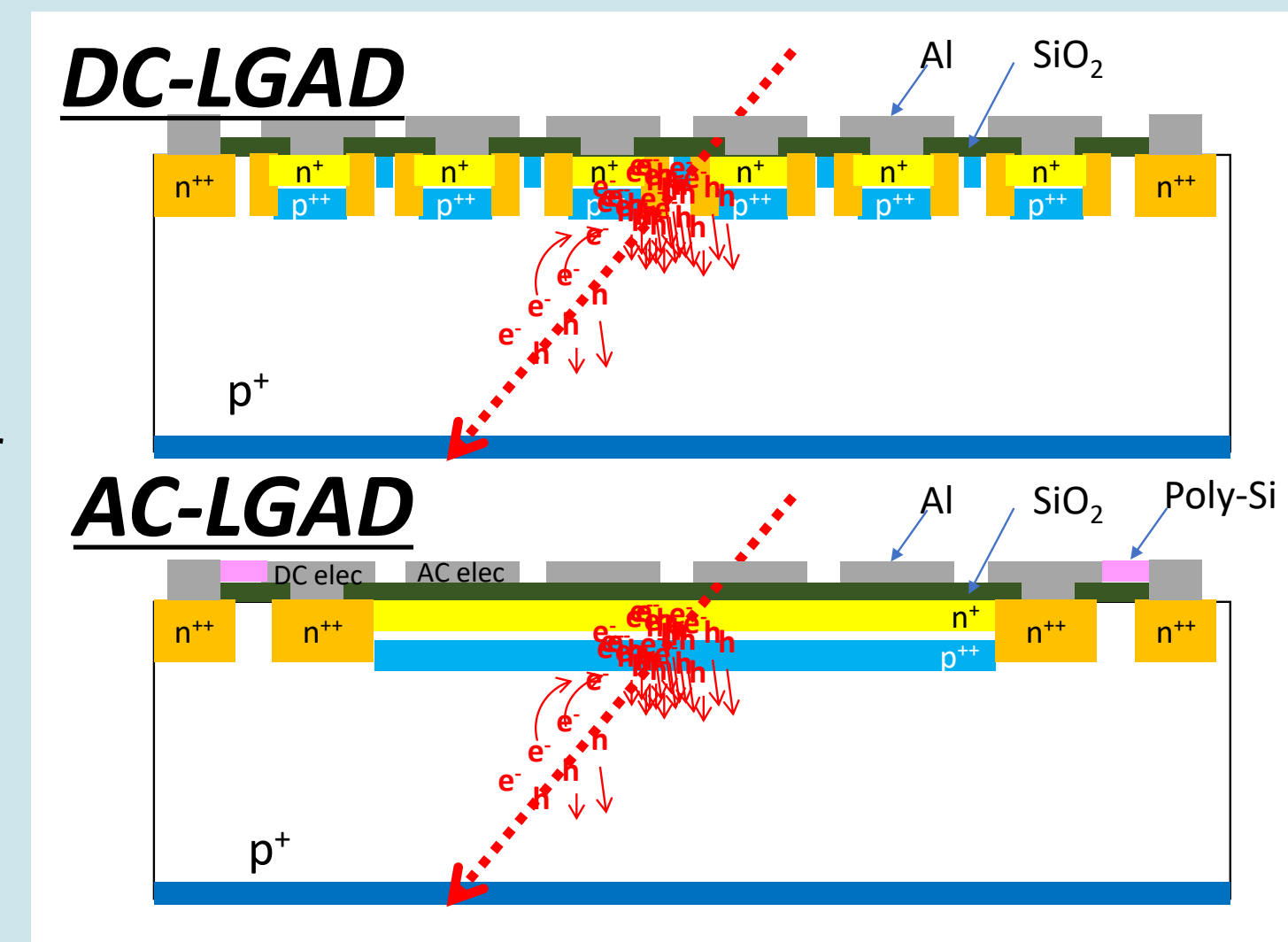
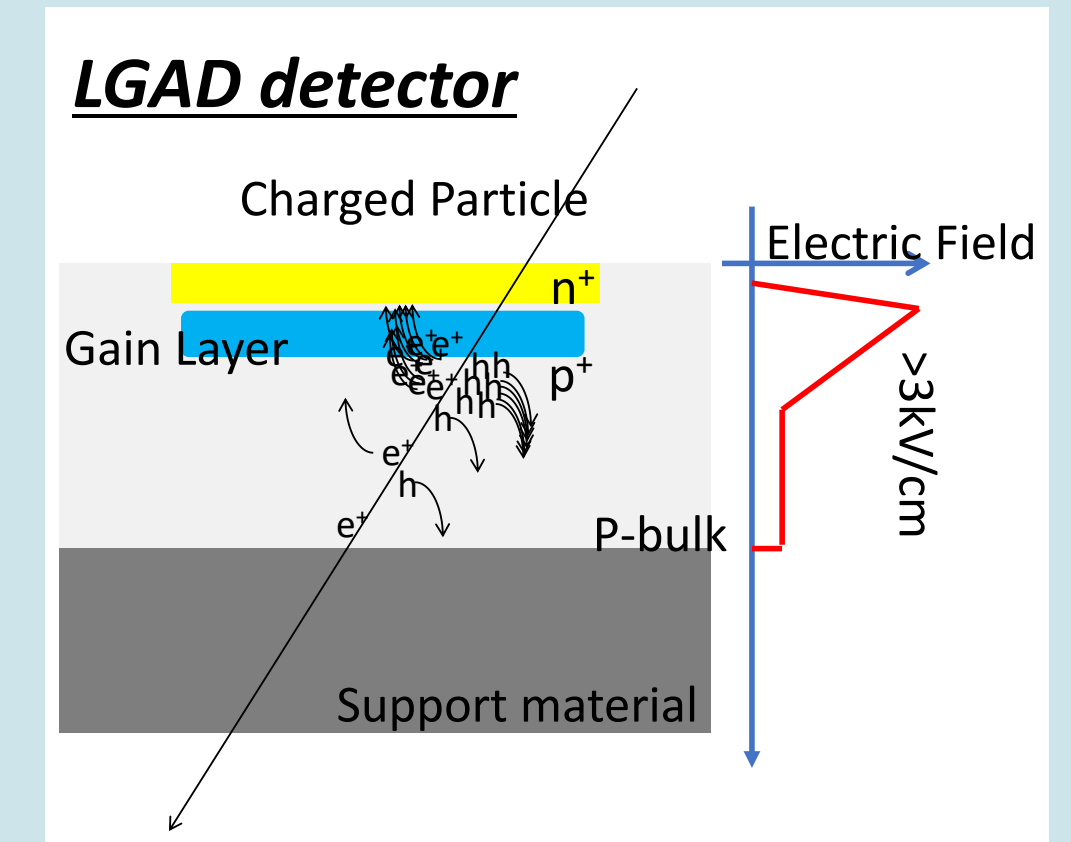


Original schedule of sensor + ASIC (Jan. 2024)



AC-LGAD technology

- Low Gain Avalanche Diode (LGAD)
 - The gain layer (p+ under n+ layer) makes a high electric field inducing electron avalanche → rapid signal raising
 - Standard LGAD (DC-LGAD) has much nonnegligible inactive area in fine segment case
 - CMS and ATLAS adopt DC-LGAD technology at HL-LHC
- AC-coupled LGAD (AC-LGAD)
 - One large gain layer with multiple AC-coupled readout metals on an oxide layer makes possible fine-segment readout keeping high timing resolution
 - High spatial resolution can be achieved with charge sharing even with relatively large pitches
 - EIC can adopt AC-LGAD technology thanks to the low multiplicity environment



K. Nakamura et al.,
JPS Conf. Proc. 34, 010016 (2021)

R&D elements for AC-LGAD

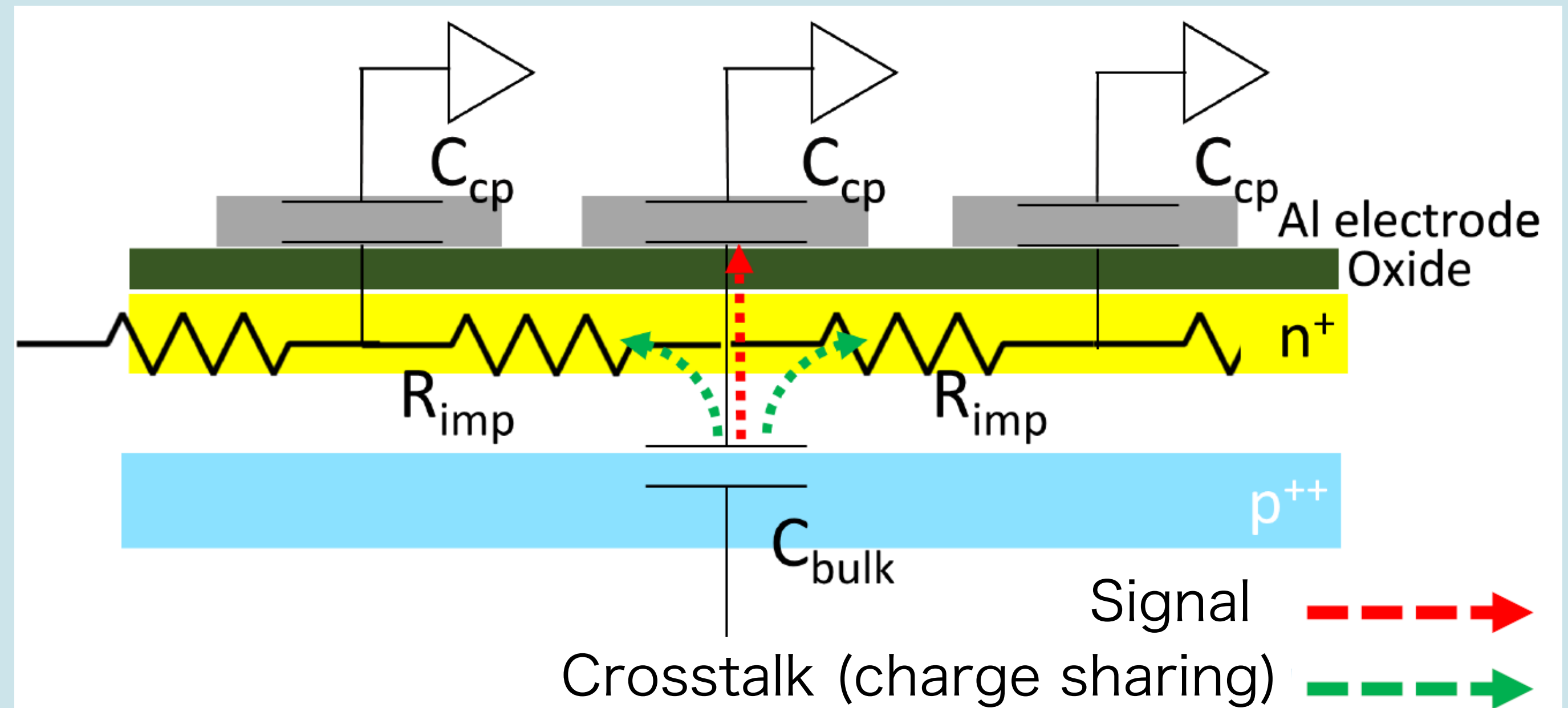
- Issues of AC-LGAD
 - Crosstalk in n⁺ layer
 - Small signal due to AC-coupling

- Signal size Q

$$Q = \frac{Z_{R_{imp}}}{Z_{R_{imp}} + Z_{C_{CP}}} Q_0$$

- Two important parameters

- R_{imp} → larger is better
 - n⁺ doping concentration
- C_{cp} → larger is better
 - Smaller electrode size → smaller C_{cp}
 - Thinner oxide → larger C_{cp}

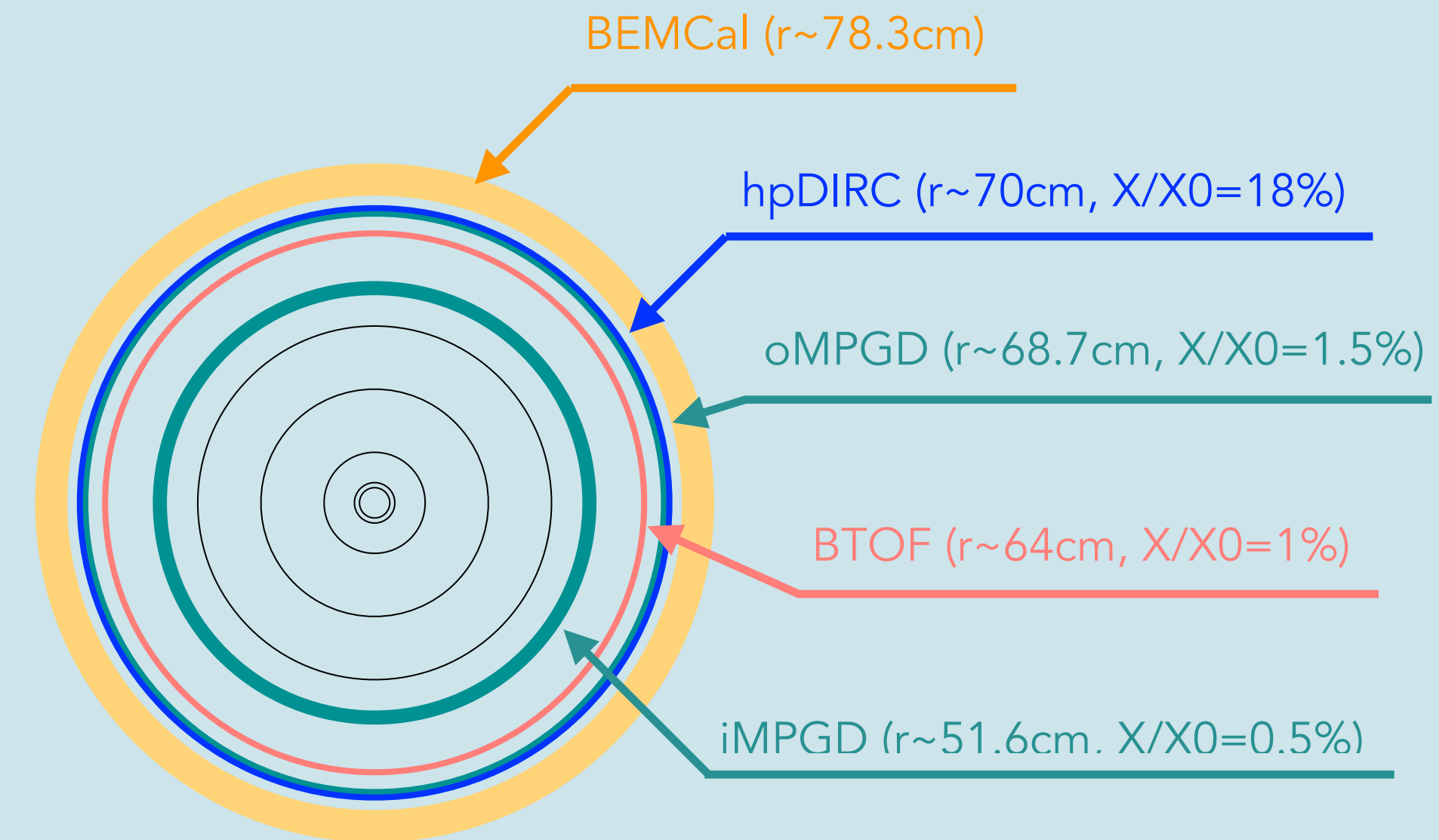


K. Nakamura et al., JPS Conf. Proc. 34, 010016 (2021)

Development goal
Keep a larger signal and smaller crosstalk
with a good time and spatial resolution

Material budget study (Hiroshima)

- **Shunichiro Muraoka** (M2 student) is working on the BTOF material effects on hpDIRC and BEMCal performance
- This study is significant for the stave structure design
 - oMPGD is placed just in front of hpDIRC in the latest design → Not big effects on angular determination resolution by the BTOF material
 - The material budget of hpDIRC in the active area is approximately 18% → Not big effects on the EMCal performance by the BTOF material
- The study will reveal if the very strict limit of 1% material budget imposed on BTOF is really necessary
 - This will open new options for the stave material selection and 1.3 m FPC design



Current Status

■ Track Reconstruction (EICRecon)

- Particle gun : π^+ from (0,0,0), 1000event
- Momentum : $1 \leq p \leq 10\text{GeV}$
- Eta : $-1.4 \leq \eta \leq 1.4$

Reconstruct tracks from each detector hit information using EICRecon official package

[Shunichiro's slide link](#)

Next plan

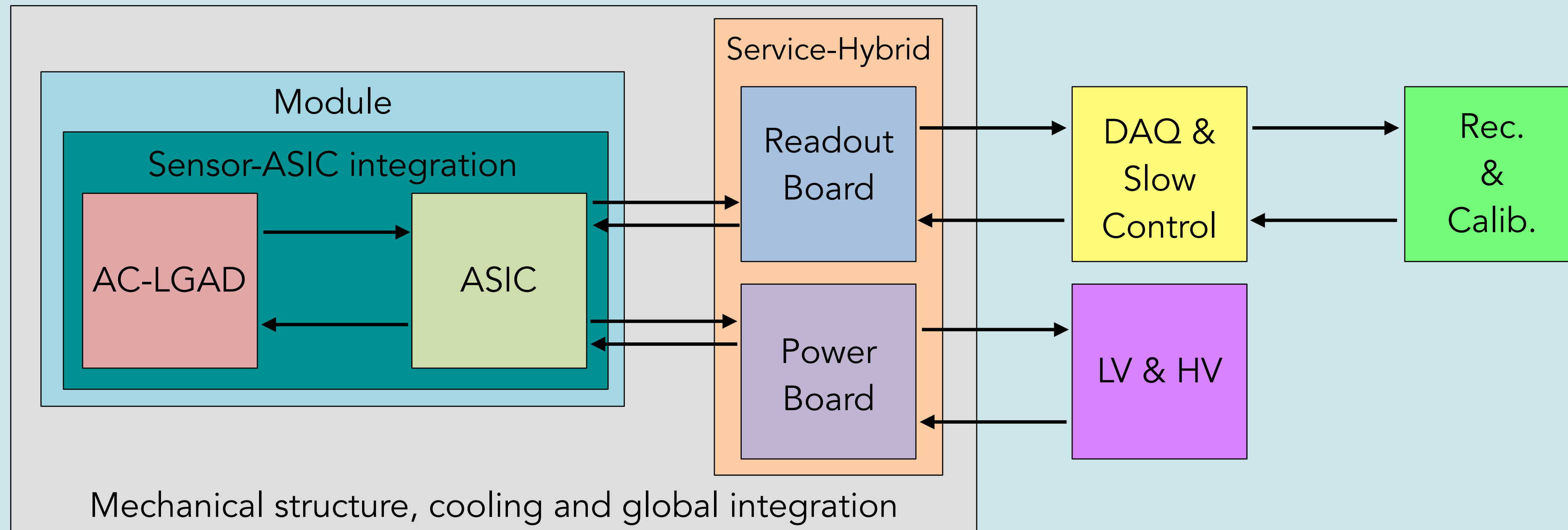
Track reconstruction to hpDIRC surface

Track direction: Tangent
DIRC (71 cm)

Outward fit
Inward fit
Track IU (Track Parameters)
Outer MPGD

Calculate the **angular distribution** of incident particles on the hpDIRC surface

TOF structure



- **Barrel-TOF (BTOF)**

- Strip-type AC-LGAD
- ASIC (FCFD)
- Sensor-ASIC integration
- Module
- Service-Hybrid
- Mechanical structure
- Global integration

- **Forward-TOF (FTOF)**

- Pixel-type AC-LGAD
- ASIC (EICROC)
- Sensor-ASIC integration
- Module
- Service-Hybrid
- Mechanical structure
- Global integration

- **Common system**

- DAQ
- Cooling
- Software (Rec. & Calib.)
- HV & LV
- Slow control

New clean room (100m²) @ HU

