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# Test of Single Event Effects on ITS3 monolithic sensors

Nicola Minafra

On behalf of the ALICE Collaboration



This work is supported  
by DOE EPSCoR

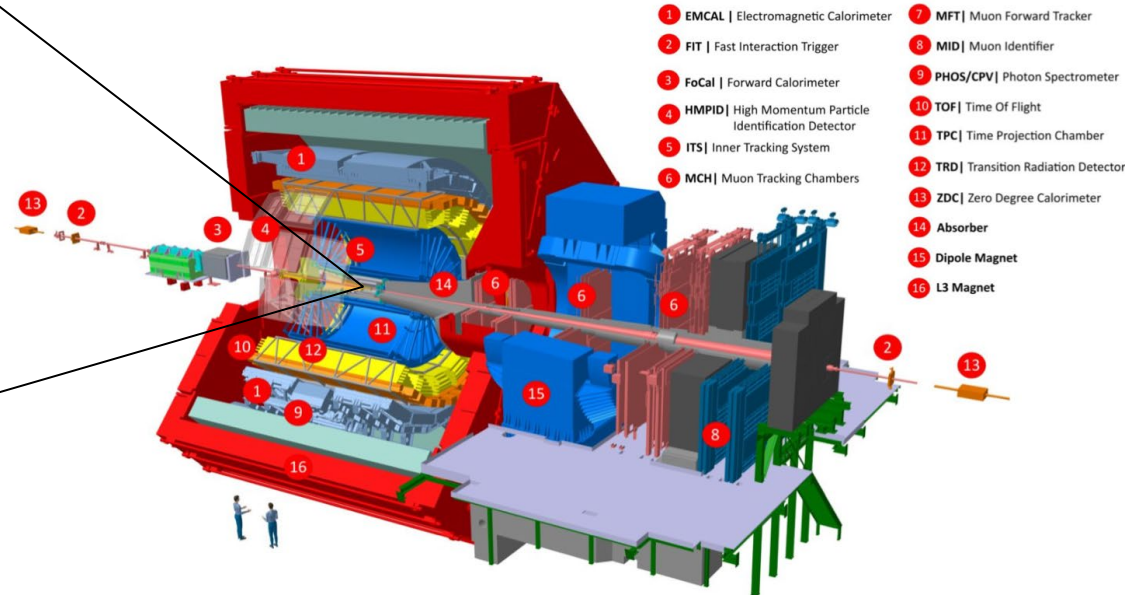
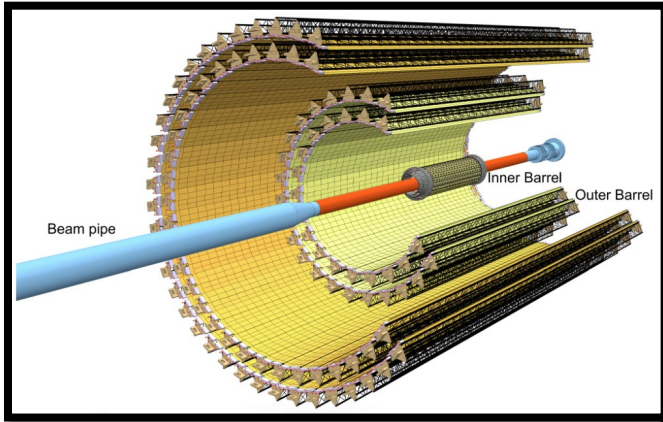
July 27<sup>th</sup> 2024





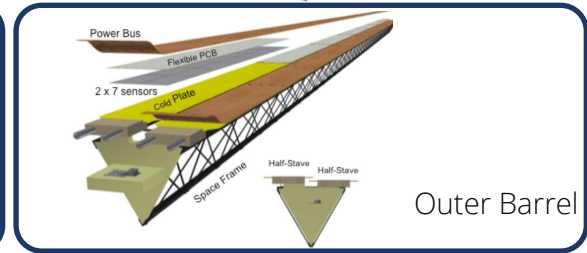
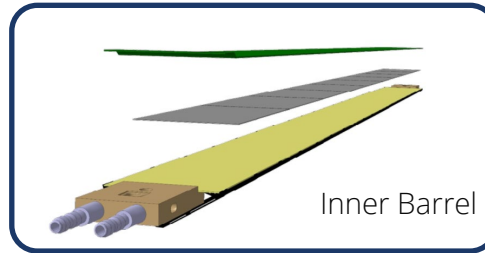
- Monolithic sensors for the ALICE: ITS and FoCal
- Stitched Monolithic Pixel Sensor (MOSS) for ITS3
- Stitched Monolithic Sensors for EIC
- Characterization of Single Event Effects

# The Inner Tracking System (ITS2) of the ALICE Experiment

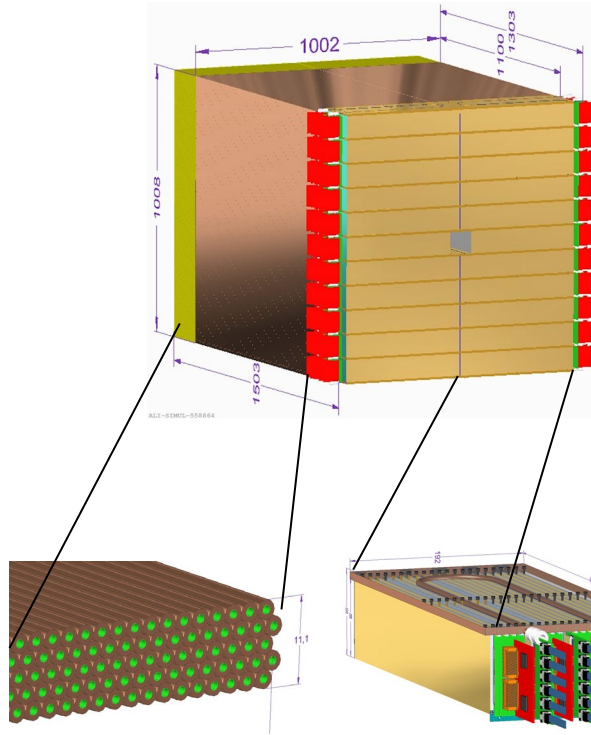


7 layers

- All silicon pixels
- Rate capability  $\sim 100$  kHz Pb+Pb
- 24k chips
- $10 \text{ m}^2$
- 12.5 GPixel

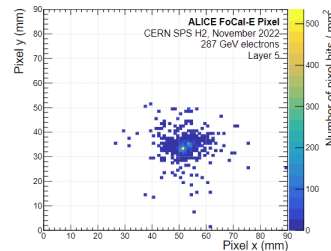
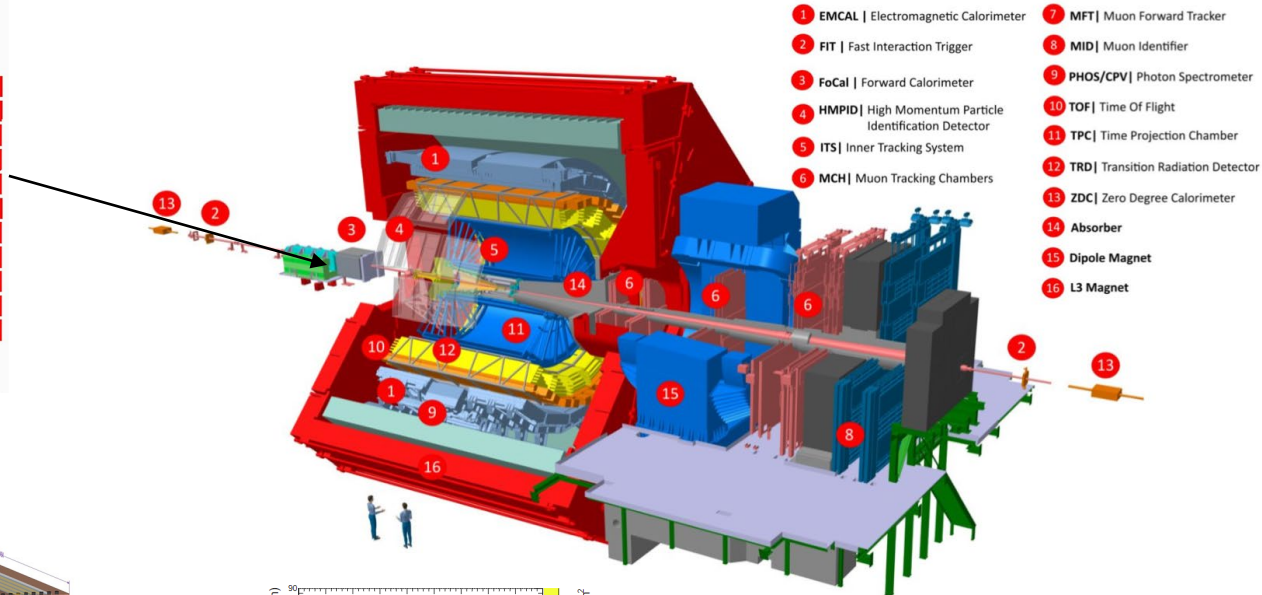


# FoCal: Forward Calorimeter for ALICE detector for Run 4 of the LHC



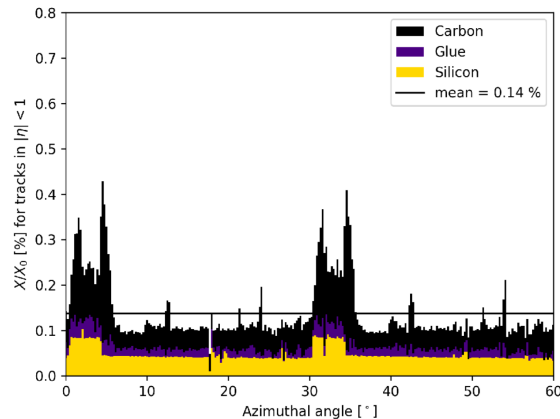
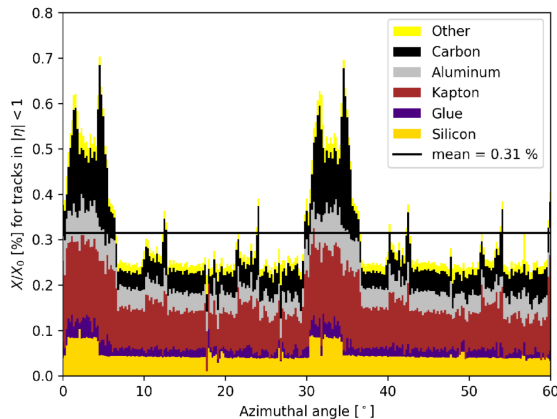
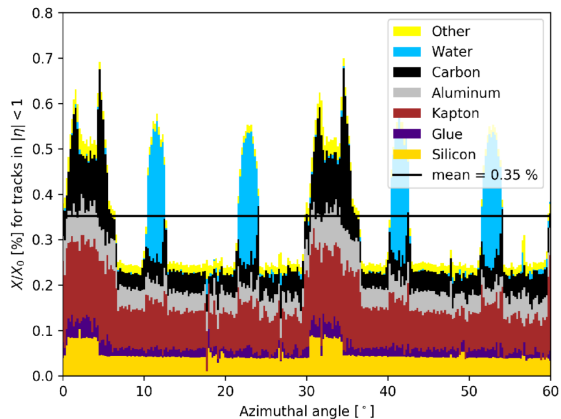
FoCal-H  
Transversally segmented  
spaghetti calorimeter  
Tot thickness  $\sim 6 \lambda_{had}$

FoCal-E  
20 Layers (LG + HG Si detectors +  
W absorbers). Tot ( $\sim 20 X_0$ )



High spatial resolution of ALPIDES  
guarantees 2 photons discrimination

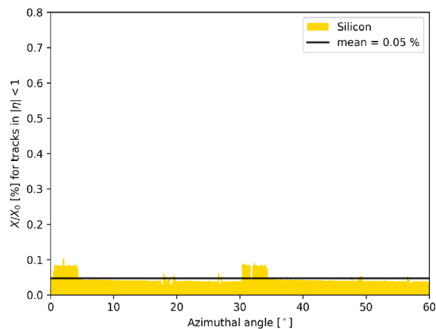
# Limitation of ITS2: toward ITS3



Si makes only 1/7th of total material!!

Removal of water cooling - **possible** if power consumption stays below 20 mW/cm<sup>2</sup>

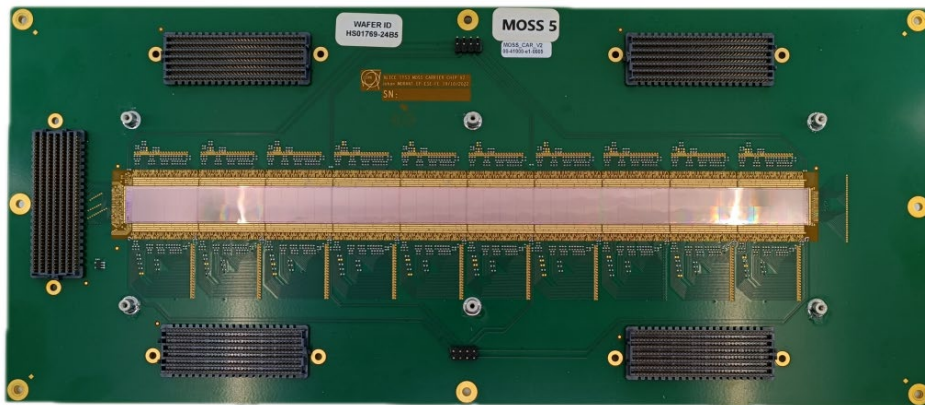
Removal of the circuit board (power+data) - **possible** if integrated on chip



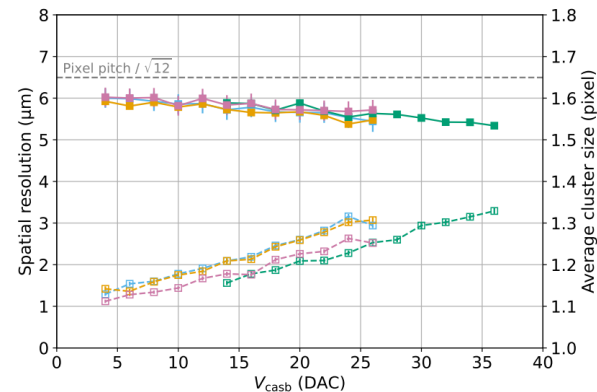
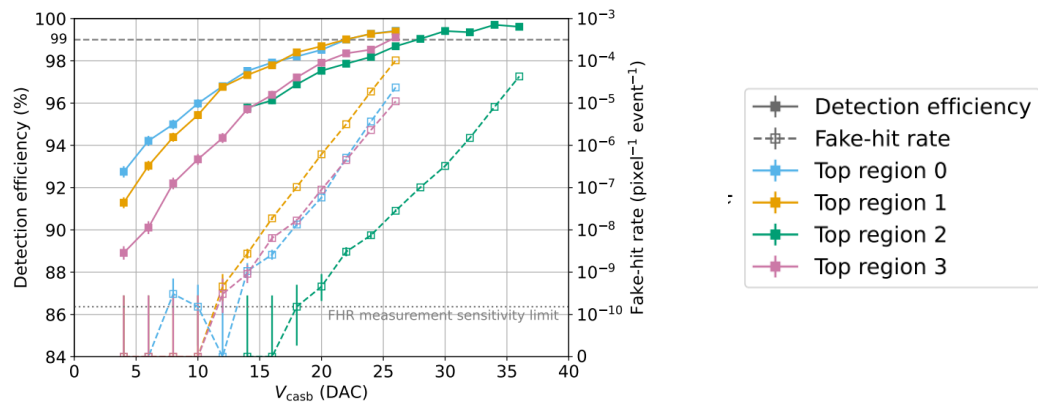
Removal of mechanical support - **benefit** from increased stiffness by rolling Si wafers



# MOSS: prototype of monolithic stitched sensor



Detection efficiency and resolution measured with MOSS at the CERN PS using a MOSS wire-bonded on its carrier card

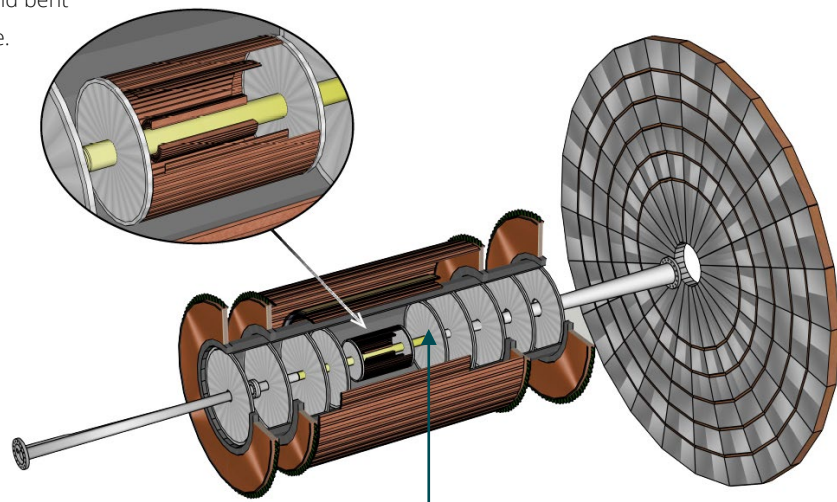
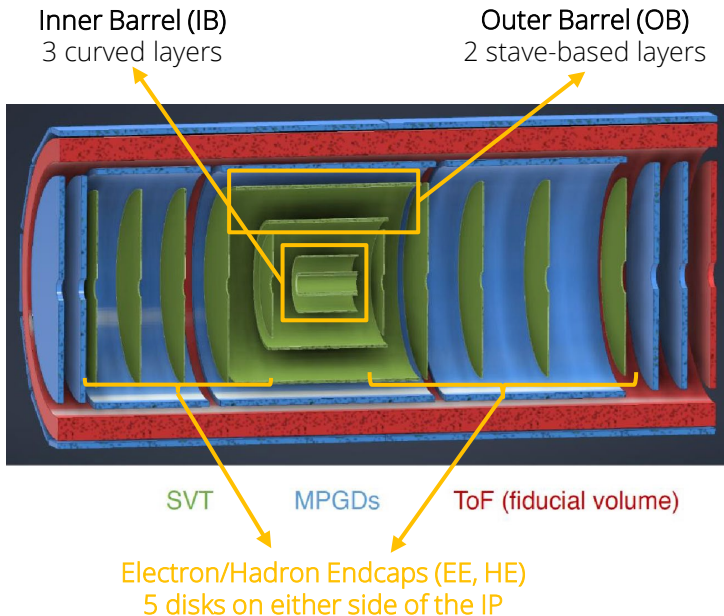




# Inner Tracker for ePIC at the EIC

Silicon Vertex and Tracker (SVT)

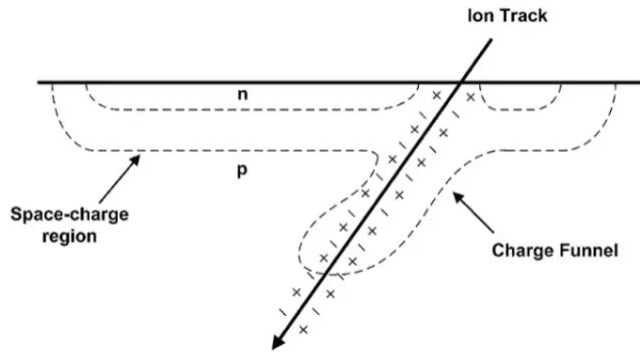
ITS3 wafer-scale stitched sensor, thinned and bent around beam pipe.



Barrel layers and disks

EIC Large Area Sensor (LAS), i.e. ITS3 sensor size optimized for high yield, low cost, large area coverage.

A single particle passing through the silicon is depositing energy: Linear Energy Transfer (LET)



## Single Event Upset (SEU):

change of state caused by one single ionizing particle

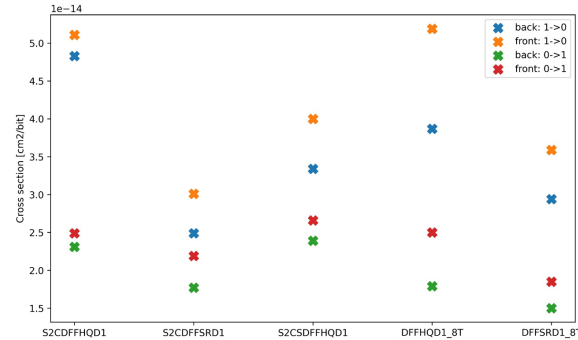
## Single Event Latchup (SEL):

the inadvertent creation of a **low-impedance path** between the power supply rails of a MOSFET circuit, triggering a parasitic structure which disrupts proper functioning of the part, possibly even leading to its destruction due to overcurrent. A power cycle is required to correct this situation.





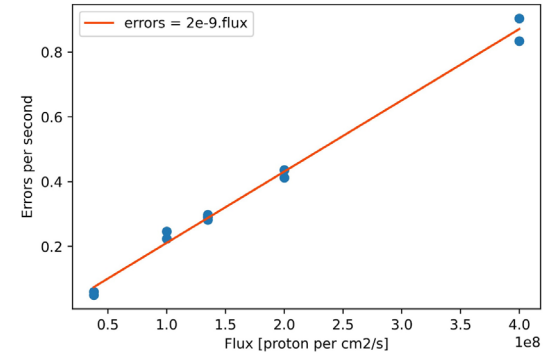
## SEU1



Flux of  $2 \times 10^9$  protons/ $\text{cm}^2/\text{s}$

- asymmetry between 1->0 and 0->1 bit flips for all FIFOs
- significant differences between individual types of FIFO structures

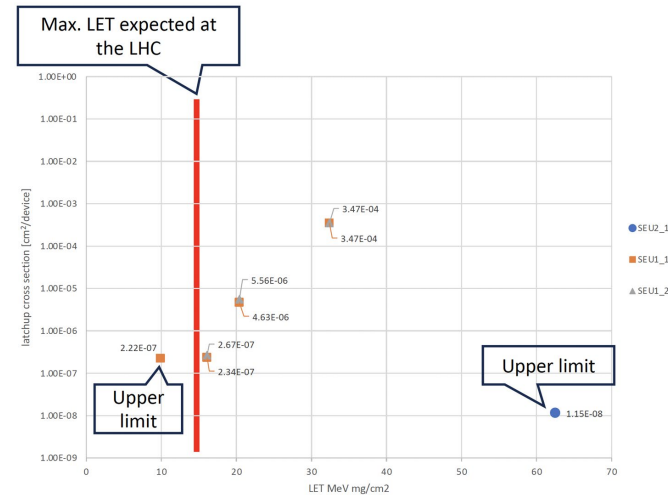
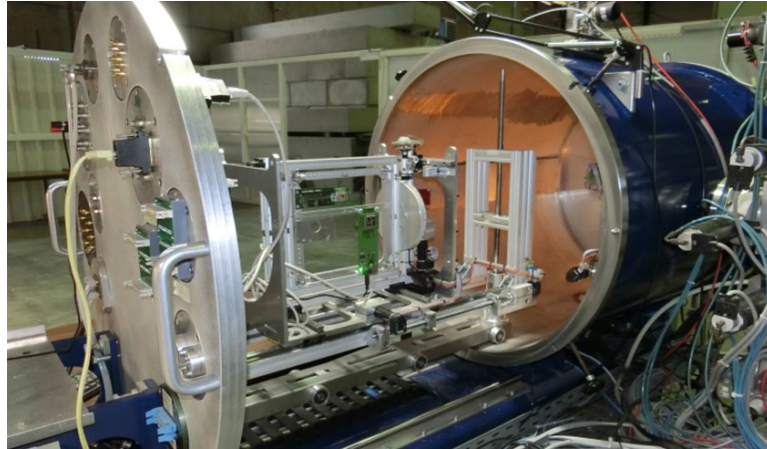
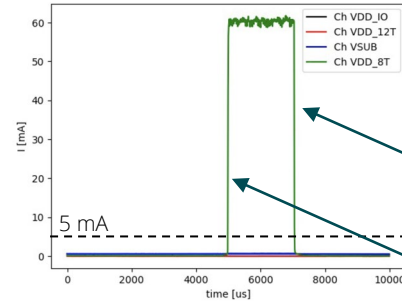
## SEU2

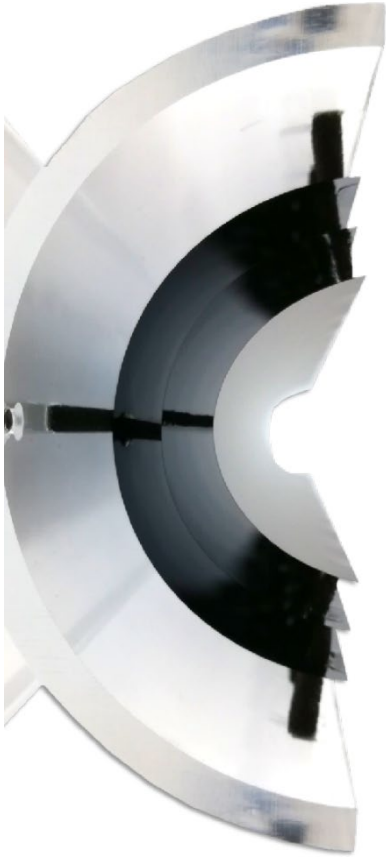


- no asymmetry between 1->0 and 0->1 observed
- SEU occurrence linear with the beam flux

# SEL tests: Heavy Ion Facility @UCLouvain (BE)

M/Q	Ion	Energy [MeV]	Range [ $\mu\text{m}$ ]	LET [MeV/(mg/cm <sup>2</sup> )]
3,25	<sup>13</sup> C <sup>4+</sup>	131	269,3	1,3
3,14	<sup>22</sup> Ne <sup>7+</sup>	238	202,0	3,3
3,37	<sup>27</sup> Al <sup>8+</sup>	250	131,2	5,7
3,27	<sup>36</sup> Ar <sup>11+</sup>	353	114,0	9,9
3,31	<sup>53</sup> Cr <sup>16+</sup>	505	105,5	16,1
3,22	<sup>58</sup> Ni <sup>18+</sup>	582	100,5	20,4
3,35	<sup>84</sup> Kr <sup>25+</sup>	769	94,2	32,4
3,32	<sup>103</sup> Rh <sup>31+</sup>	957	87,3	46,1
3,54	<sup>124</sup> Xe <sup>35+</sup>	995	73,1	62,5





- Monolithic sensors (ALPIDE) are currently used in ALICE: ITS and FoCal (and MFT)
- It is possible to design a wafer scale monolithic sensor that allows lower and more uniform material budget
- Technical Design report of ITS3 approved by CERN LHC Committee (LHCC) and the CERN Research board (RB)
- SEE tests performed at Louvain-la-Neuve (BE) and BASE (USA)  
[Z. Ye: Update on Irradiation and Beam Tests](#)
- ER1 sensors are working and are currently characterized
- Characterization of Single Event Effects (and much more...) is needed to provide feedback to the designers for ER2 (exp. <Q1 2025)



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# Test of Single Event Effects on ITS3 monolithic sensors

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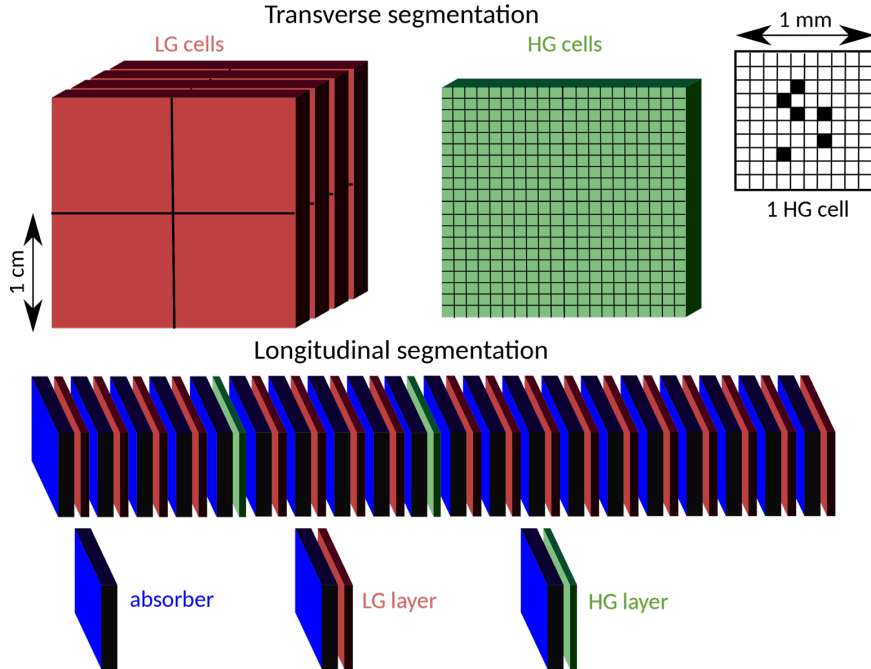
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July 27<sup>th</sup> 2024

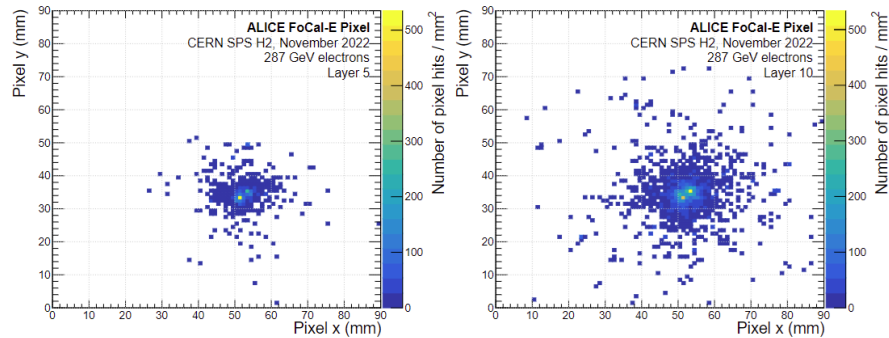
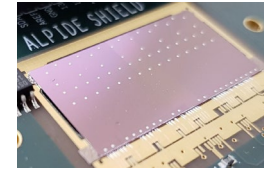


# FoCal-E: low granularity pad sensors, high granularity ALPIDEs

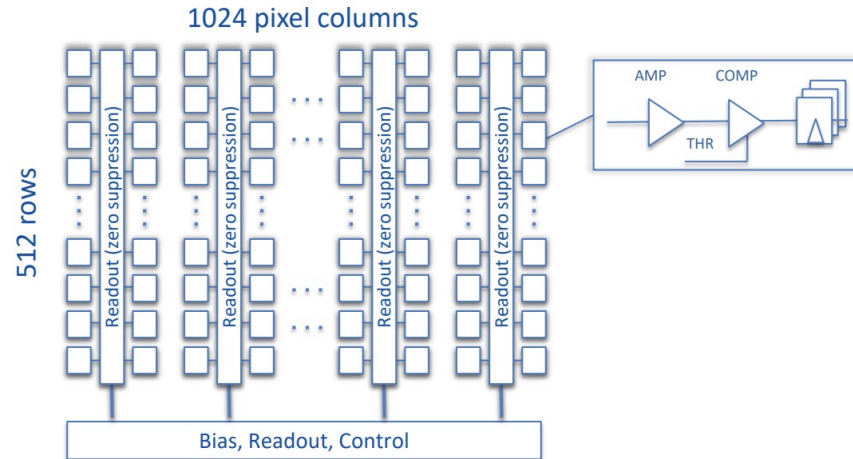
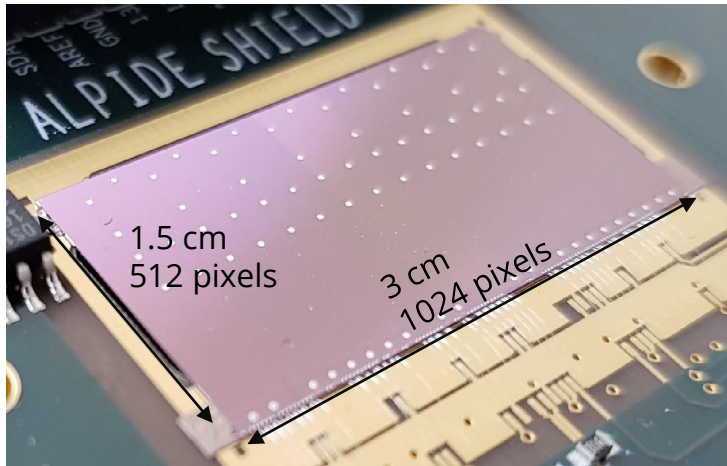
20 layers of W (each of 3.5mm thickness) and Si sensors



High granularity layers (positions 5 & 10):  
monolithic pixel sensors (ALPIDE)



## Pixel Sensor CMOS 180 nm Imaging Process (TowerJazz)



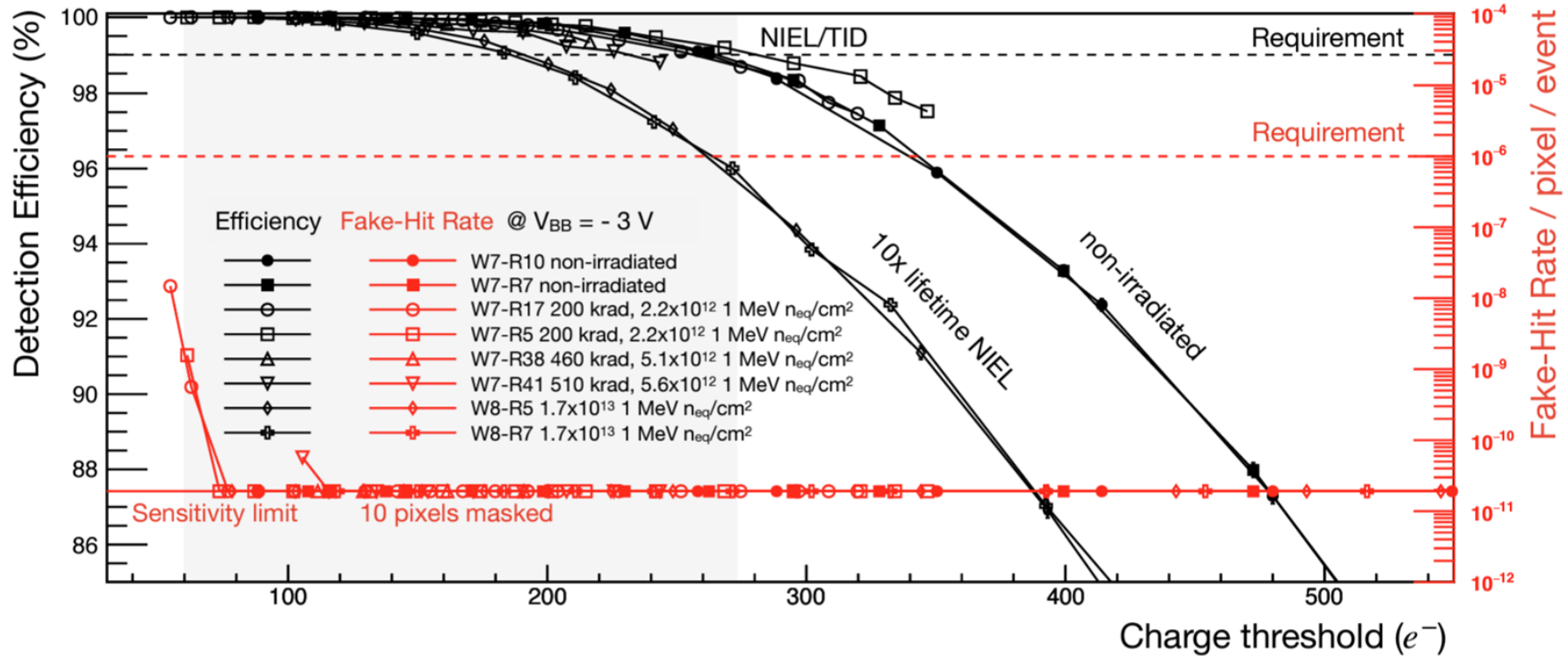
High-resitivity ( $>1 \text{ k}\Omega \text{ cm}$ ) p-type epitaxial layer ( $25 \mu\text{m}$ ) on p-type substrate

- Small n-well diode ( $2 \mu\text{m}$  diameter)  $\Rightarrow$  low capacitance ( $\sim 5 \text{ fF}$ )
- Reverse bias voltage ( $-6\text{V} < V_{\text{BB}} < 0\text{V}$ ) to substrate to increase depletion region
- Deep p-well shields n-well of PMOS

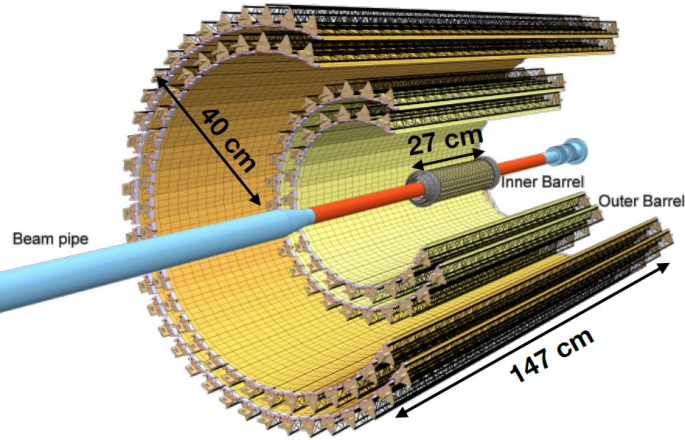
- Continuously active front-end
- Global shutter (STROBE signal)
- Zero-suppressed matrix readout
- Triggered or continuous readout modes



# The ALPIDE monolithic sensor



# The Inner Tracking System (ITS2) of the ALICE Experiment

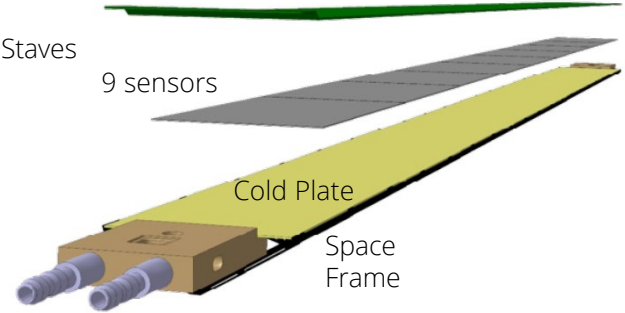


3 Inner Layers: 12+16+20 Staves

1 Module/Stave

9 sensors per Module

50  $\mu\text{m}$  sensors



2 Middle Layers: 30+24 Staves

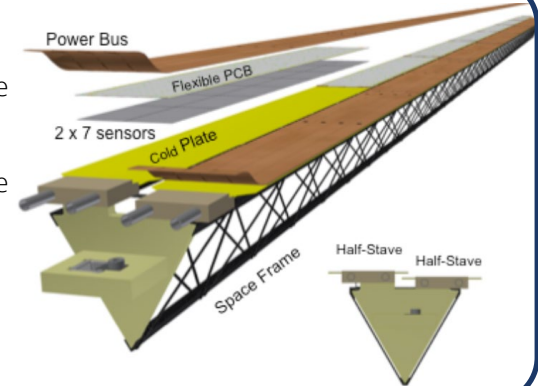
2x4 Modules/Stave

2 Outer Layers: 42+48 Staves

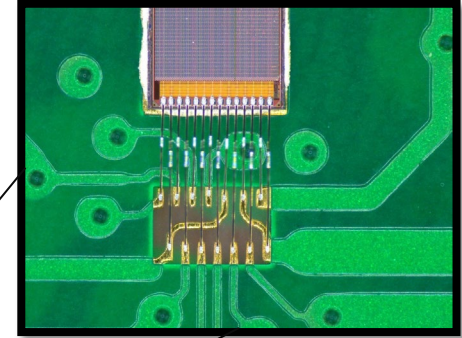
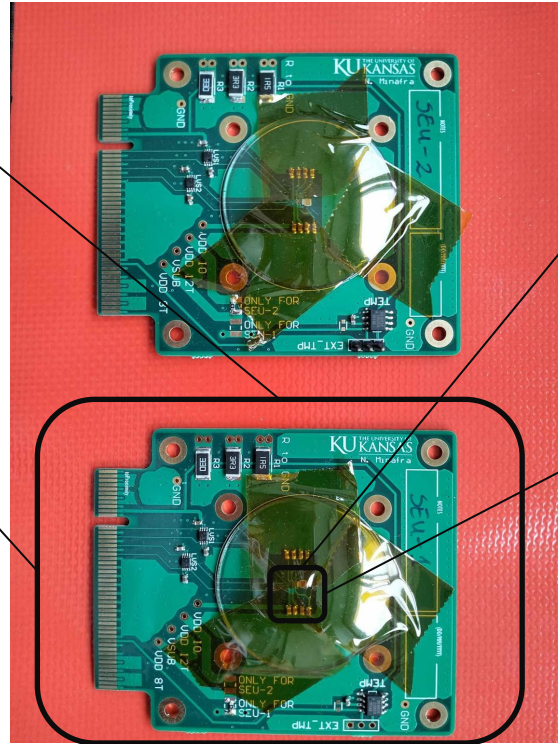
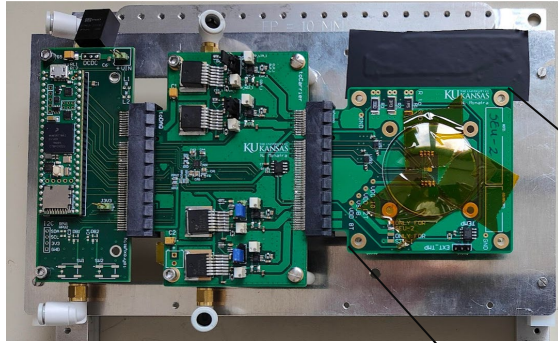
2x7 Modules/Stave

2x7 sensors / Module

100  $\mu\text{m}$  sensors

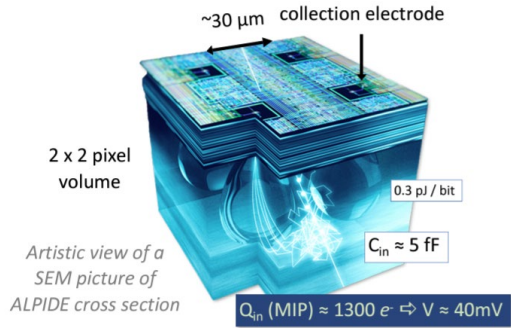


# SEE Investigation



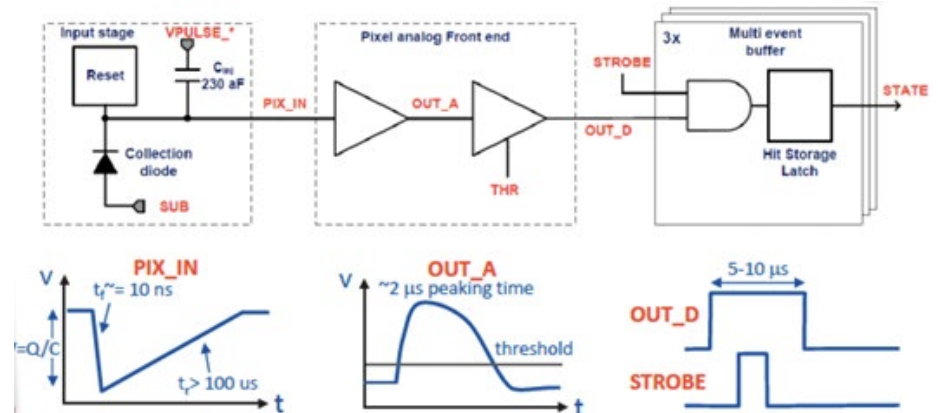
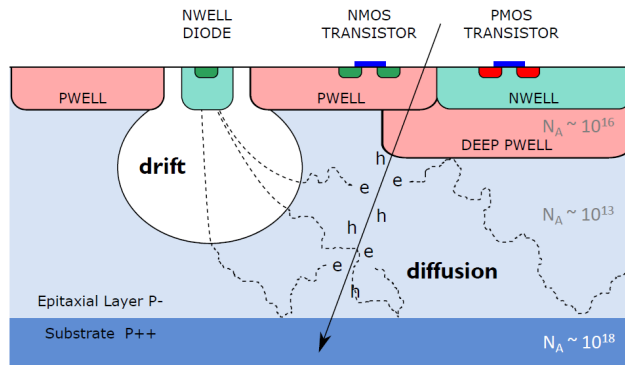
# The ALPIDE monolithic sensor

## Pixel Sensor CMOS 180 nm Imaging Process (TowerJazz)

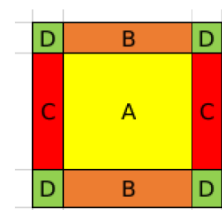
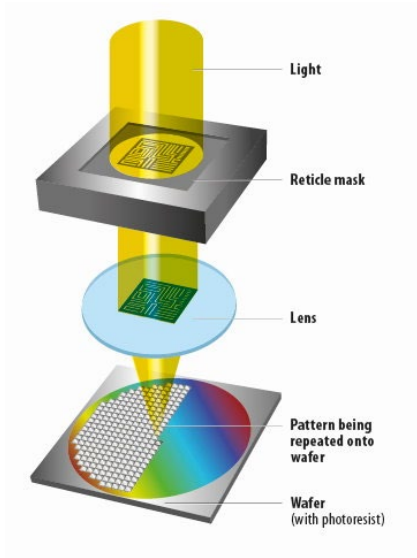


Each pixel (29  $\mu\text{m}$  x 27  $\mu\text{m}$ ) has:

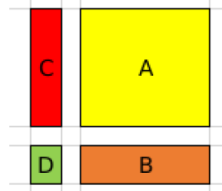
- Amplification
- Discrimination
- 3 hit storage registers (MEB)
- Test charge injection
- Masking



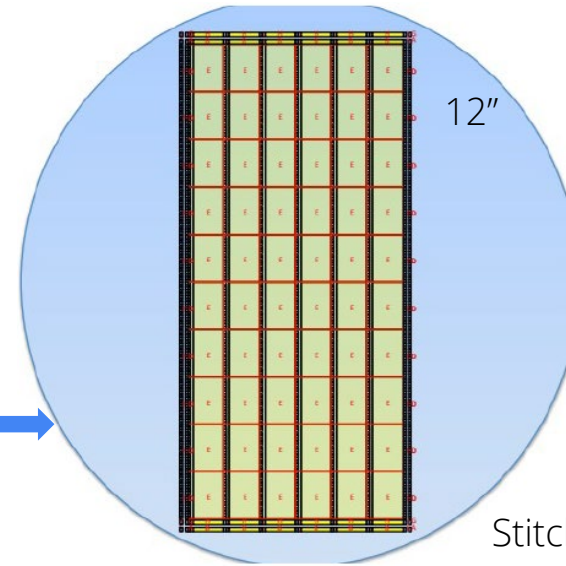
# Wafer-scale sensors



Reticle



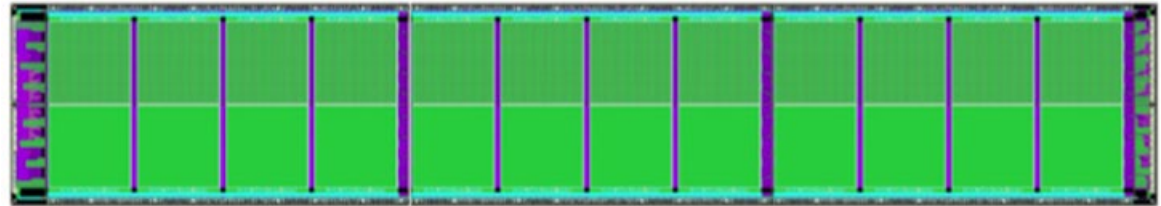
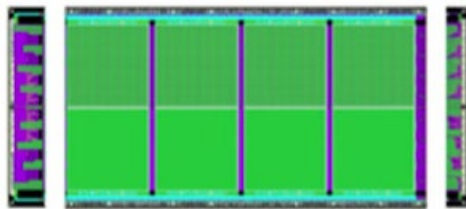
Splitted



12"

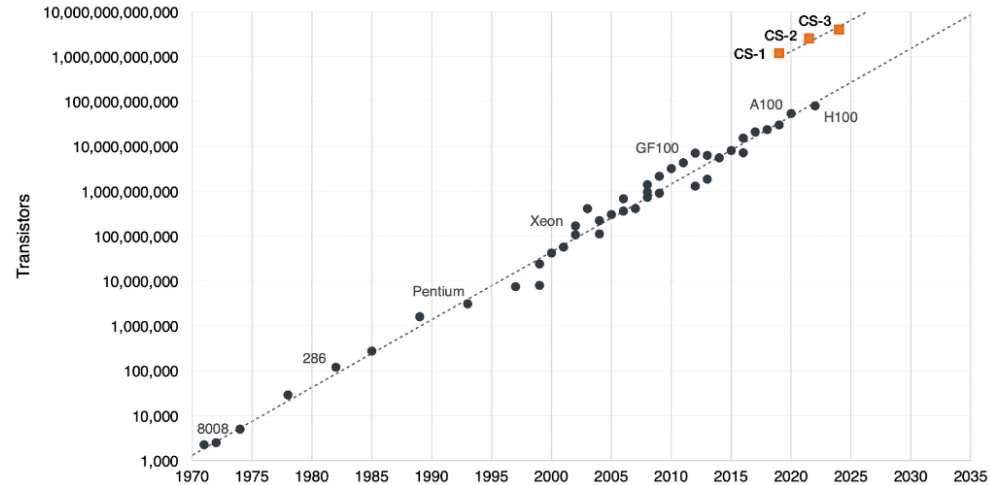
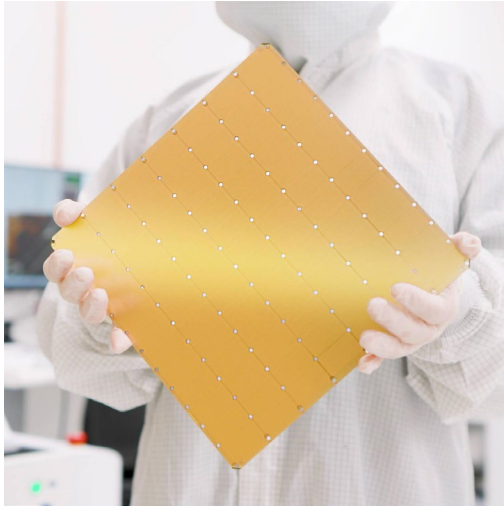
Stitched

6 wafers make the entire ITS3 production





# Wafer-scale for AI



CEREBRAS WSE-3

	WSE-3	Nvidia H100	Cerebras Advantage
Chip Size	46,225 mm <sup>2</sup>	826 mm <sup>2</sup>	57 X
Cores	900,000	16,896 FP32 + 528 Tensor	52X
On-chip memory	44 Gigabytes	0.05 Gigabytes	880 X
Memory bandwidth	21 Petabytes/sec	0.003 Petabytes/sec	7,000 X
Fabric bandwidth	214 Petabits/sec	0.0576 Petabits/sec	3,715 X