Report from the Interaction Tagger Workfest

P. Antonioli (INFN-Bologna)

ePIC Collaboration Meeting
Lehigh University 22-27 July 2024

O(20) participants

But here the short version summary

The workfest was so succcessfull that we agreed the title of the workfest was misleading

Session

Interaction Tagger Workfest

26 Jul 2024, 13:00

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~~Interaction Tagger Workfest~~

~~26 Jul 2024, 13:00~~

Session

dRICH Data Reduction Workfest
How to tag tracks in dRICH acceptance
(an interaction tagger is another thing, eh)

26 Jul 2024 @ **17:00**

Why this workfest?

Since long time we aired the idea of a tagger able to provide a simple signal to curb **dRICH data throughput**

an agnostic tagger just for detecting tracks in dRICH acceptance could be built with **something specific (dTT)** and/or using also information from ***other*** **detectors** (FHCal, FEMCal, TOF , ...)

Since long time we aired the idea of smart things happening analysing quickly dRICH data (ML, pattern regognition, ...)

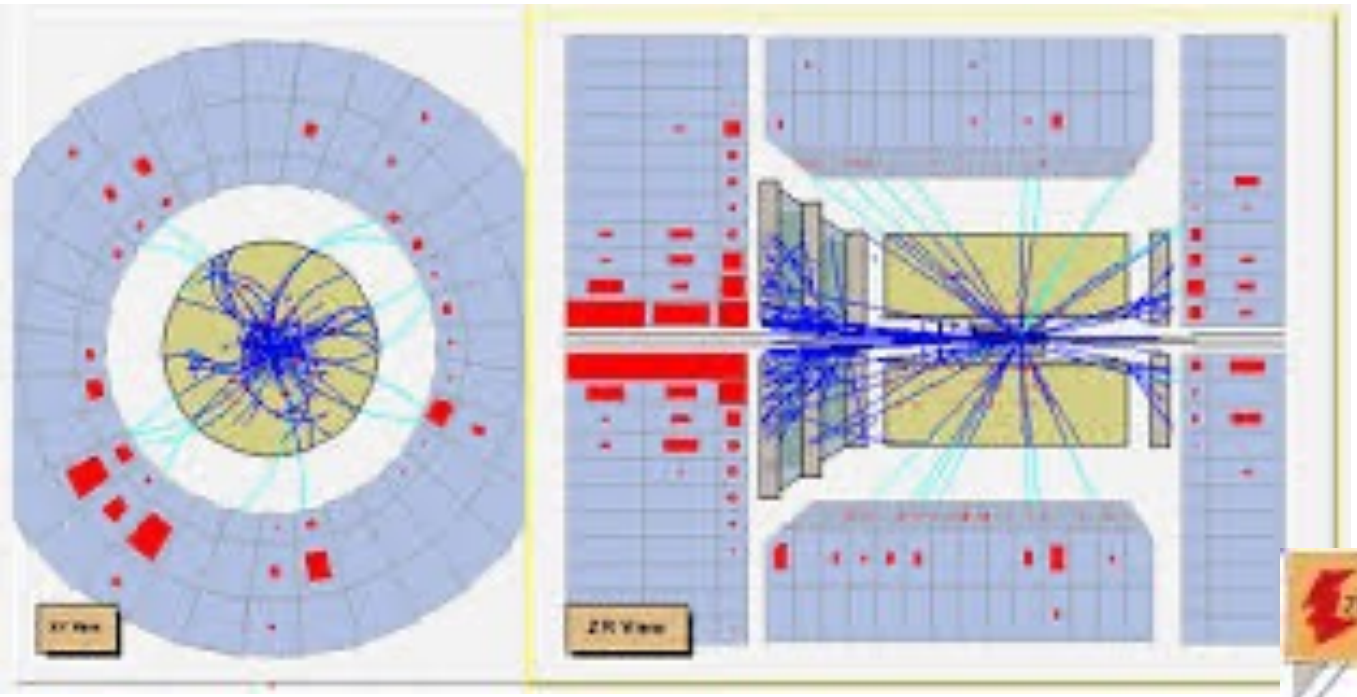
"**data reduction algorithms** integrated with **SRO DAQ and computong**"

Generally speaking, an interaction tagger for ePIC (1 interaction/every 200 BC) is a good idea

This should be **unbiased minimum-bias interaction tagger**

13:00	**Introduction** *Rm 61, Rausch Business Center*		*Marco Contalbrigo* 13:00 - 13:10
	dRICH Data Stream *Rm 61, Rausch Business Center*	**dRICH data throughput**	*Pietro Antonioli et al.* 13:10 - 13:30
	Interaction Minbias Trigger *Rm 61, Rausch Business Center*	**unbiased minimum-bias interaction tagger**	*Dr E. C. Aschenauer* 13:30 - 13:50
	ePIC DAQ Scheme *Rm 61, Rausch Business Center*	**SRO DAQ and computing**	*David Lawrence et al.* 13:50 - 14:10
14:00	**dRICH Tagget** *Rm 61, Rausch Business Center*	**something specific (dTT)**	*Marco Battaglieri* 14:10 - 14:30
	dRICH Data Filter *Rm 61, Rausch Business Center*	**data reduction algorithms**	*Dr Luca Pontisso et al.* 14:30 - 14:50
	Forward HCal *Rm 61, Rausch Business Center*	***other* detectors**	*Miguel Arratia et al.* 14:50 - 15:10
15:00	**Forward ECal** *Rm 61, Rausch Business Center*		*Oleg Tsai et al.* 15:10 - 15:30

Interaction tagging explained with ZEUS

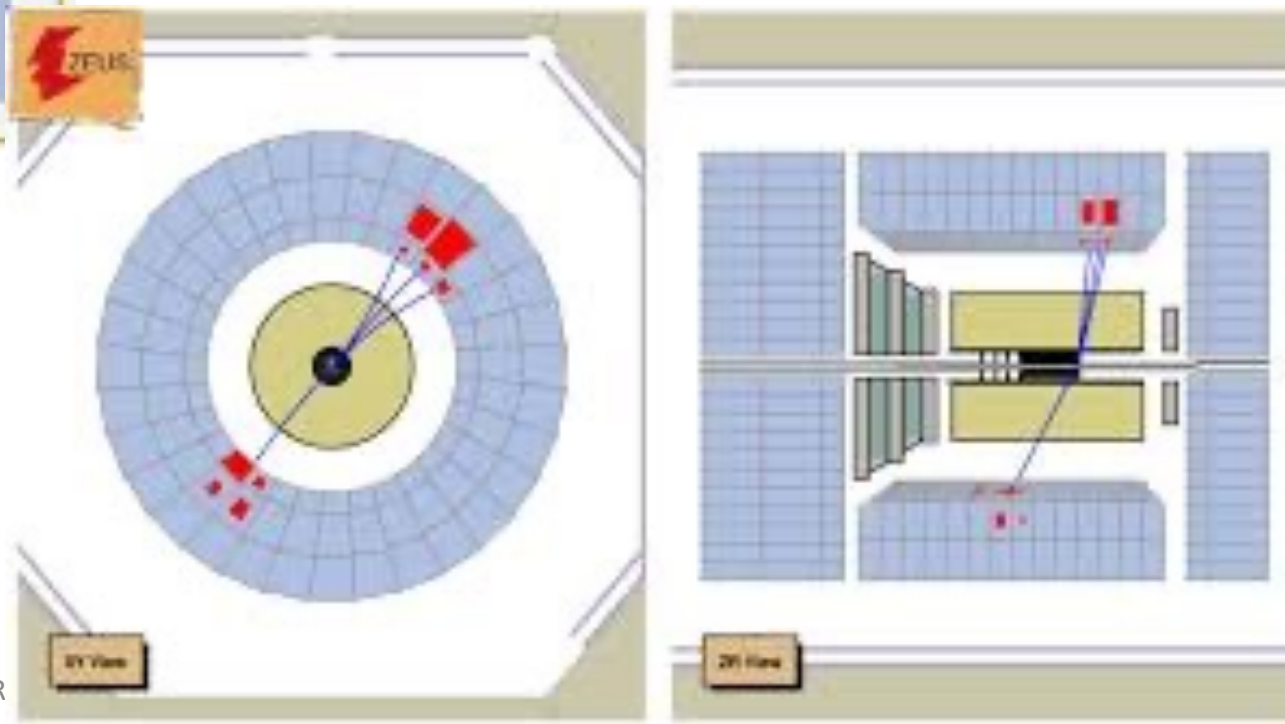


*Take home message

Construct a minimum-bias interaction tagger to cover full physics in an unbiased way is a different problem

combination of BHCAL + FHCAL to start with but...

(remember: @HERA hadrons went from right to left, @EIC they will go from left to right even if "forward" means always hadron direction)



The project/TIC will follow up coordinating different detectors info to build such tagger

the dRICH data stream

see Pietro slides for more details

Back to ATHENA proposal!

This is now implemented on ALCOR64 shutter (gating)

from signals from single photoelectrons. We hope to reduce this by a factor of 3–5 in the FEBs using sample cuts relative to the bunch crossing time. Further reduction can be obtained by a software trigger applied in the DAQ computers. Requiring a collision to be present will provide a data reduction by a factor of at least 200 allowing the ATHENA DAQ to write all collision data to tape. Another option for data reduction is by machine learning techniques implemented in the FPGAs of the FELIX boards; dedicated development and feedback from initial data are needed.

Software trigger means making a selection "after" data are on computers (beyond DAM)

Requiring a collision means look to physics → Elke's talk + "detectors" talks

ML on FPGA for RICH (NA62 expertise) → Alessandro/Luca talk

First (years) data will be critical: we don't need to reduce initial data

dRICH data stream at EIC day-0

Interaction tagger reduction factor	1	Channel/chip	64
Interaction tagger latency [s]	2,00E-09	**Shutter width (ns)**	10
EIC parameters			
EIC Clock [MHz]	98,522		
Orbit efficiency (takes into account gap)	0,92		

We first learn how to calibrate the shutter

dRICH data stream analysis		**Limit**	**Comments**
Sensor rate per channel [kHz]	3,00	4.000,00	
Rate post-shutter [kHz]	2,70	800,00	
Throughput to serializer [Mb/s]	1,73	788,16	
Throughput from ALCOR64 [Mb/s]	13,80		limit FPGA dependent: - check with RDO
Throughput from RDO [Gb/s]	0,05	10,00	based on VTRX+
Input at each DAM I [Gbps]	2,53	470,00	
Buffering capacity at DAM I [MB]	0,65		to be checked but seems manageable
Throughput from DAM I to DAM II [Gbps]	2,53	10,00	this might be higher (from FELIX to FELIX)
Output to each DAM II [Gbps]	68,41	270,00	

Aggregated dRICH data throughput		**Comments**
Total input at DAM I [Gb/s]	68,41	This is only "inside" DAM, not to be transferred on PCI
Total input at DAM II [Gb/s]	68,41	This is based on aggregation above + reduction factor of the interaction tagger
Total output from DAM II [Gb/s]	68,41	Further reduction possible to be investigated (FPGA level?)

- Presented full parameterization of dRICH data stream
- Main three parameters are ALCOR shutter window, "tagger data reduction factor (DRF)" and DCR/sensor
- At maximum radiation damage, with DRF=1 trhoughput is 1.4 Tbps (dRICH aggregated)
- At EIC day-0 /DRF=1/no shutter just 66.6 Gbps
- DRF=200 corresponds to physics, DRF=20 would be enough...

*Take home message

The dRICH data stream is not an issue, it is well understood

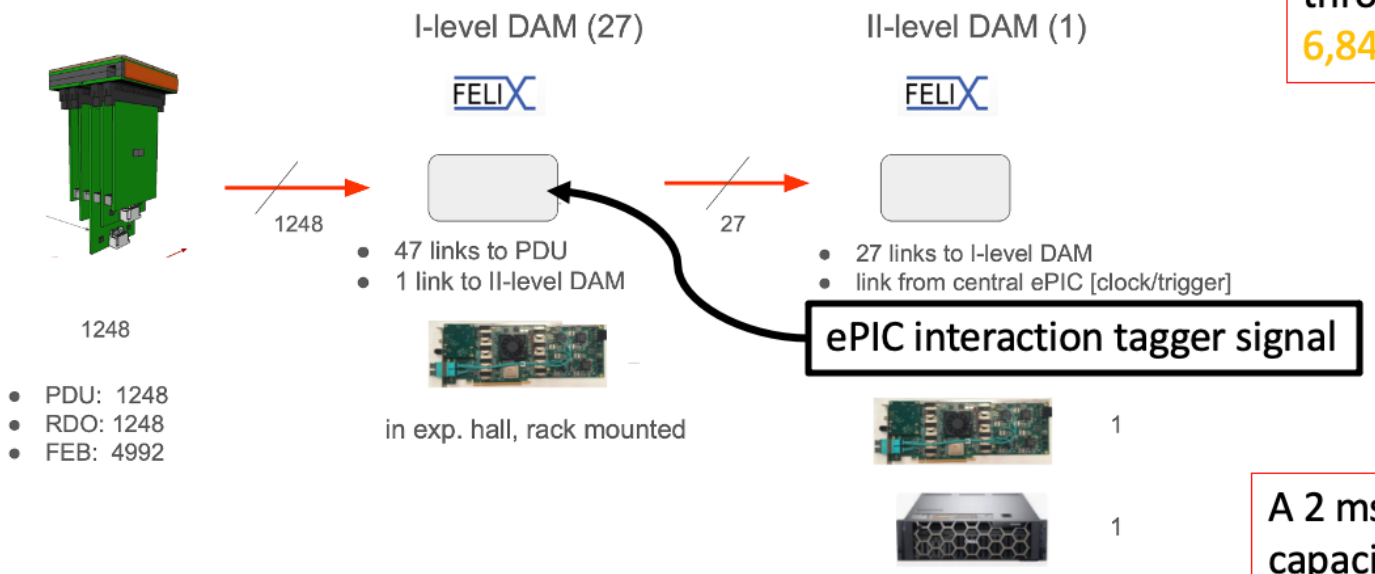
dRICH DAQ (from RDO to DAQ servers)

CURRENT BASELINE

Full dRICH data modeling understood: throughput will be really high only after several years of operations
- see ageing modeling and annealing procedures for SiPM DCR (backup and in pre-brief)
- see detailed data modeling throughput (backup)
- see J. Landgraf presentation

From electronics & DAQ PDR

dRICH DAQ design foresees two levels of DAMs:



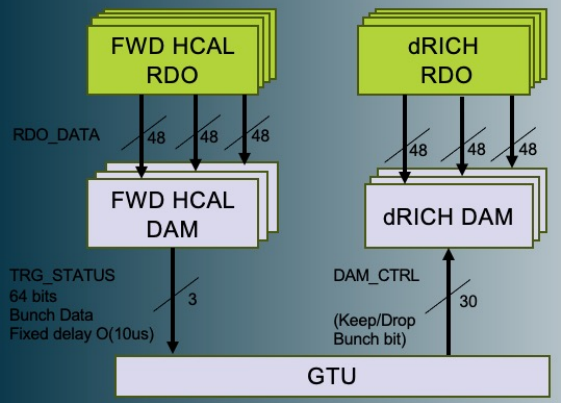
Feasibility studies for an interaction tagger are on-going providing a factor 100-200 reduction reducing throughput out of DAM (PCI memory) to:
6,84 Gbps - 70 Mbps

A 2 ms latency requires less than 1 MB buffering capacity in each DAM

How does it fit with ePIC DAQ? see Jeff slides for more details

Trigger Example: (dRICH tag based on external detector)

- *Given the requirement for a backup triggered readout for RICH, it is necessary to carefully define the physics trigge rate, trigger conditions, and trigger latency in order to facilitate design of the RICH front-end.*



ePIC depends upon a flexible scheme in which sufficient bandwidth is available for data to the dRICH DAM in the worst case. (> 4x safety). The selecting detectors (ex FWD HCAL) generate information characterizing beam in O(10us). The decision is made by the GTU and returned to DAM boards with fixed latency. The maximum latency is orders of magnitudes less than available buffering in DAM board memory. A hardware trigger is supported by the GTU but uses the same dRICH buffering scheme and delays as the firmware trigger option.

Activity	Notes
Data Arrives at DAMs	<=10us from Bunch Crossing
Data Evaluation in HCAL DAMs	100ns
TRG_STATUS to GTU	Data transmitted to GTU after fixed delay from source crossing O(10us)
Trigger Evaluation on GTU	Fixed Latency O(100ns)
Keep/Drop Bit to (dRICH) DAMs	Fixed Latency O(40ns)
Drop data / forward data	Drop/Forward after fixed time O(11us)
DAM Buffer	16GB
Buffer Time available	2.6 seconds

Ex: HCal generates trigger dRICH is triggered

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via GTU triggers info will be distributed to detectors

Example with FHCal, but the scheme is flexible:

- other detectors
- something originating from dRICH itself
- a combination (OR/AND) of the above

*Take home message

It does, no problem.

a dRICH track tagger?

see MarcoB slides for more details

A dRICH Interaction Tagger (dIT) integrated into the dRICH based on plastic scintillators that provide a prompt and fast signal (position-sensitive) of hadrons crossing the dRICH volume

Just in front of aerogel window within dRICH envelope, using dRICH readout

(note: in Marco's slides this proposal is called dRICH Interaxtion Tagger but during the meeting we rebaptized it dRICH Track Tagger = dTT)

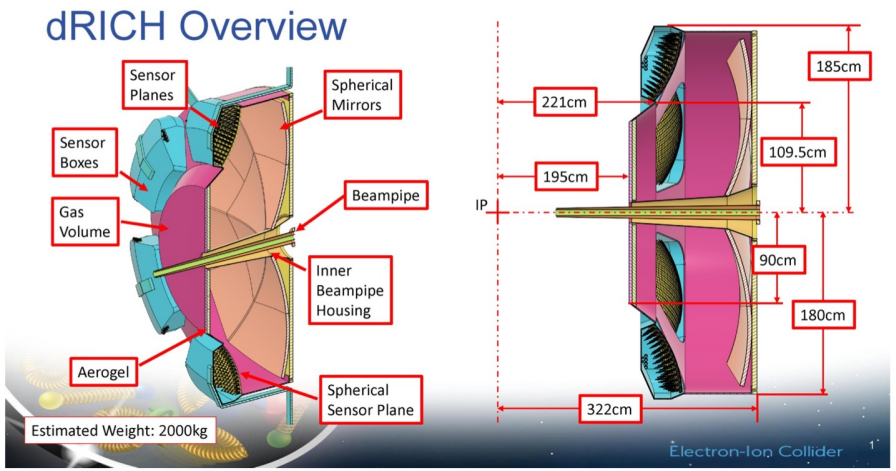
- Presented estimates of background (it seems manageable)
- similar to STAR/sPHENIX event plane detector (speak with Rosi!)
- Simulation + miniprototypes tests + tiles/fiber optimization + engineering checks neeeded
- Results by ePIC July 2025 (option could be mentioned in pre-TDR)

*Take home message

promising idea, obvioulys must be validated by studies. DAQ likes it ("seems robust and close the thing")

dIT preliminary design

- The signal/bg rate is not uniform on dRICH front face (larger in the central region)
- Preliminary ideas include:
  - a grid of V and H SciFi at 90°
  - a grid of diagonal 60 ° SciFi
  - small (~1x1 cm²) in the central region and large (~10x10 cm²) in the peripheral region plastic scintillator tiles



E.g:

- 2 layers, 1000 SciFi, 2 m long, and 0.5 cm ∅;
- SciFi:
  - attenuation length ~ 4 m
  - time rising edge ~ 100 ps
  - hit duration ~ 10-20 ns
- SciFi optical coupled with SiPMs cabled to RDOs;
- Two-sides readout → 4k SiPMs & 4k channels (dRICH 320k channels)
- 256 channels for RDO →need to add 16 RDOs
- Cost estimate: ~ $150k

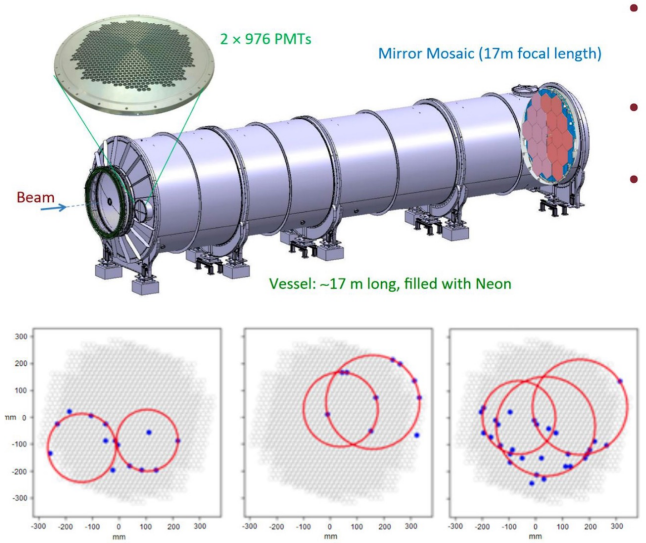
dRICH Interaction Tagger (dIT) 8

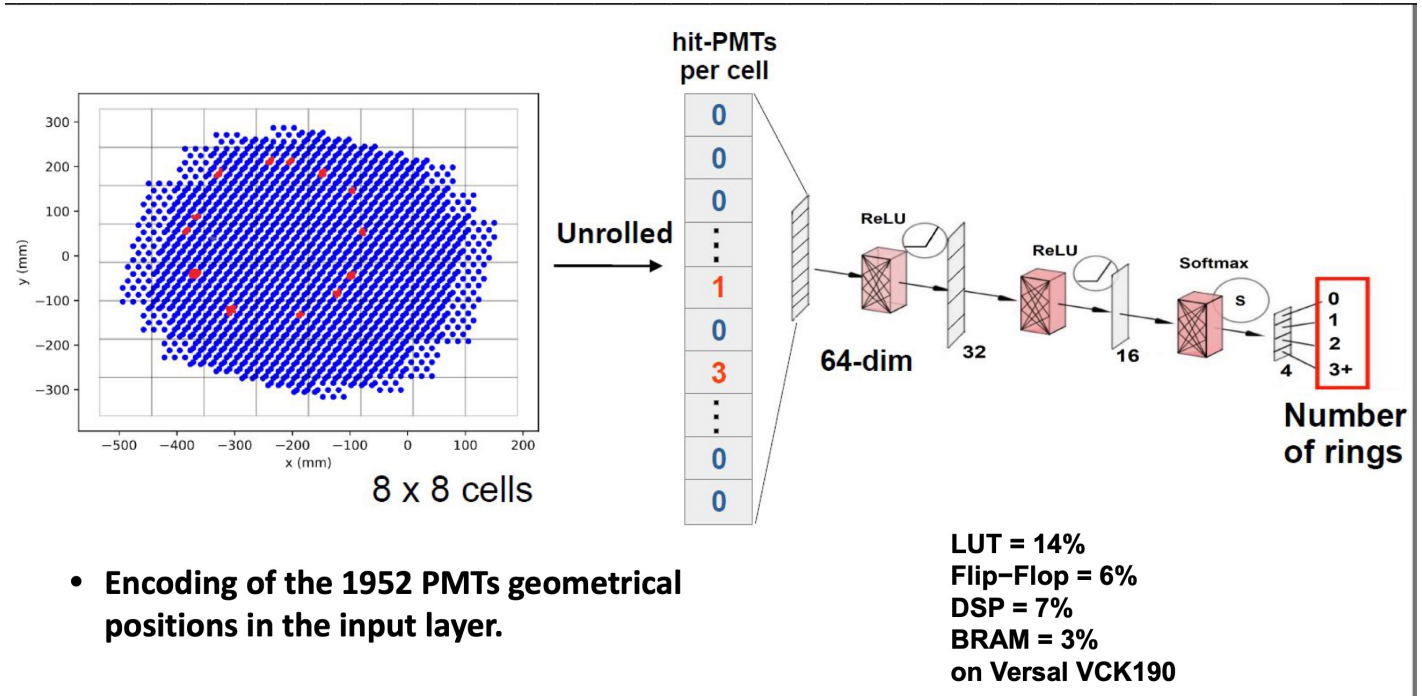
dRICH data filtering

see Luca slides for more details

Design Ideas for an Online Data Reduction System for the ePIC dRICH Detector

Extensive experience from INFN RM and INFN RM-TV on algorithms deployed on FPGA and GPU
RICH know-how from NA62 pattern recogniton (NN on FPGA)





- **Encoding of the 1952 PMTs geometrical positions in the input layer.**

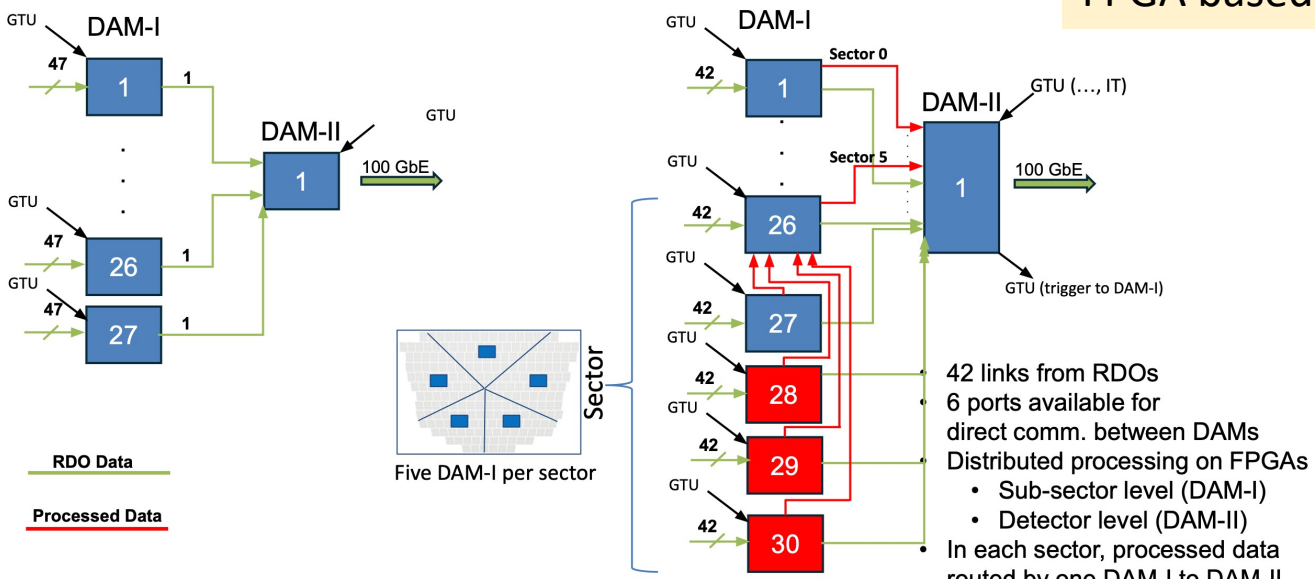
The groups are working on simulated dRICH data, a tagger signal would complement their work (as extra-input to seed reconstruction

dRICH data filtering (2)

see Luca slides for more details

dRICH Data Reduction Stage on FPGA: example deployment

FPGA based scheme



42 links from RDOs
6 ports available for direct comm. between DAMs
Distributed processing on FPGAs
- Sub-sector level (DAM-I)
- Detector level (DAM-II)

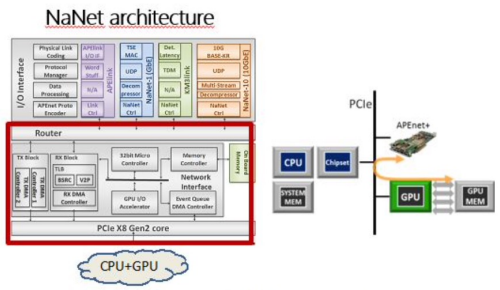
In each sector, processed data routed by one DAM-I to DAM-II

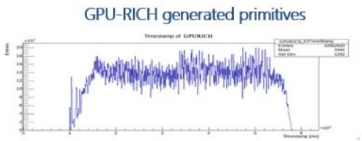
100 GbE+GPU based scheme

From HPC to HEP: NaNet Project

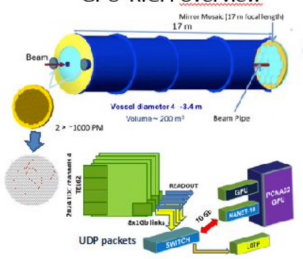
NaNet: Design and implementation of a family of FPGA-based PCIe Network Interface Cards:

- Bridging the front-end electronics and the software trigger computing nodes.
- Supporting multiple link technologies and network protocols.
- Optimizing data transfers with GPU accelerators.
- Enabling a low and stable communication latency.
- Having a high bandwidth.
- Processing data streams from detectors on the fly (data compression/decompression and re-formatting, coalescing of event fragments, …).



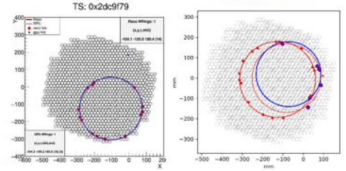


	NaNet-1	NaNet³	NaNet-10	NaNet-40
Year	Q3 - 2013	Q1 - 2015	Q2 - 2016	Q3 - 2019
Device Family	Altera Stratix IV	Altera Stratix V	Altera Stratix V	Altera Stratix V
Channel Technology	1 GbE	KM3link	10 GbE	40 GbE
Transmission Protocol	UDP	TDM	UDP	UDP
Number of Channel	1	4	4*	2
PCIe	Gen2 x8	Gen2 x8	Gen3 x8**	Gen3 x8
SoC	NO	NO	NO	NO
High Level Synthesis	NO	NO	NO	YES
nVIDIA GPUDirect RDMA	YES	YES	YES	YES
Real-time Processing	Decomp.	Decomp.	Decomp. Merger	?



GPU 1 ring == Reco 1 ring

GPU 1 rings
Reco 2 rings

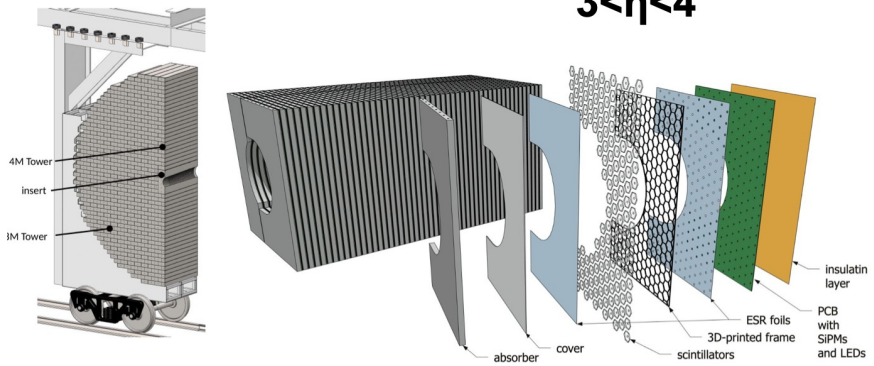


*Take home message

Studies with simulated data critical to define best solution to deploy

dRICH track tagger using FHCal

see Miguel slides for more details



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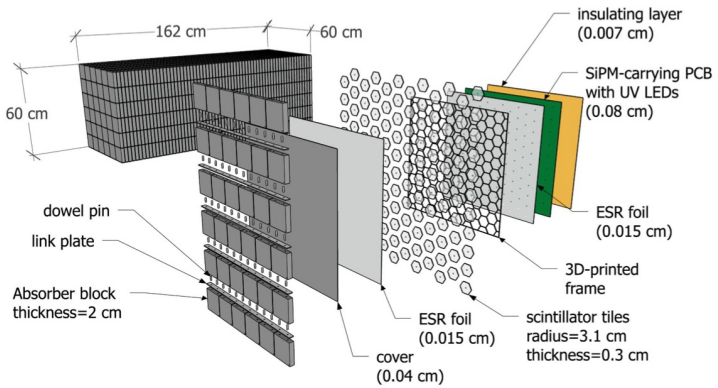
M. Arratia et al. *NIMA 1047 (2023) 167866*



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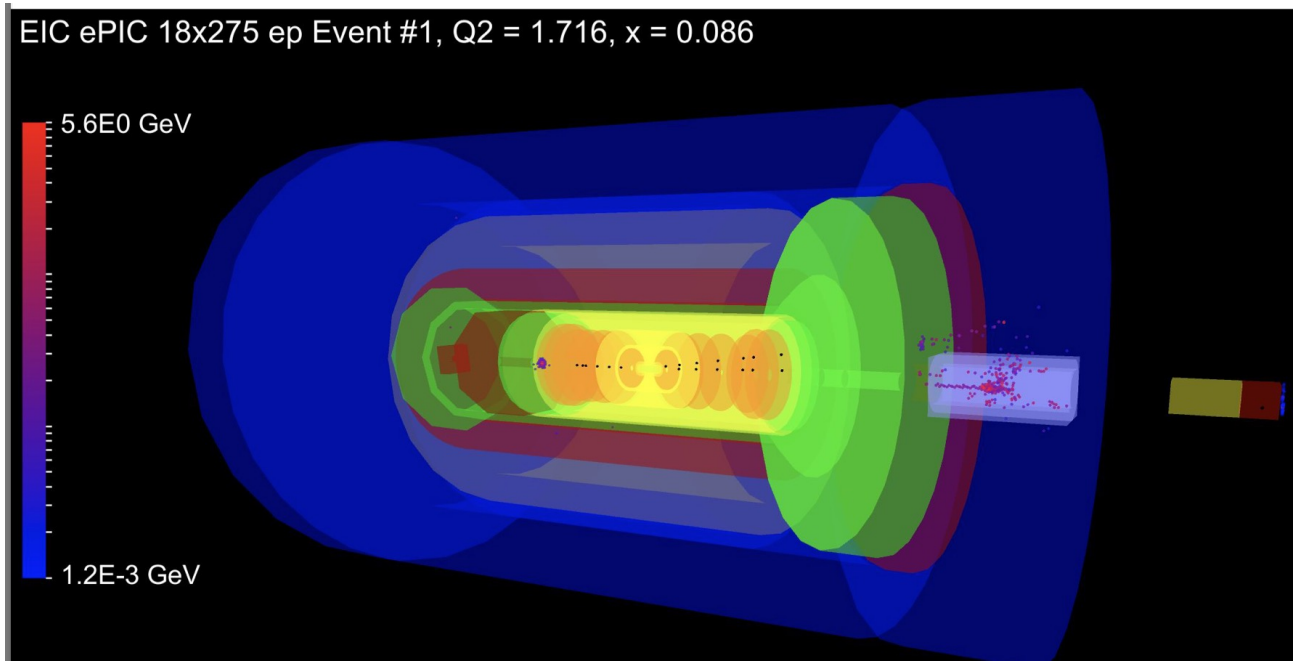
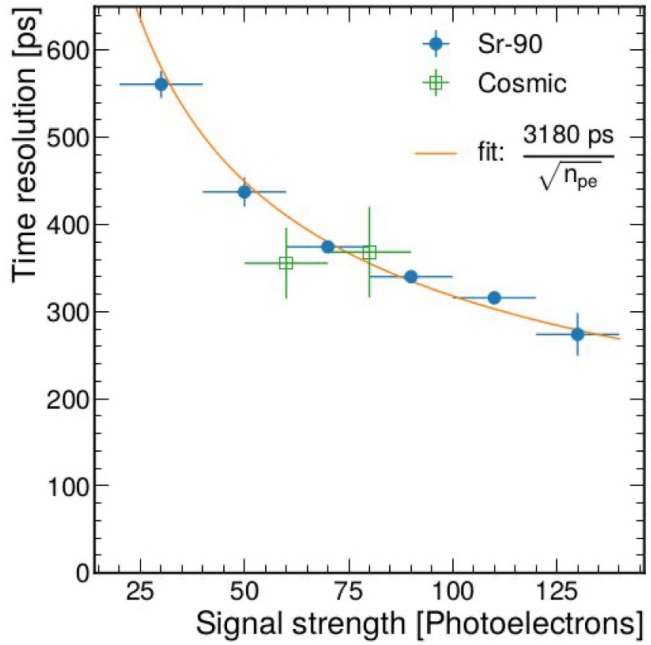
R. Milton et al. arXiv:2406.12877



FHCAL could detect tracks (at MIP level) with high efficiency for dRICH

time resolution is ok



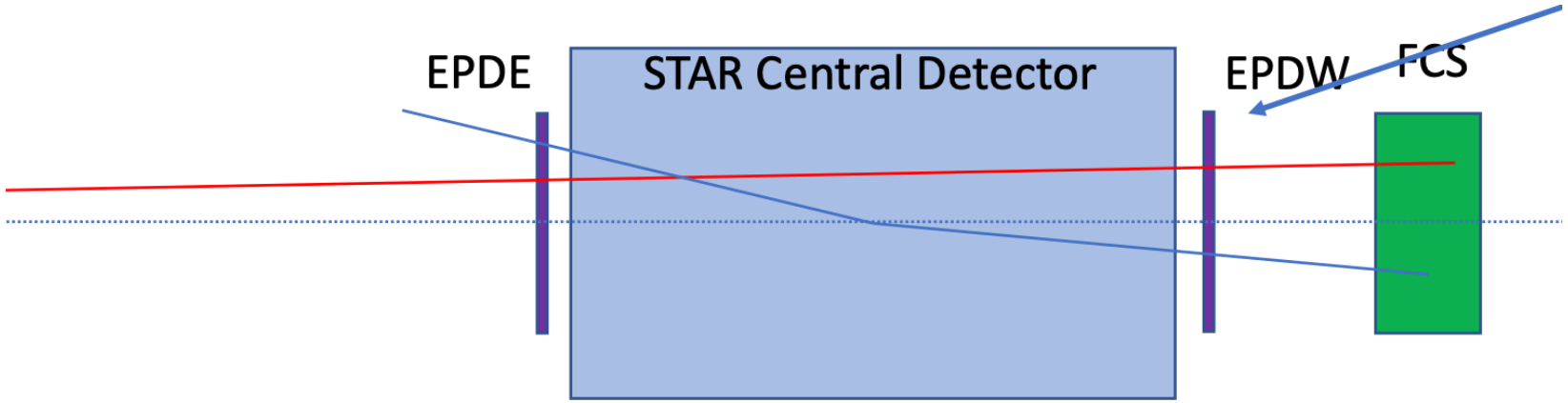
*Take home message

FHCAL can play role for both:
- "dRICH track tagging"
- minimum bias interaction trigger

dRICH track tagger using FEMcal

see Oleg slides for more details

Talk based on STAR experience (trigger based) and FCS experience
Stressed importance of EPD (Event Plane Detector @ STAR/sPHENIX) – dTT has similar design



re-use EPD from STAR not possibile (Elke) but dTT can offer that ("West")
FEMCal cannot distinguish between electrons and photons, but still can tag electrons not reaching FHCal

*Take home message

FEMCall can provide further complementing information for dRICH track tagging
We will certainly speak with EPD experts to share know how/design ideas tetc.

Conclusions/Action points

- ✓ No data reduction need at EIC day-0. We will use NONE of all these tools immediately, we will tune taggers and data filtering with real data during EIC first years of operation.
- ✓ The dRICH data throughput is something understood, manageable and we have an array of solutions to handle it
- ✓ an unbiased minimum-bias interaction tagger for ePIC is a wider problem

- get estimates of radiation load during "early EIC Science Program"
- dTT proposal needs to make obviousl scientific due diligence to proof the concept
  → 1 year/in time for TDR
- FHCal / FEMCal need to be quantitatve on what they can provide at DAM level to GTU
- data filtering: test algorithms, understand between FPGA / GPU solutions
- we couldn't hear from AC-LGAD TOF due to concurrent TOF workfest. But we will do (note for organizers: FPGA and GPU can work in a highly parallelized way, human beings not. 😄)