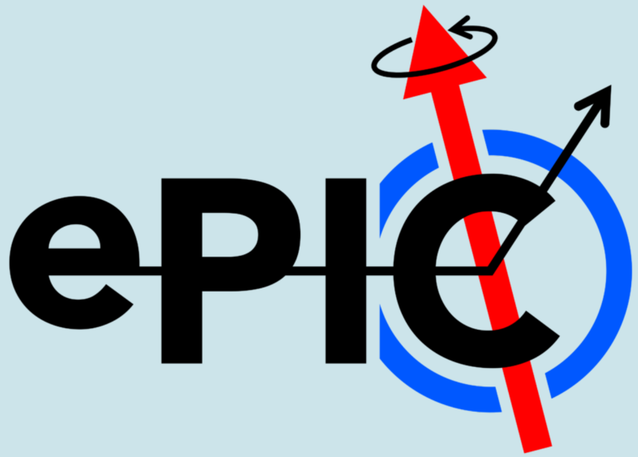


Barrel TOF status

Satoshi Yano (Hiroshima University)

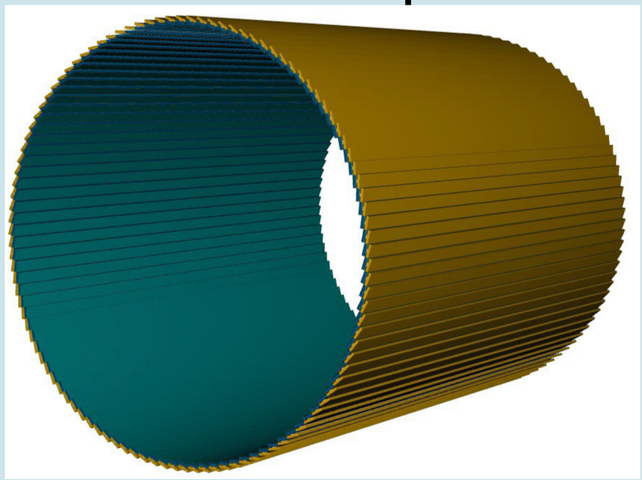
ePIC Collaboration meeting @ Rehigh University

07/26/2024

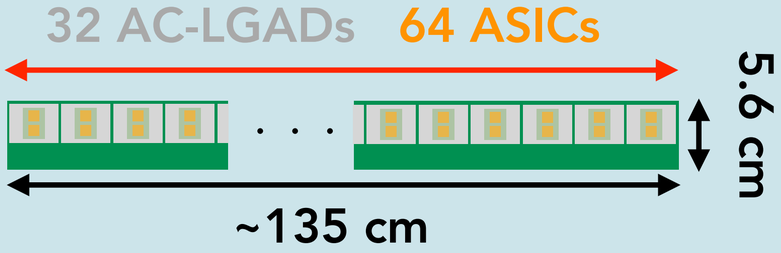
Detector Layout of BTOF

- BTOF is composed of 288 half staves to form a cylindrical shape
- 32 AC-LGAD **strip-type** sensors are attached to one half stave
  - Two ASICs are placed just above one sensor (several options)
- Radius is 63 - 66 cm from the beam pipe covering $-1.42<\eta<1.77$
- Total material budget in acceptance is ~0.01 X/X_0

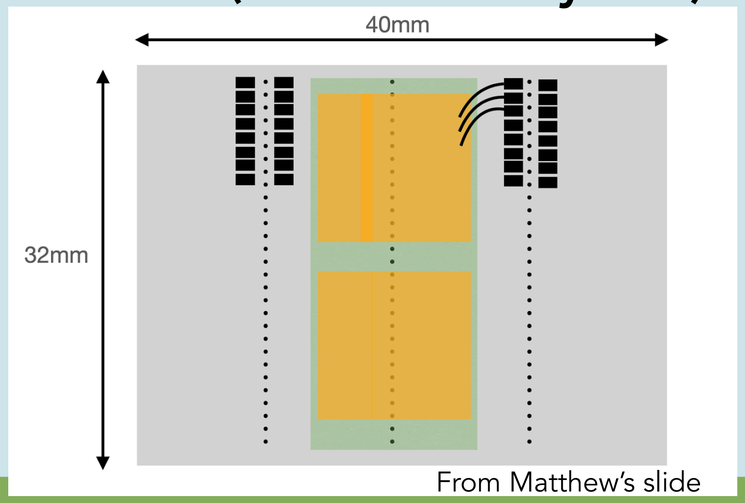
BTOF shape



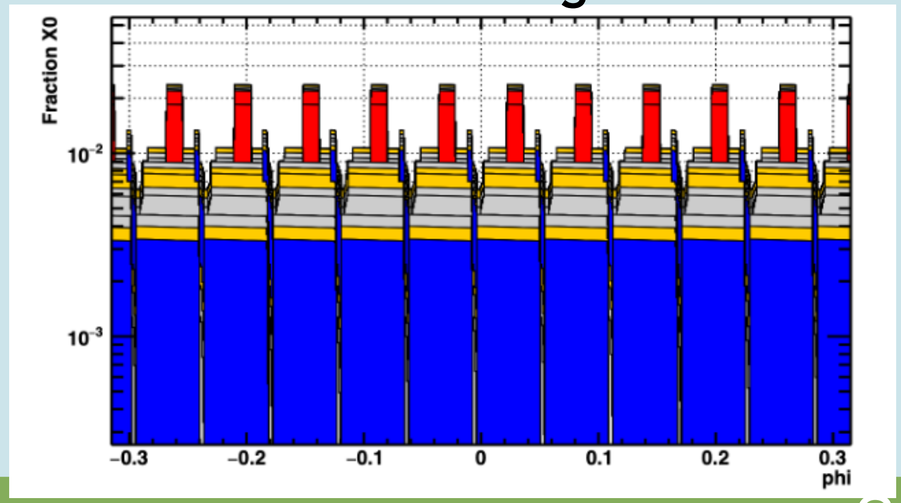
BTOF Half stave



Module (Sensor-ASIC hybrid)

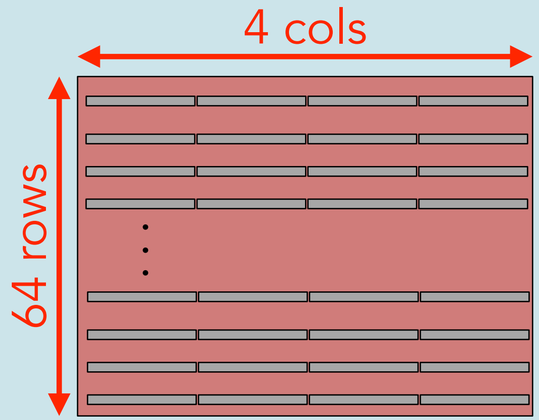


Material budget



BTOF AC-LGAD sensor

- Strip-type sensor, 3.2 x 4 cm^2 sensor size with 0.5 x 10 mm^2 metals, is used in BTOF



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  - **11 m^2**
  - **2.4 M readout channels**

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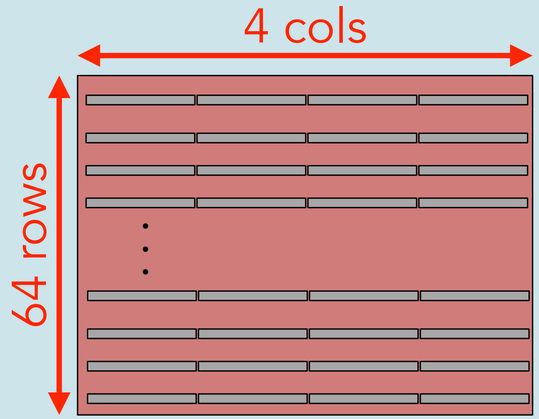
  - Gain and DC have temperature dependences
  - Performance redundancy should be considered



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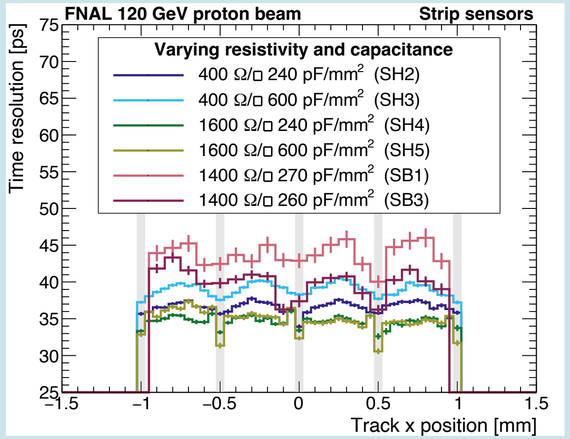

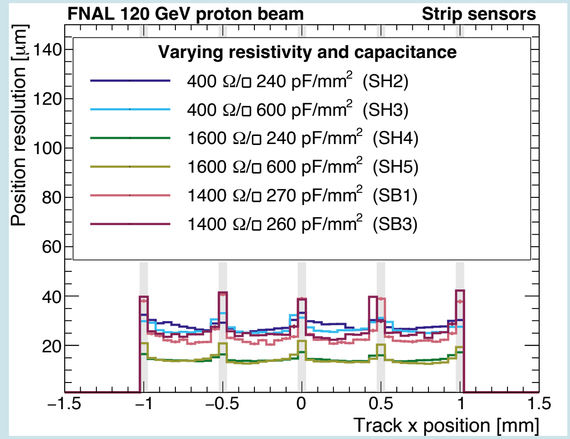

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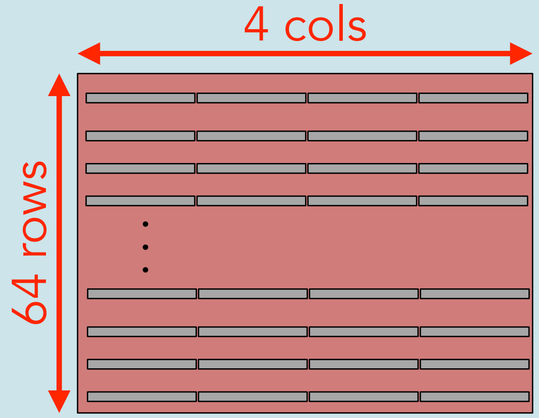
- Validation with full-size sensors and study of the uniformity of the performance (gain and temperature dependence) will be critical in FY25



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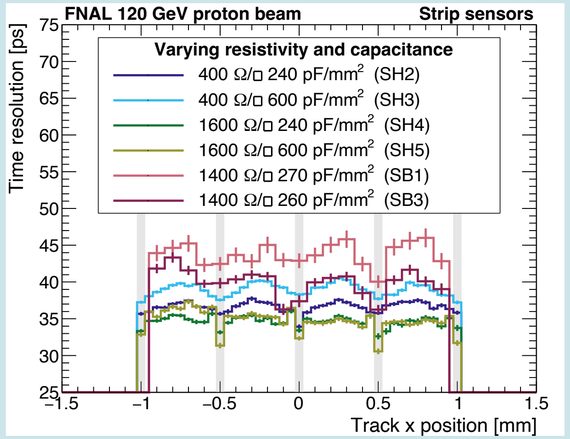

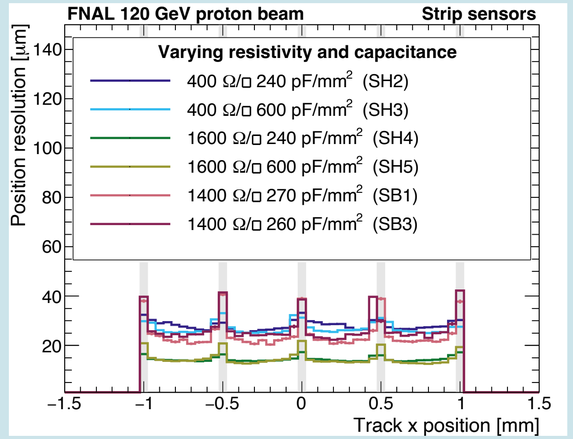

Frontend ASIC

- Required functional requirements are,
  - Input charge: 1~30 fC (document)
  - Input capacitance: ~10 pF
  - Jitter: < 20 ps
  - Clock: ~98.5 MHz
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- Several options of ASIC for the strip-type AC-LGAD readout
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- Showstopper of each candidate
  - FCFD: Analog block is OK. How about digital block design and fabrication? When?
  - HGCROC: checking the compatibility with the strip-type sensors is necessary. How to get it? From who?
  - EICROC: Analog block re-design is necessary to match larger input capacitance. who and when?

Support structure and temperature control

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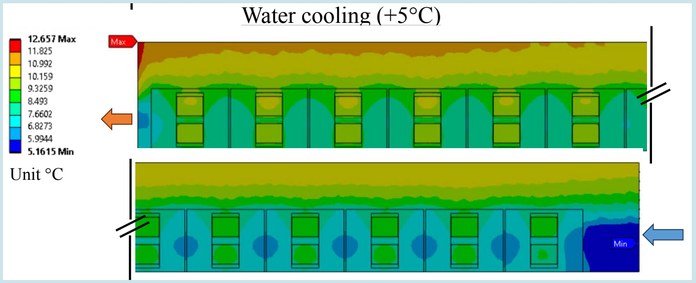
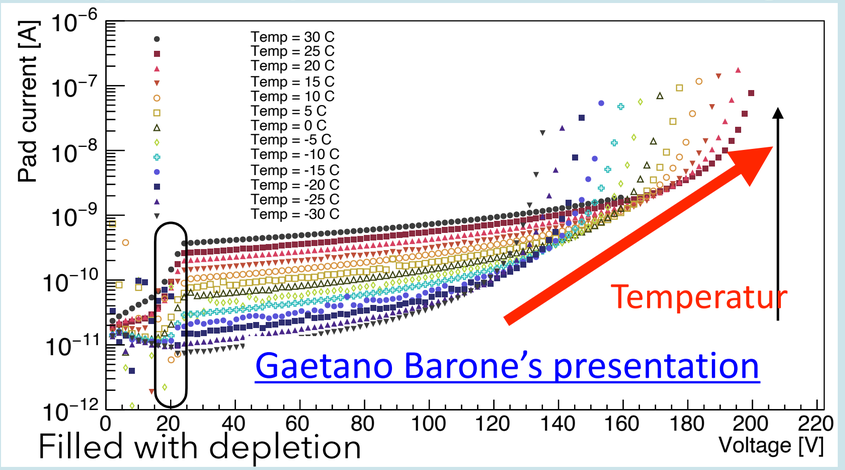
- Long stave has a temperature gradient inlet and outlet of the cooling pipe
  - Deteriorate the uniformity of the sensor performance
  - Need precise monitoring and need complicated operations (ex, supply different bias voltages according to temperature readings while taking data)
  - Low material FPC avoids making many HV lines

sPHENIX INTT FPC

Full-size stave test with simulation



Temperature dependence of breakdown voltage



Key items for BTOF design

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- NOTE: In general, the lower power consumption ASIC is preferred. However, as long as the cooling system can manage, the larger power consumption ASIC is still acceptable.

Summary of checking list before pre-TDR

- The checking list for pre-TDR
  - How much material budget is allowed
  - How much performance variation is seen by the temperature variation
  - How much temperature variation is allowed
  - How much power consumption is allowed with various stave designs and cooling design

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  - How much material budget is allowed
  - How much performance variation is seen by the temperature variation
  - How much temperature variation is allowed
  - How much power consumption is allowed with various stave designs and cooling design

- The fastest full-chain prototype would be the one using HGCROC with full-size HPK sensors
  - HGCROC compatibility with sensors (HPK and BNL)
  - ppRDO should be designed with HGCROC
    - ppRDO is being developed with ETROC2 for FTOF as of now

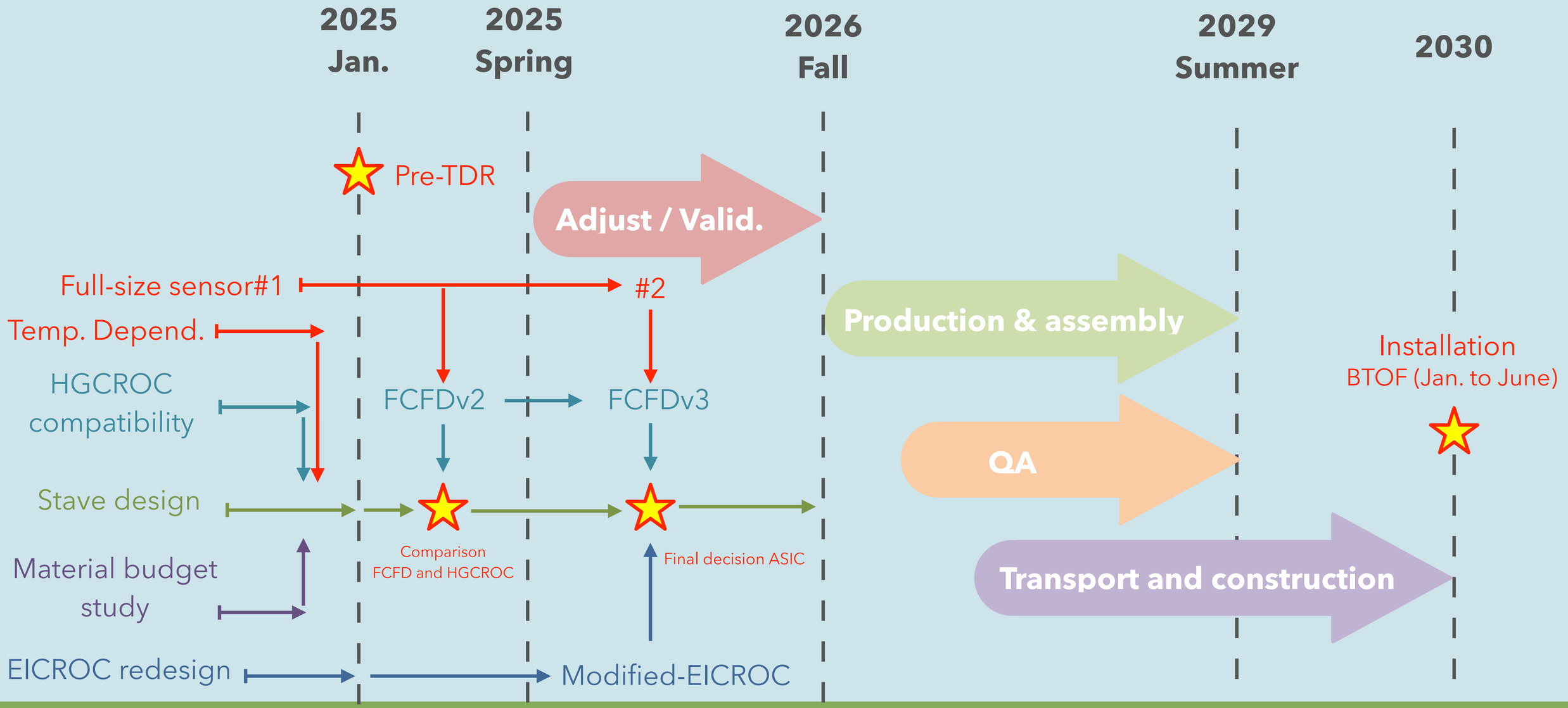
Budgetary requests from Japan to support BTOF project

- The Japanese team is requesting a large amount of budget from next FY25 in Japan (April 2025~)
  - $10M for 7 years for BTOF including R&D with eRD112 and eRD109 and mass production (for infrastructures, sensor, ASIC, FPC, RDO, …)
  - Decision for next year's budget will possibly come by the end of this year.

  - https://japannews.yomiuri.co.jp/science-nature/science/20240515-186185/

Backup

BTOF schedule

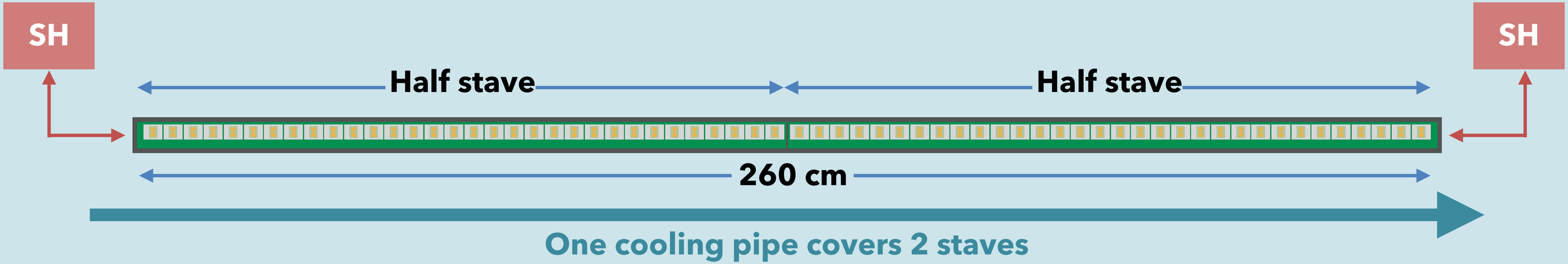


Power consumption of BTOF

- BTOF power consumption is larger than the FTOF due to the size difference
- SH (Readout board and Power board) of BTOF is located in a different place than sensors + ASICs
- Each SH provides ~20 W to a stave
- One cooling pipe covers 2 staves ~40 W power consumption

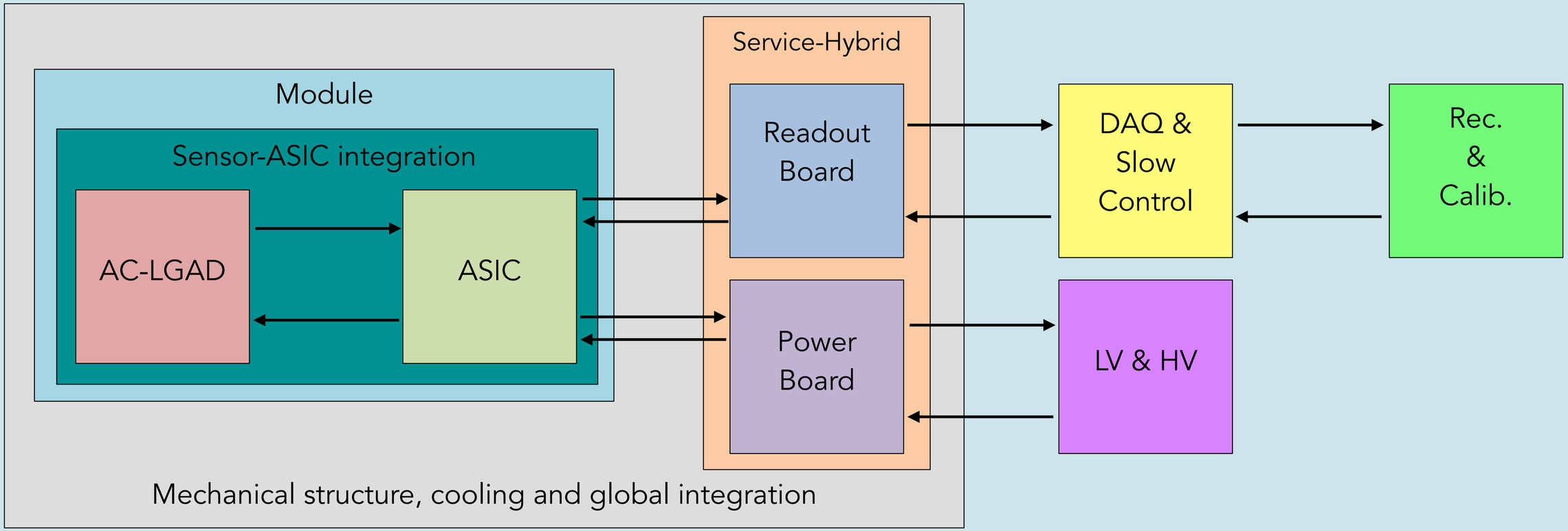
BTOF

	Power
Sensors+cable	0.6 kW
ASIC (2mW/ch)	4.7 kW
DC-DC	3.3 kW
FPGA	1 kW
Total	9.6 kW



Main heat source is ASIC, so the location of ASIC and sensors should be designed very carefully to minimize the temperature gradient effects

TOF system structure



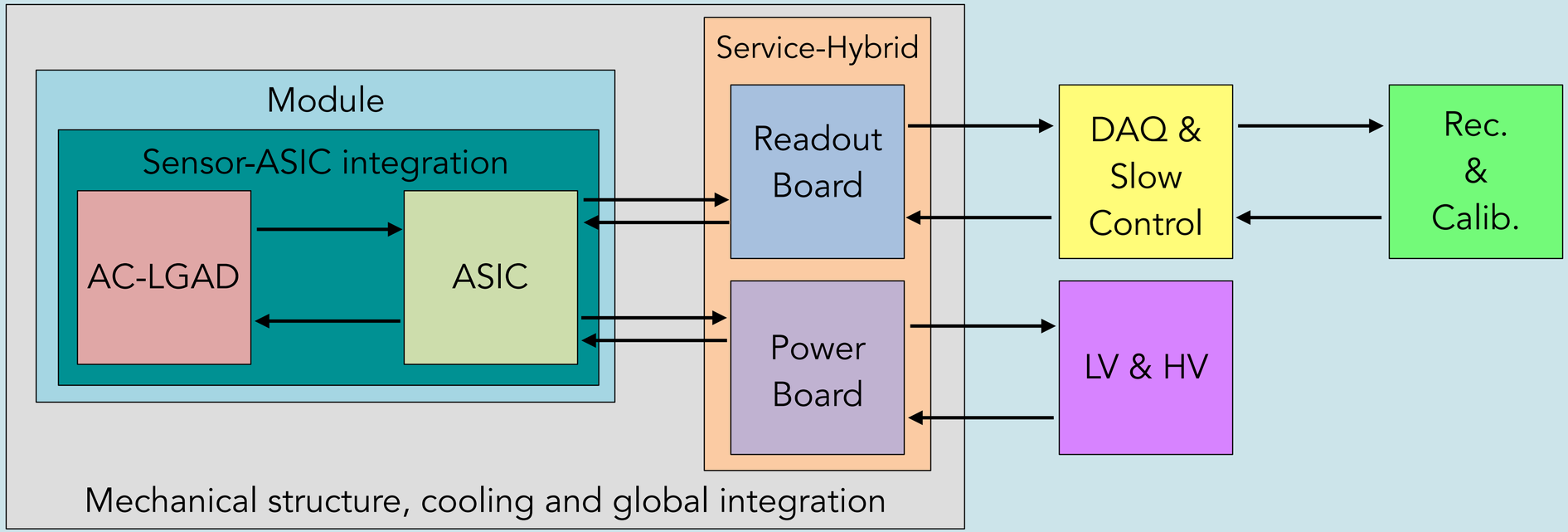
Institutes in TOF tasks (official)

- Brookhaven National Laboratory (USA)
- Fermi National Accelerator Laboratory (USA)
- Rice University (USA)
- Oak Ridge National Laboratory (USA)
- Ohio State University (USA)
- Purdue University (USA)
- University of California Santa Cruz (USA)
- University of Illinois at Chicago (USA)
- Hiroshima University (JP)
- RIKEN (JP)
- Shinshu University (JP)
- Nara Woman University (JP)
- National Chen-Kung University (TW)
- National Taiwan University (TW)
- IJCLab, OMEGA, CEA-Saclay (FR)

Tasks in BTOF

- **AC-LGAD sensor**
  - BNL
  - ORNL
  - Univ. of California, Santa Cruz
  - Univ. of Illinois, Chicago
  - Hiroshima University
  - Shinshu University
- **Frontend ASIC**
  - Fermilab
  - Rice University
  - ORNL
  - Hiroshima University
  - National Taiwan University
  - IJCLab/OMEGA/CEA-Saclay
- **Sensor-ASIC integration**
  - BNL
  - ORNL
  - Univ. of California, Santa Cruz
  - Univ. of Illinois, Chicago
  - National Taiwan University
- **Module structure**
  - Purdue University
  - National Cheng-Kung University
- **Module assembly**
  - BNL
  - ORNL
  - Ohio State University
  - Univ. of California, Santa Cruz
  - Hiroshima University
  - RIKEN
  - Nara Woman University
  - National Taiwan University
- **Flex PCB**
  - ORNL
  - Nara Woman University
- **Service Hybrid**
  - Rice University
- **Backend electronics**
  - BNL

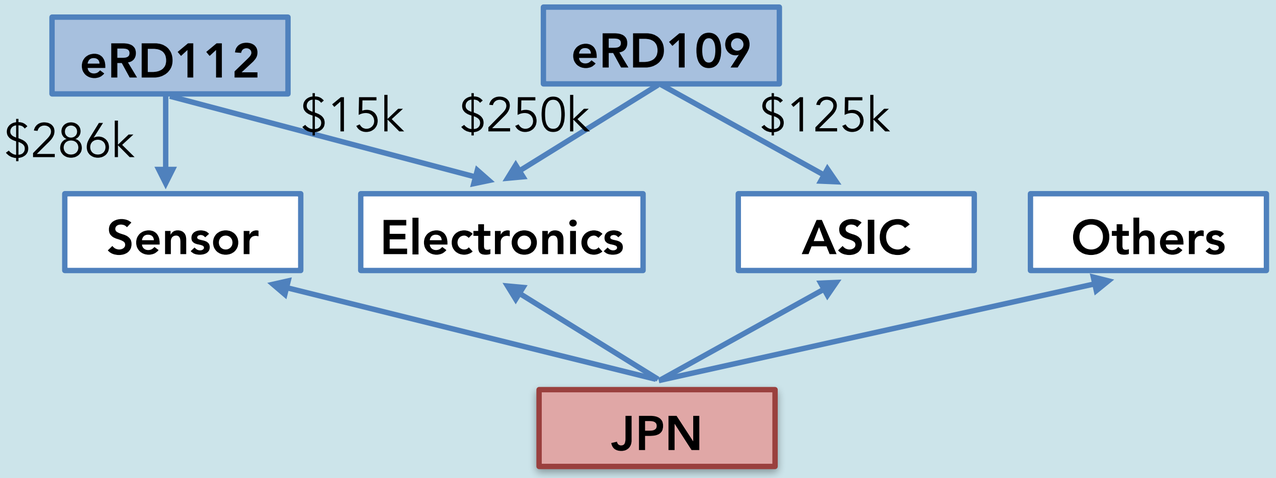
TOF structure

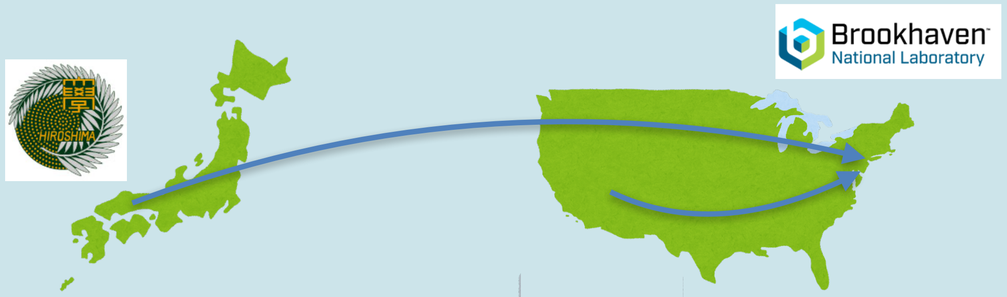


- **Barrel-TOF (BTOF)**
  - Strip-type AC-LGAD
  - ASIC (FCFD)
  - Sensor-ASIC integration
  - Module
  - Service-Hybrid
  - Mechanical structure
  - Global integration
- **Forward-TOF (FTOF)**
  - Pixel-type AC-LGAD
  - ASIC (EICROC)
  - Sensor-ASIC integration
  - Module
  - Service-Hybrid
  - Mechanical structure
  - Global integration
- **Common system**
  - DAQ
  - Cooling
  - Software (Rec. & Calib.)
  - HV & LV
  - Slow control

Strengthening cooperation with the U.S. and JPN

- We believe that strong and efficient cooperation between Japan and eRD can solve the problems we have now
  - We have just started to think and make the strategy between eRD112, eRD109, and JPN for R&D
  - We have to think about assembling and construction strategy





- Clean room (~100m^2) construction is just starting at Hiroshima
  - Different resource from the requesting one
  - Main purpose is BTOF assembling