# **ePIC** Forward TOF overview

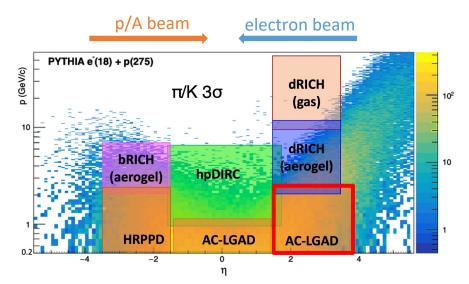
Wei Li (Rice University)

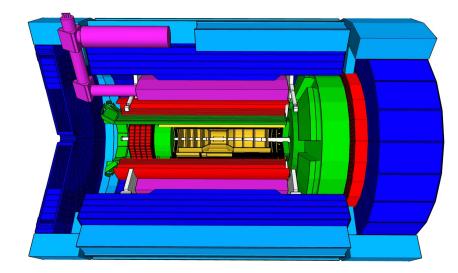
TOF and AC-LGADs Workfest@ePIC collaboration meeting July 26, 2024

BROOKHAVEN

Jefferson La

### AC-LGADs TOF system for PID





#### Latest envelope (link)

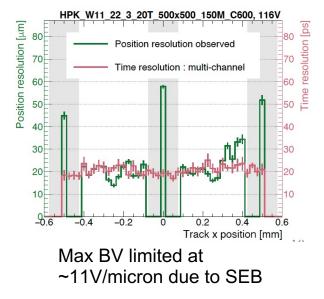
Detector	r (cm)	z (cm)	Momentum range for $3\sigma \pi/K$ separation
Barrel TOF	62 <r<69.5< td=""><td>-117.5<z<171.5< td=""><td><math>0.2 &lt; p_T &lt; \sim 1.2 \text{ GeV}</math></td></z<171.5<></td></r<69.5<>	-117.5 <z<171.5< td=""><td><math>0.2 &lt; p_T &lt; \sim 1.2 \text{ GeV}</math></td></z<171.5<>	$0.2 < p_T < \sim 1.2 \text{ GeV}$
Forward TOF	10.5 <r<60< td=""><td>185<z<193< td=""><td>0.2 &lt; p &lt; ~2.3 GeV</td></z<193<></td></r<60<>	185 <z<193< td=""><td>0.2 &lt; p &lt; ~2.3 GeV</td></z<193<>	0.2 < p < ~2.3 GeV

#### z thickness is now 8 cm, instead of 15 cm

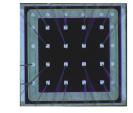
### FTOF requirements and R&D progress

#### Current requirements (presented at FY23 EIC Project R&D - DAC Meeting)

	Area (m <sup>2</sup> )	Channel size (mm <sup>2</sup> )	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10	0.5*10	2.4M	30 → 35 ps	30 $\mu m$ in $r \cdot \varphi$	0.01 X <sub>0</sub>
Forward TOF	1.4	0.5*0.5	5.6M	25 ps	30 $\mu m$ in x and y	$0.08 \rightarrow 0.025 X_0$
B0 tracker	0.07	0.5*0.5	0.28M	30 ps	20 $\mu m$ in x and y	$0.01 \rightarrow 0.05 X_0$
RPs/OMD	0.14/0.08	0.5*0.5	0.56M/0.32M	30 ps	140 $\mu m$ in x and y	no strict req.



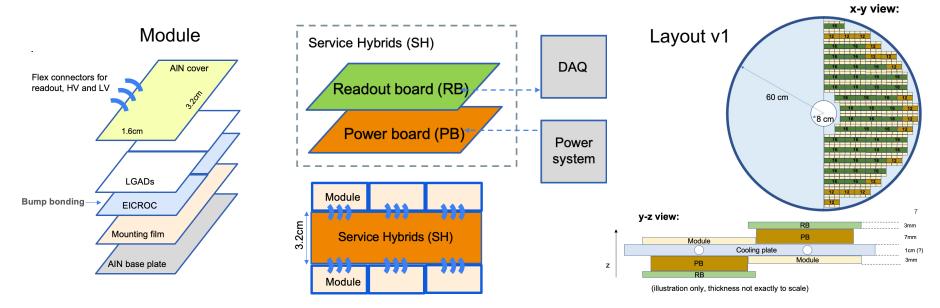
#### HPK Pixel Sensor (2x2 mm<sup>2</sup>)



Promising to achieve the requirements with 20micron thick, 0.5x0.5mm<sup>2</sup> pixel sensors Large sensors (32x32, 64x32) being produced by HPK and will be evaluated later this year



#### Initial FTOF layout design from the Jan. collaboration meeting



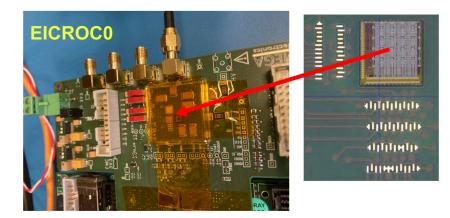
Continue refining the design in light of ongoing SH and module prototyping efforts

- Each SH servicing up to 32 ASICs (previously 16)
- Reduced envelope in z requires us to be more cautious with the layout design

### **FTOF ASICs - EICROC**

ASIC requirements:

- Pixel size: 0.5x0.5 mm<sup>2</sup>
- Low jitter: <20ps
- Low power consumption: 1mV/channel

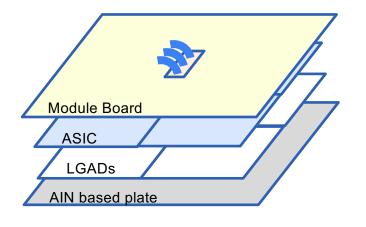


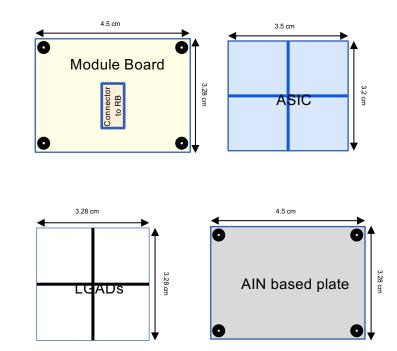
EICROC0 (4x4): first version LICROC1 (8x32?): intermediate size LICROC2 (32x32): full size LICROC3 (32x32): final (if needed)

See talk by Christophe et. al. for latest development

## FTOF module (updated)

- 4 AC-LGADs sensor per module
- Each sensor: 32x32 pixels and 1.6x1.6 cm<sup>2</sup>

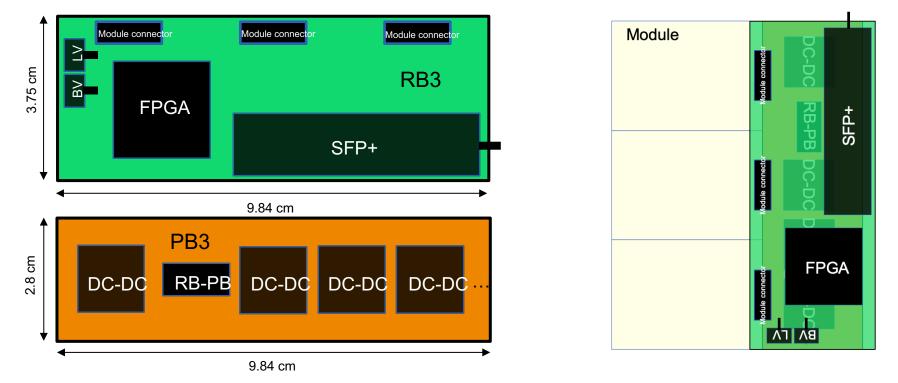




More realistic dimensions considering guard rings, mounting holes etc.

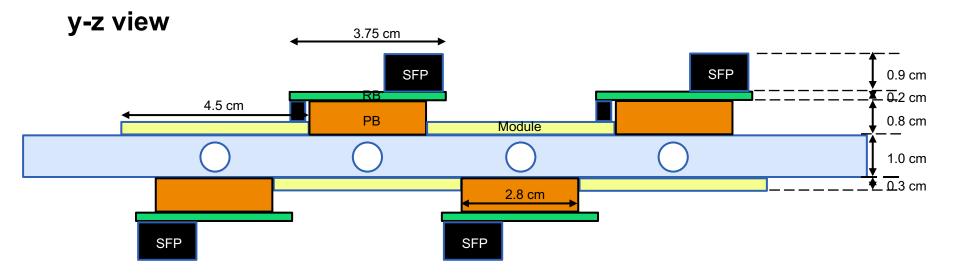
### Service hybrids design and prototyping

Shortest readout (RB3) and power (PB3) board serving 3 modules or 12 ASICs



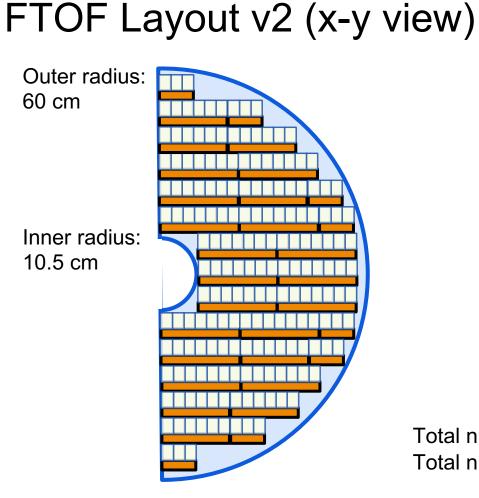
Another two longer versions serving 6 and 7 modules, or 24 and 28 ASICs

#### FTOF detector layout v2



Total thickness is about 5cm, which would fit within 8cm z-envelope

- Thickness of cooling and support structure still uncertain
- Need to take into account routing of cables and fibers as well



Row	modules	RB3	RB6	RB7	All RBs
1	3	1	0	0	1
2	9	1	1	0	2
3	12	0	2	0	2
4	14	0	0	2	2
5	16	1	1	1	3
6	17	1	0	2	3
7	14	0	0	2	2
8	14	0	0	2	2
9	14	0	0	2	2
10	17	1	0	2	3
11	16	1	1	1	3
12	14	0	0	2	2
13	12	0	2	0	2
14	9	1	1	0	2
15	3	1	0	0	1
Sum	184	8	8	16	32

Total number of modules: 184\*4 = **736** Total number of service hybrids: 32\*4 = **128** 

#### Channel counts and power budget

	Counts		Power
Modules	736	Sensors	0.3kW
Sensors/ASICs	2944	EICROC	2.9kW
Data fiber pairs	128	DC-DC	2kW
LV cable pairs	128	FPGAs	0.5kW
HV cable pairs	128	Total	5.7kW

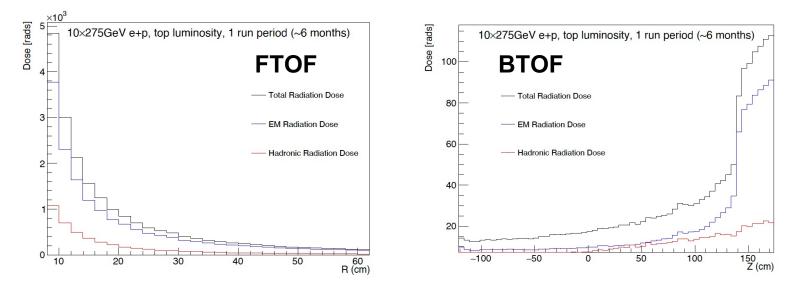
Assuming a single value of HV for each SH

Channels and power budget reduced from v1 by  $\sim$ 30% mainly because of the reduced envelope and # of SHs

#### **FTOF** radiation dose

#### Signal+beam gas (updated)

#### Xiao Huang



Assuming 10 years of operation and a safety factor of 2, the most inner part of FTOF expects ~ 100 kRad

## Summary

FTOF has been making steady progress toward the final design

- Pixel AC-LGADs sensors of 20 microns in thickness meets the FTOF requirements. Next step is to scale up to large sensors to evaluate their performance and yields.
- EICROC1 design is in progress.
- Service hybrids design and prototyping are progressing very well (see details later in the frontend electronics talk).
- Refined layout design v2

Still lots of work and challenges ahead. We highly welcome more institutes/colleagues to join the efforts and take leading roles!

# Backups