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Fermilab Constant Fraction Discriminator Readout Chip

***A. Apresyan**, M. Barria, I. Dutta, A. Hayrapetyan, S. Los, C. Madrid, C. Pena, C. Perez, V. Sepulveda, C. Valenzuela, S. Xie, T. Zimmerman*

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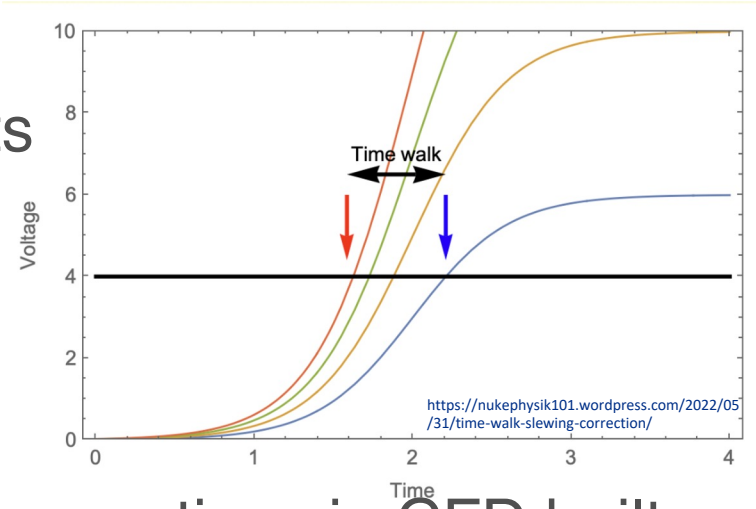
Hardware-enabled CFD Readout for Timing Detectors

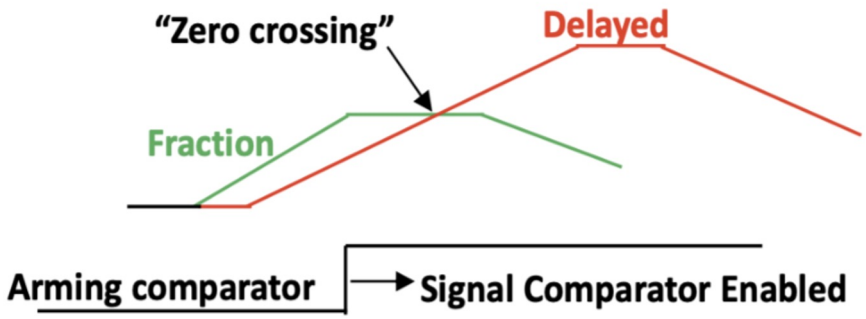
- Time-walk effect is well known & must be corrected for best performance
- Conventionally addressed with online or offline corrections via some type of LUT
- But under harsh radiation environments of future colliders, corrections may be time-dependent and messy!



- We implemented a hardware-enabled correction via CFD built into the readout ASIC design

Fermilab CFD Chip Design

- Primary application is (AC-)LGAD sensors for MIP signals
- But can be used for many types of precision timing detectors
- Main features of the CFD are:
  - Integrator & Follower to create the “fraction” signal
  - Comparators for “arming” and timestamping



A. Apresyan et. al, **NIM A 1056, 2023, p168655**
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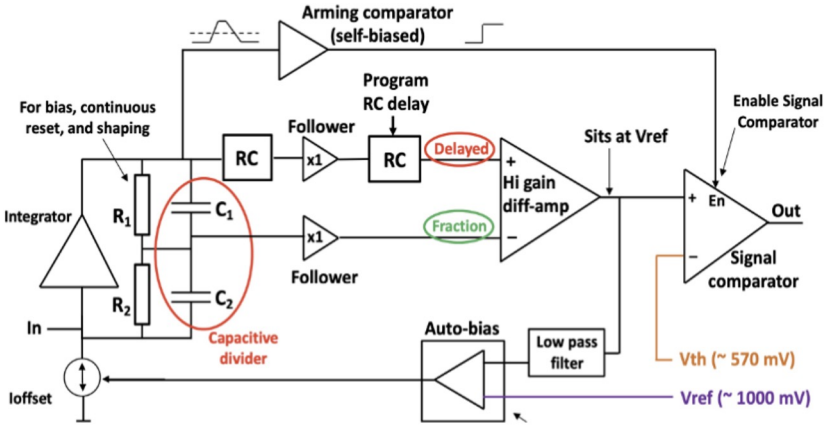

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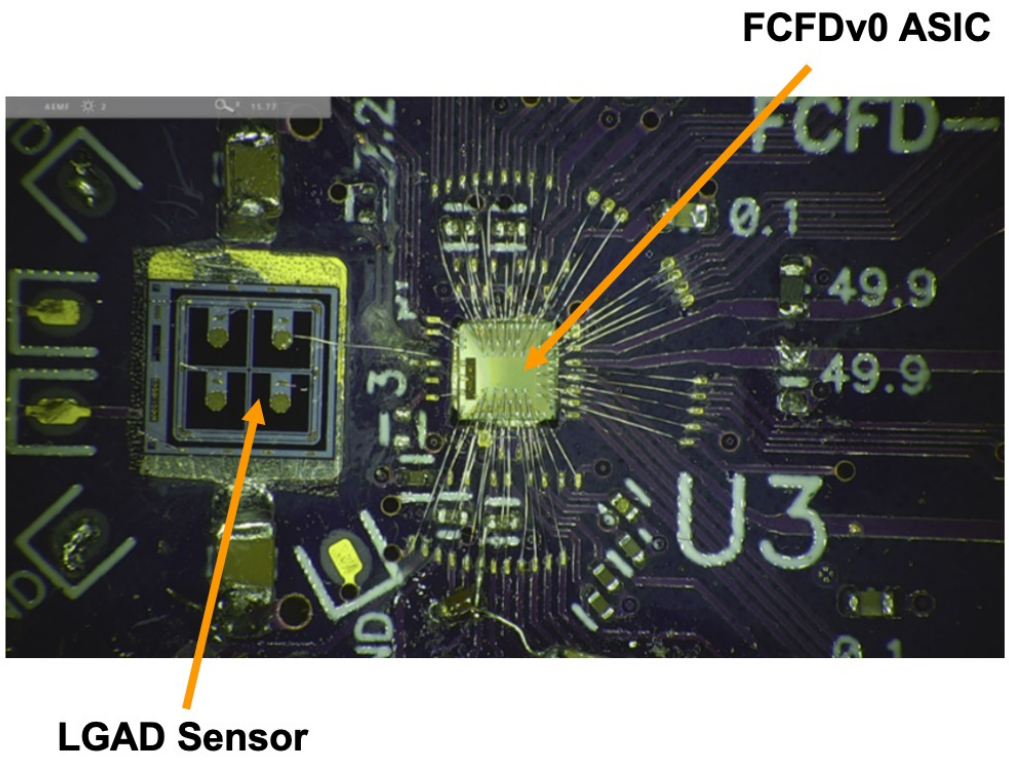
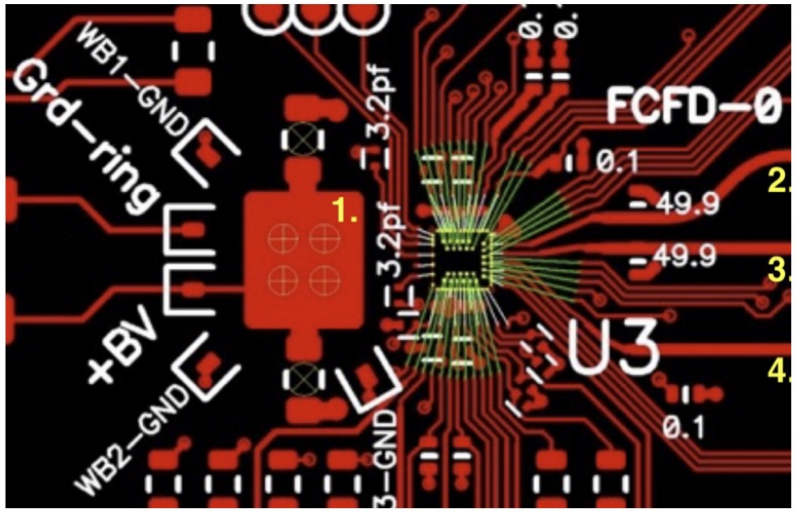
FCDF Chip Prototype v0

- First prototype designed and fabricated in 2021 & tested in 2022



Schematic Diagram



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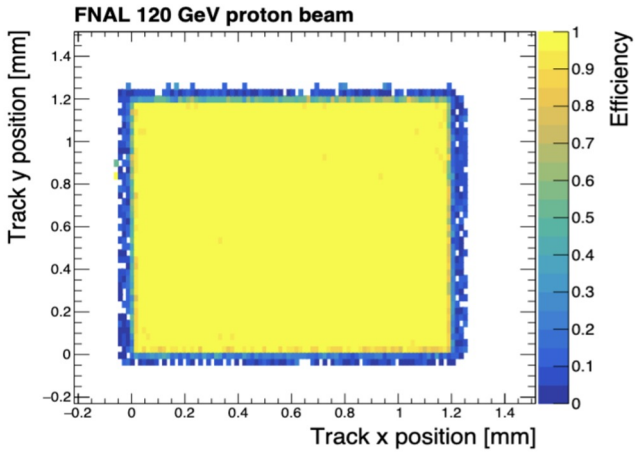
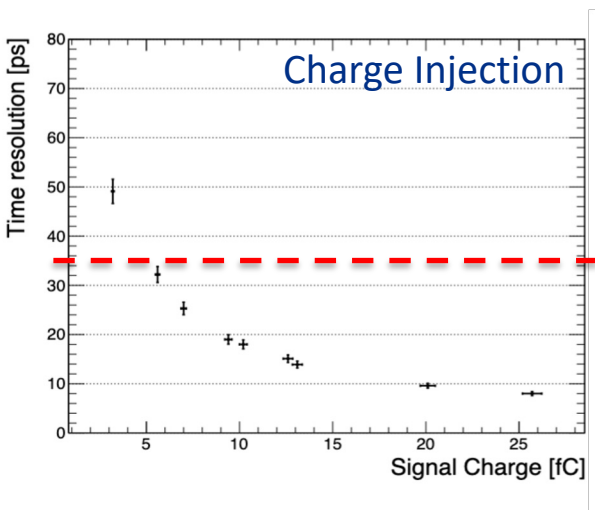
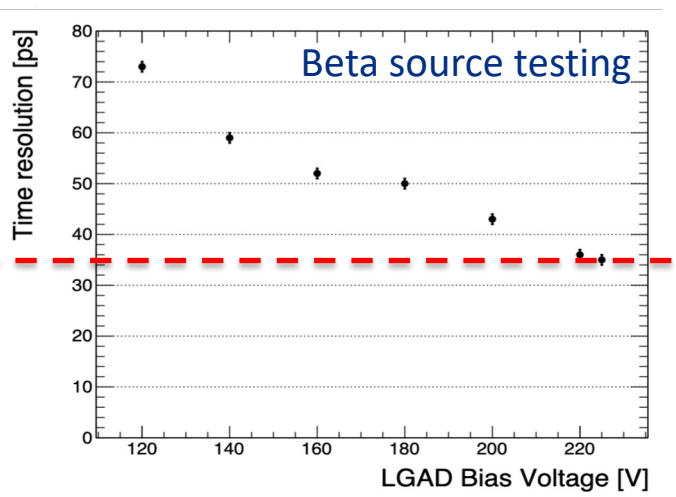
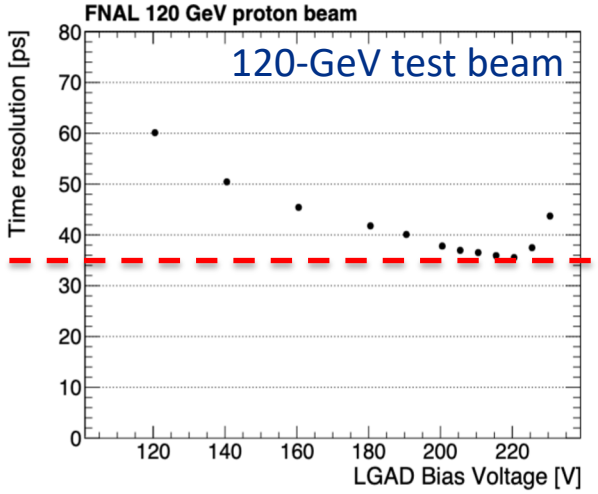
Multi-Source Signal Testing Setup

- FCFDv0 performance evaluated using multiple types of signals:
  - Charge-injected signal
  - Picosecond Laser signal
  - Radioactive Source signal
  - Proton Beam signal





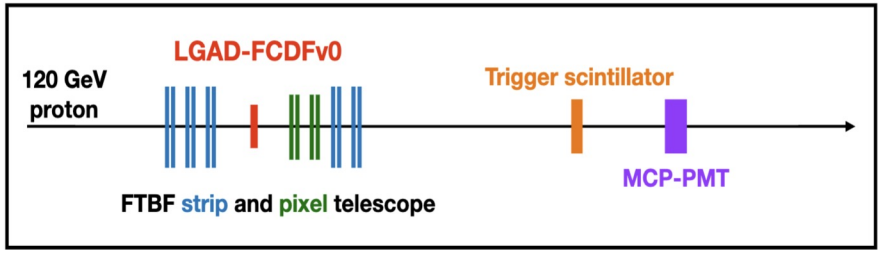


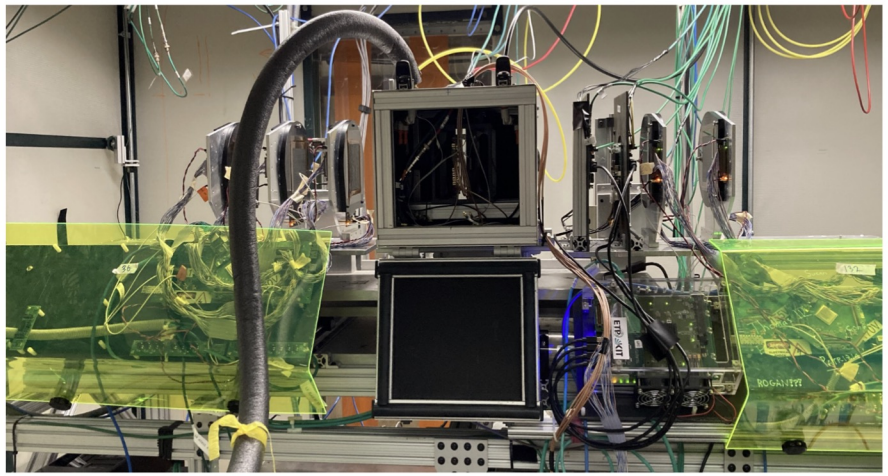


Proton Beam Measurements

- Use Fermilab Testbeam Facility to test CFD chip with 120 GeV protons

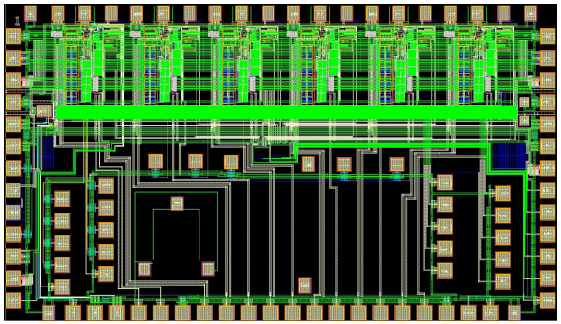
- MCP-PMT used as time reference detector
- Temperature maintained at 20C
- Tracking telescope used to measure hit positions and efficiency





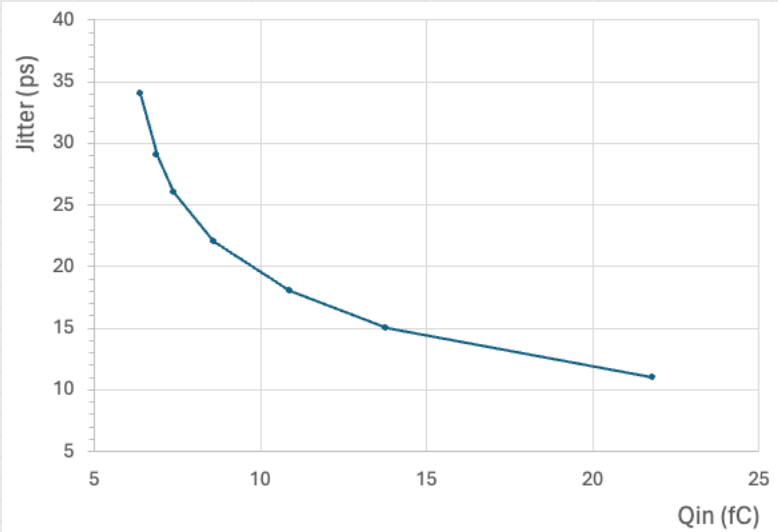
FCFDv1 developments

- Six-channel FCFDv1 submitted Sep. 2023
  - Wider dynamic range,
  - Sensitivity to smaller signals
  - Includes signal amplitude measurement for position measurement
- Specifications presented and discussed in eRD112 regular meetings
- Received the chip back from TSMC in Jan 2024
  - Testing on bench started immediately
  - Started preparations for test beam in Spring 2024



FCFDv1 initial testing

- FCFDv1 bench-top testing
  - Measurements with internal charge injections performed with an LGAD-like signal being injected.
  - With input capacitance ~3.5 pF we achieve around 11 ps time resolution
  - The analog output works linearly over the range of input charge from 7 fC to 60 fC, the discriminator flip time output stays constant within around 10 pS

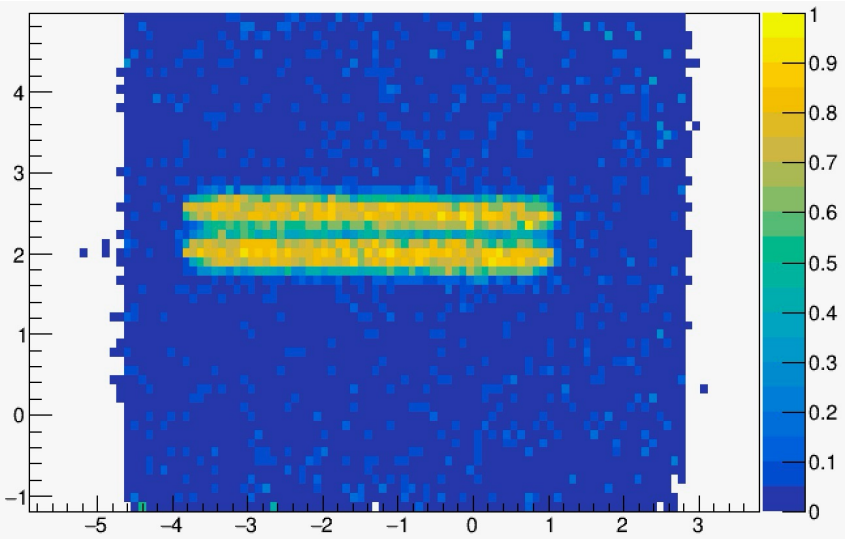


Jitter measurements with 3.5 pf input capacitance and charge injection

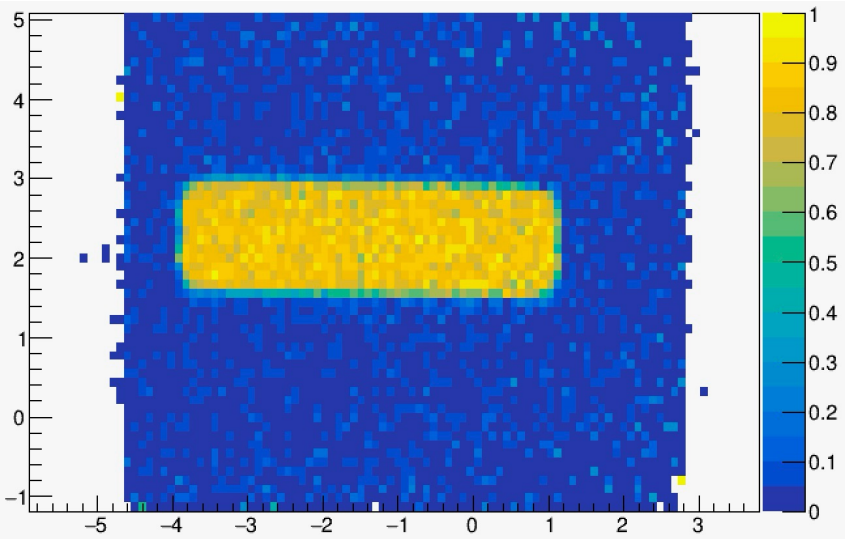
- Our measurements of the AC-LGAD strip sensors showed the complex CR-network which complicates operation of the ASIC
  - Additionally, the capacitance for some of the sensors is a lot larger than we originally specified
  - Hamamatsu 5 mm E-type strip sensors behaved the best, and we adapted the readout board for this sensor

FCFDv1 test beam in May

- Testing in the Fermilab beam in May 2024
  - Connected to a 5 mm strip AC-LGAD sensor, 500 µm pitch, 50 µm thick
- Optimizing the readout board grounding, power supplies, noise
  - Two-strip efficiency demonstrated to be 100%
  - The noise was observed to be too high, causing the comparator to fire too frequently, causing *fake hits*



Efficiency with 2-strips read out separately



Combined two-strip efficiency

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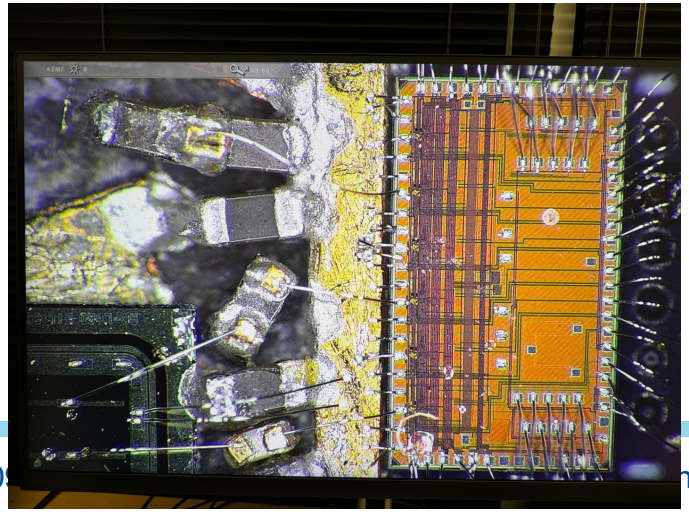
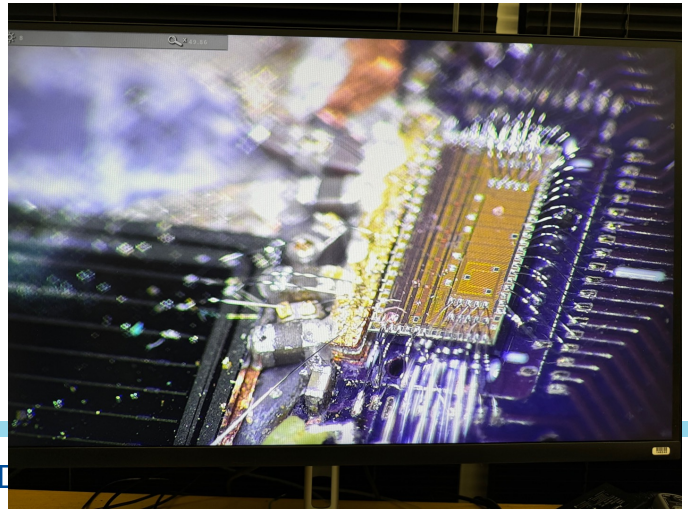
FCFDv1 test beam in June

- Modified the board for test beam in June
  - Mounted on a specially designed low-noise readout board, improved layout and optimized components
  - Added a 7-pF capacitor in series to the AC-LGAD sensor, to reduce the noise and avoid fake hits, and reduce input capacitance
    - Fake hits are reduced, at the cost of **~1/2 of signal size** to the chip input
- Mounted a DC-LGAD with 2 pixels (1.3x1.3 mm^2) connected
  - The DC-LGAD sensors would allow to test and characterize the performance of the chip, without the RC-network effects





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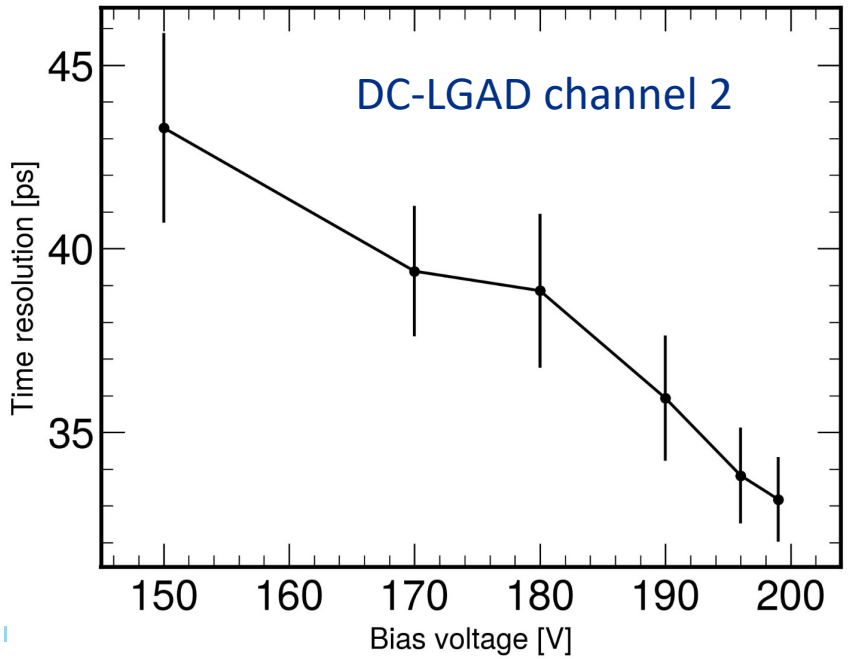
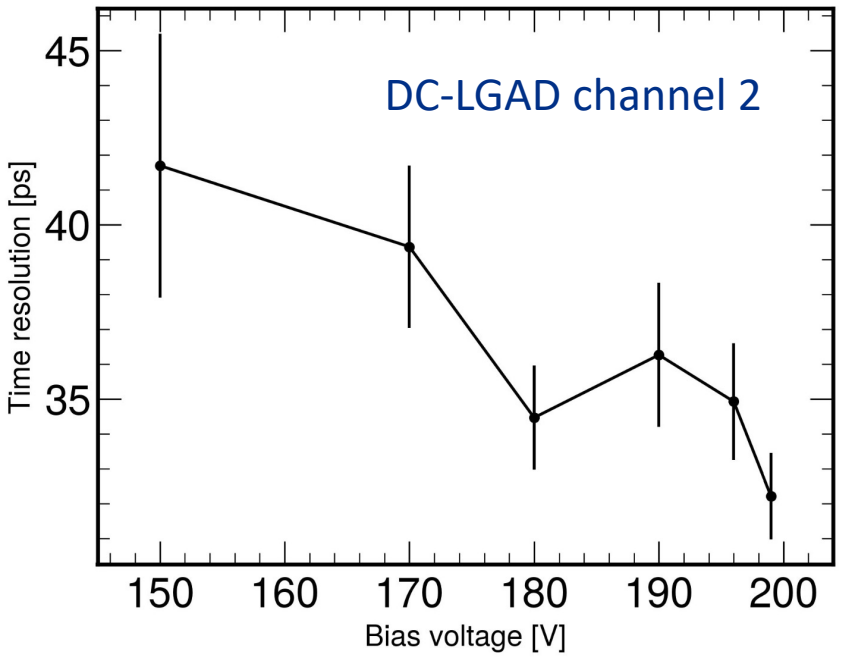
FCFDv1 test beam in June: DC-LGAD results

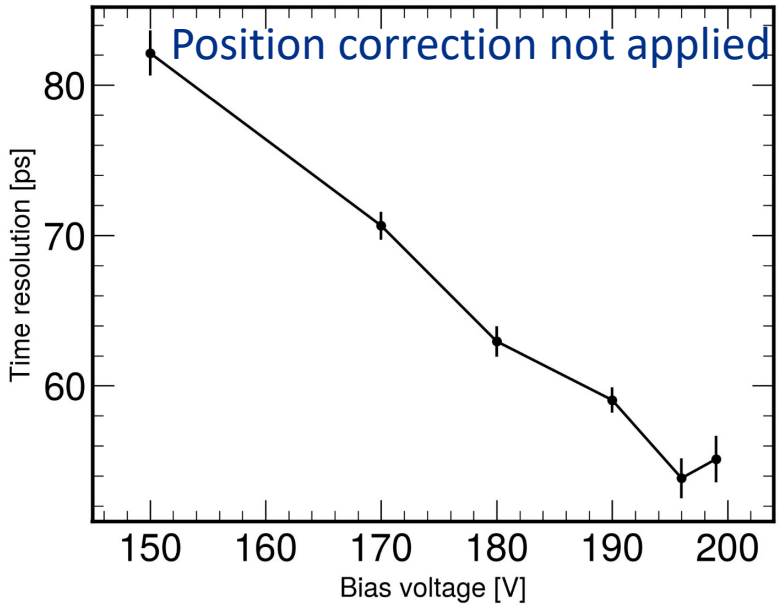
- Performed bias scan BV = 150V, 170V, 180V, 190V, 196V and 199V (breakdown above 200 V)
- Achieve time resolution around 32 ps
  - No time-walk observed, no time-walk correction applied
  - Signal amplitudes around 300 mV
  - Chip performs well for sensors with expected characteristics

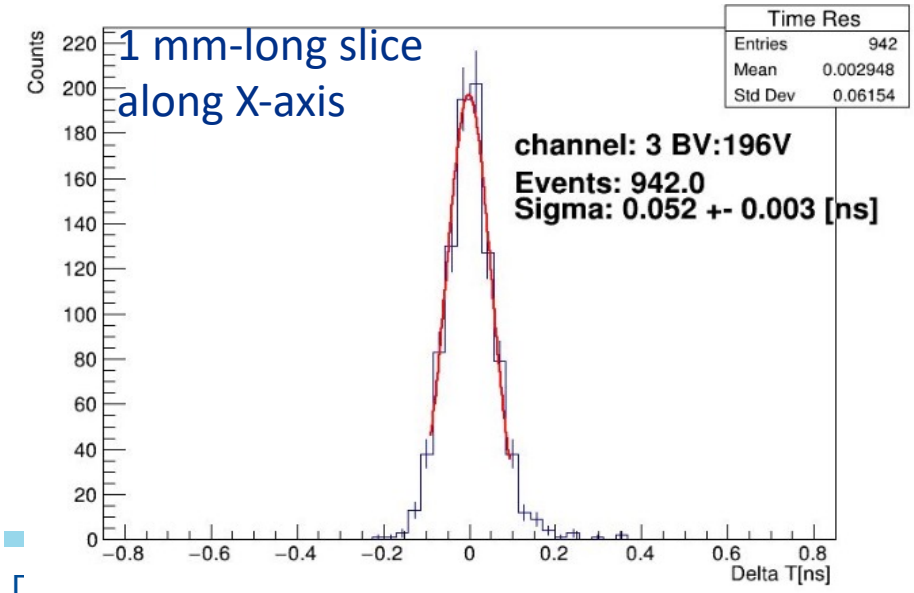




FCFDv1 test beam in June: AC-LGAD results

- Time resolution on the AC-LGAD channel achieves around 55 ps
  - Due to series capacitor, MPV signal size of strip **reduced by more than half:** ~130 mV (AC-LGAD) compared to 300 mV (DC-LGAD)
  - Time resolution for the whole strip **55 ps** (without correcting for position)
  - Time resolution in 1mm slices along strip: **52 ps** (will implement correction)
- σ_T for DC-LGADs with 130 mV signals ~ 50 ps
  - Indicates that AC-LGAD should get σ_T ~35 ps with improved comparator





Development plans in 2024 and 2025

- Finalize testing of FCFDv1
  - Test with IR-laser to study the effect of increased signal from AC-LGADs on time resolution
  - Re-optimize the chip with the final-spec AC-LGAD parameters as tested with FCFDv1 version, for a minor revision FCFDv1.1
- Next focus on the full chip: full-size FCFD v2 end of 2025
  - Finalize the geometry and sensor key parameters (strip length, sheet resistance and thickness)
  - Complete ASIC with readout that would interface with the EIC experimental DAQ
  - Implement the interfaces with RDO
- The final ASIC (v3) to be produced end of 2026

Summary

- Presented motivation, design, and results of the Fermilab CFD v0 and v1 chips
  - Measured performance of v1 chip with AC-LGAD sensors in beam showed unexpected large noise and larger than expected capacitance
- Performed detailed testing and characterization of the setup to understand strategies to achieve required performance
  - Demonstrated that FCFDv1performs well for signal sizes expected from AC-LGAD
  - Aim to submit a minor revision with fixes and confirm performance with particles
- In parallel, start design of the full chip with full system specs