EICROC0 update

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On behalf of Omega, IJCLab and CEA IRFU

Organization for Micro-Electronics desiGn and Applications

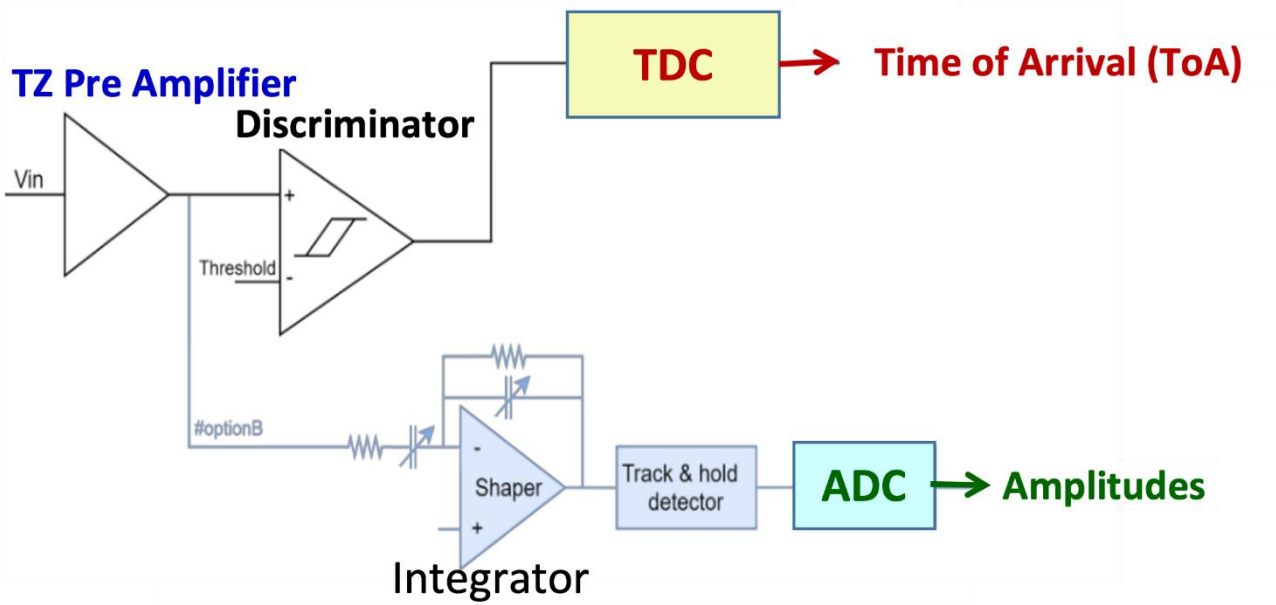
Summary

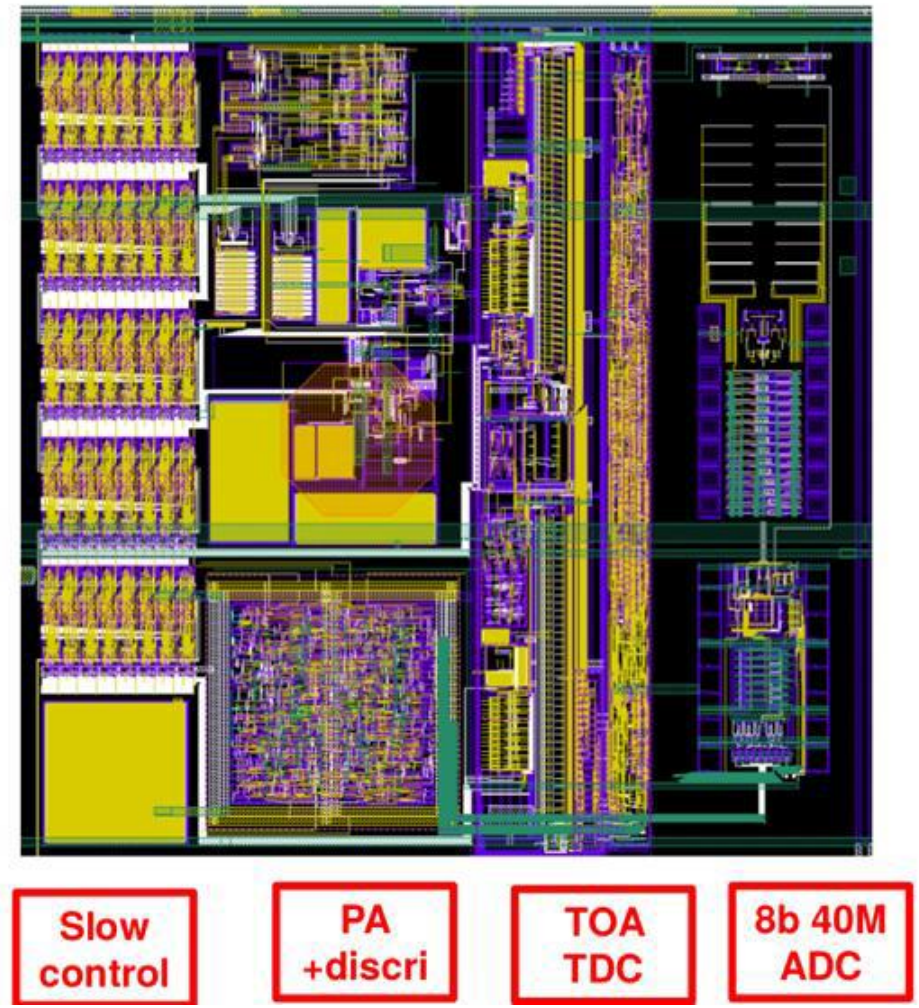
1. ASIC Presentation
2. Test setup and environment
3. Measurement results
4. ASICs status and perspectives

EICROC : Overview

EICROC : an AC-LGAD read-out ASIC

- First prototype **EICROC0** to test performance with and without a sensor
  - 4x4 pixels / ASIC
  - ~2mW/channel + 4*20mW « analog probe preamp »
  - Slow path for charge measurements (8b SAR ADC)
  - Fast path for time measurements (10b TDC from IRFU)



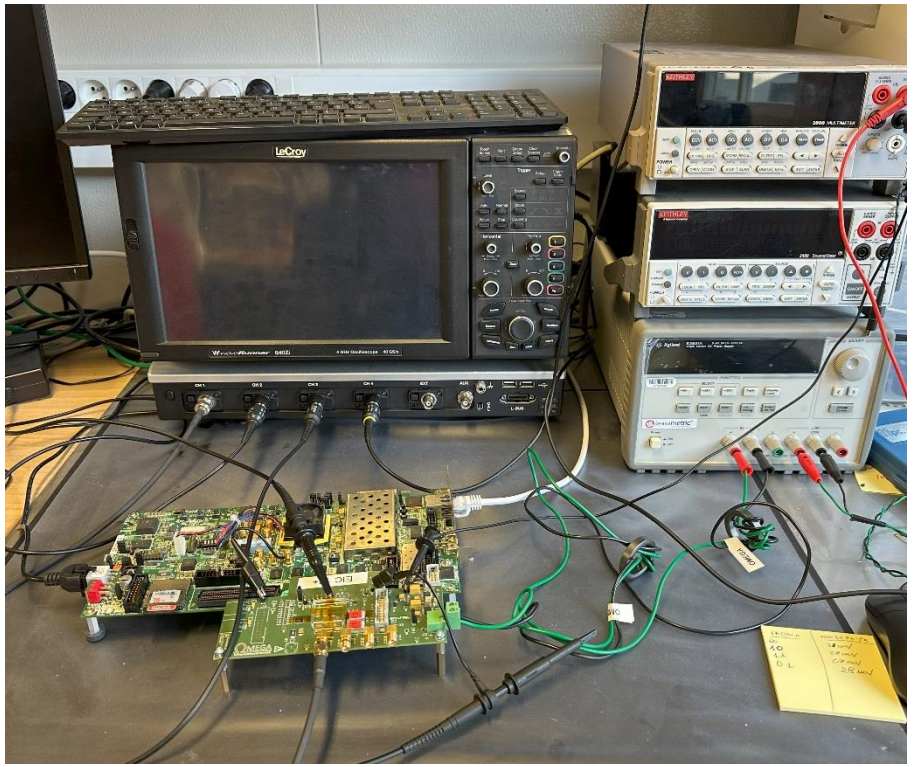


EICROC0 Layout

Test setup : EICROC0 cards

- "Classical" test setup with FPGA + EICROC0 PCBs
- 2 flavors of cards used
  - EICROC0 2.2 (ASIC with no sensor)
  - EICROC0 2.3B (ASIC with sensor)
  - Both cards are from the latest batches of PCBs

- Latest firmware (with 160MHz clock fix @ end of June)
- EICROC0 2.2 plots shown for correction values @ 5 fC
  - c_D = 11 (additional 750 fF @ preamp input), c_P = 1
- EICROC0 2.3B plots shown for correction values @ 10 fC
  - Sensor is depleted (-100 V, 1 µA)
  - c_D = 00 (no additional capacitance @ preamp input), c_P = 1



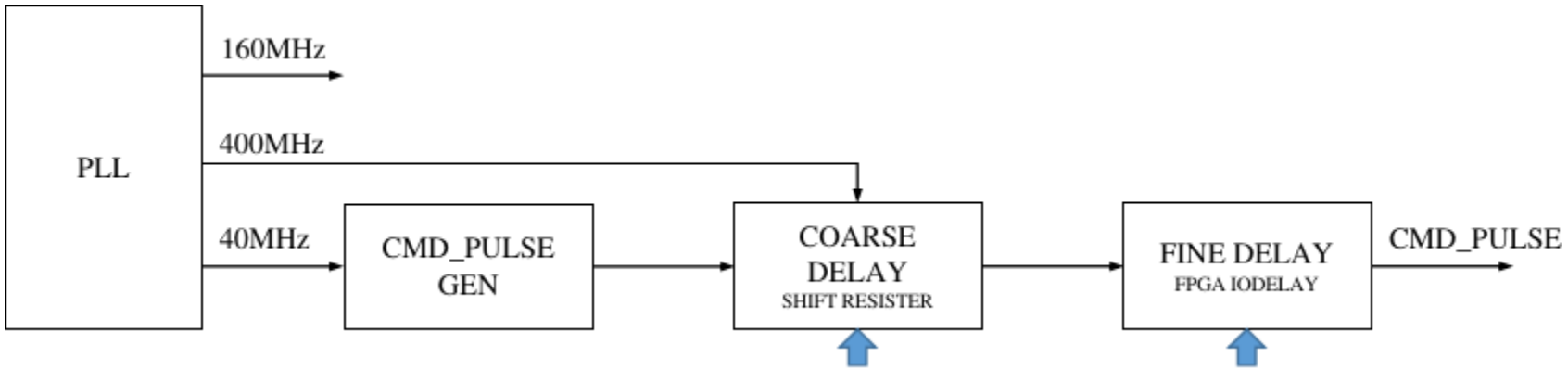
Test setup @ Omega

EICROC FPGA Clock synthesis issue

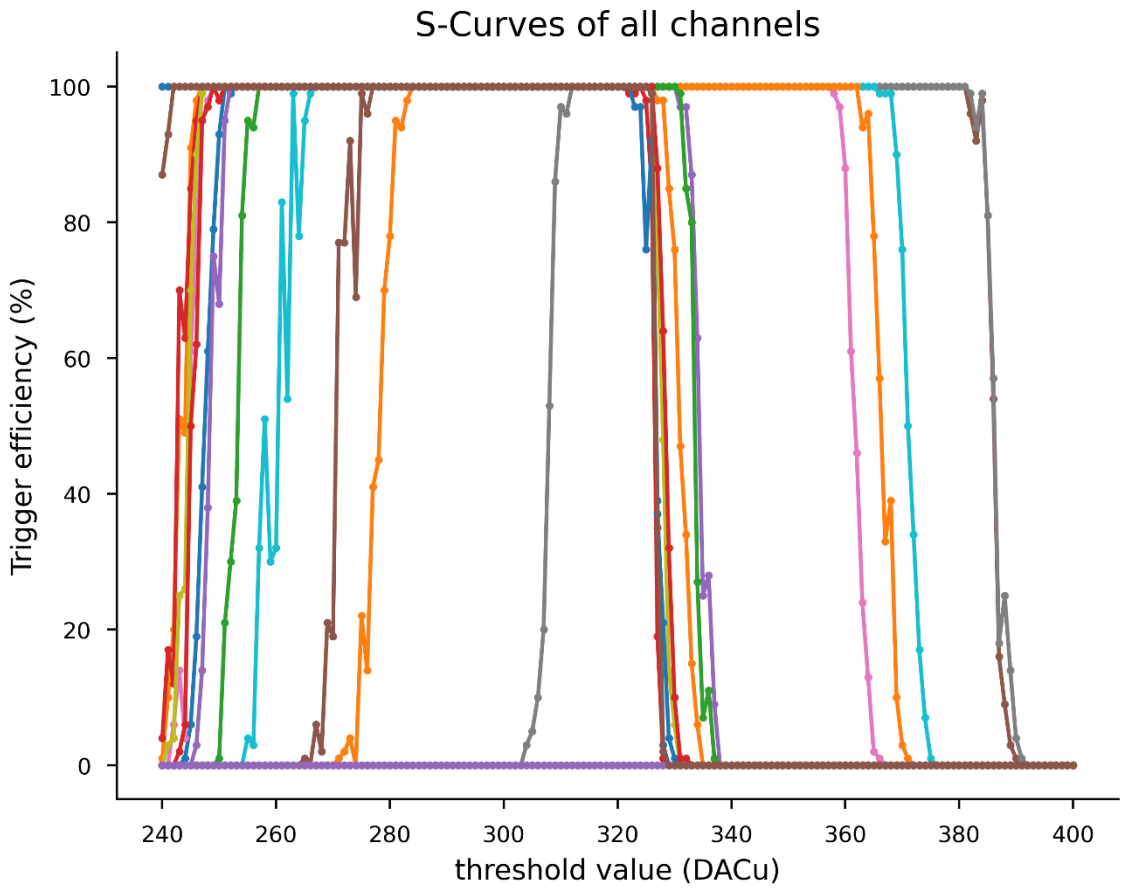
The EICROC chip receives a 160MHz clock from the FPGA (gets converted to a 40MHz internally)

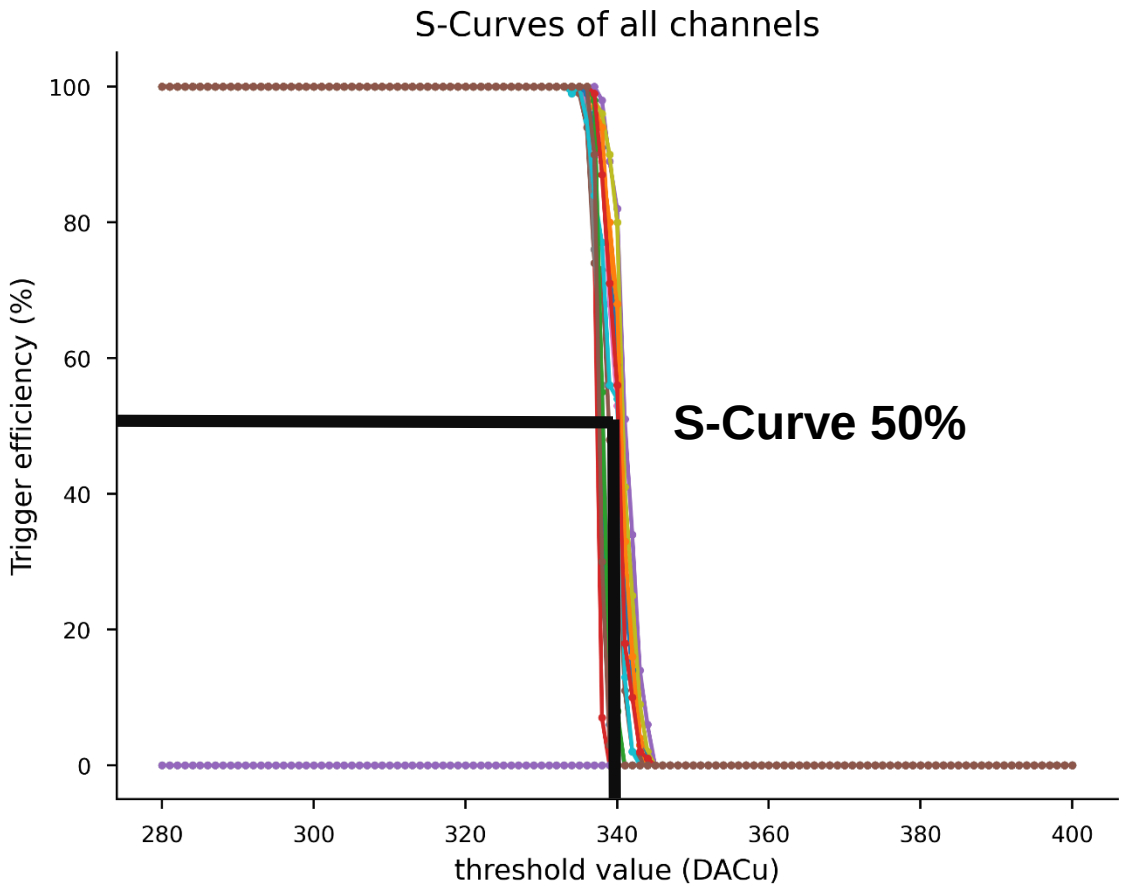
An issue with optional clock delay blocks on the FPGA added **significant** jitter to the clock, which disturbed all measurements.

The issue was fixed in June 2024, and the test results are now presented with the updated / fixed firmware.



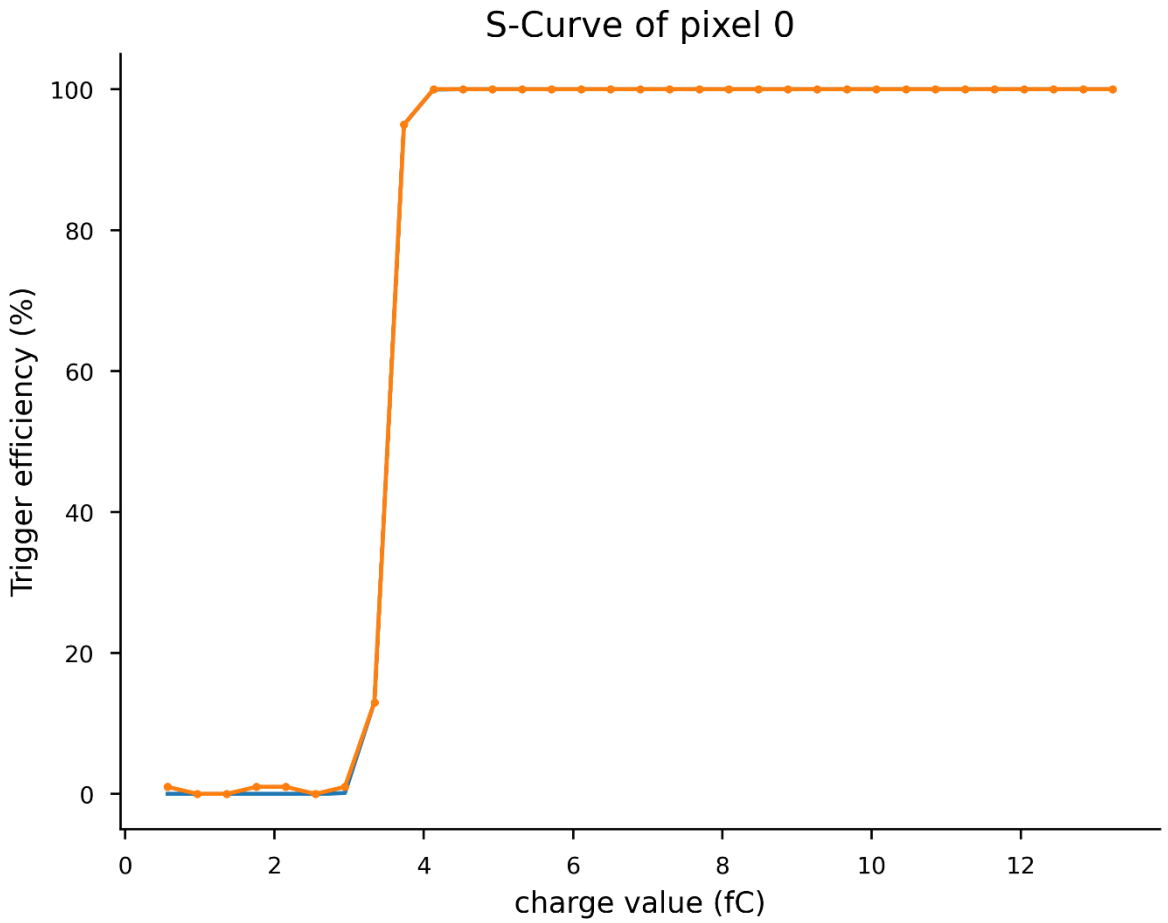
S-Curve correction



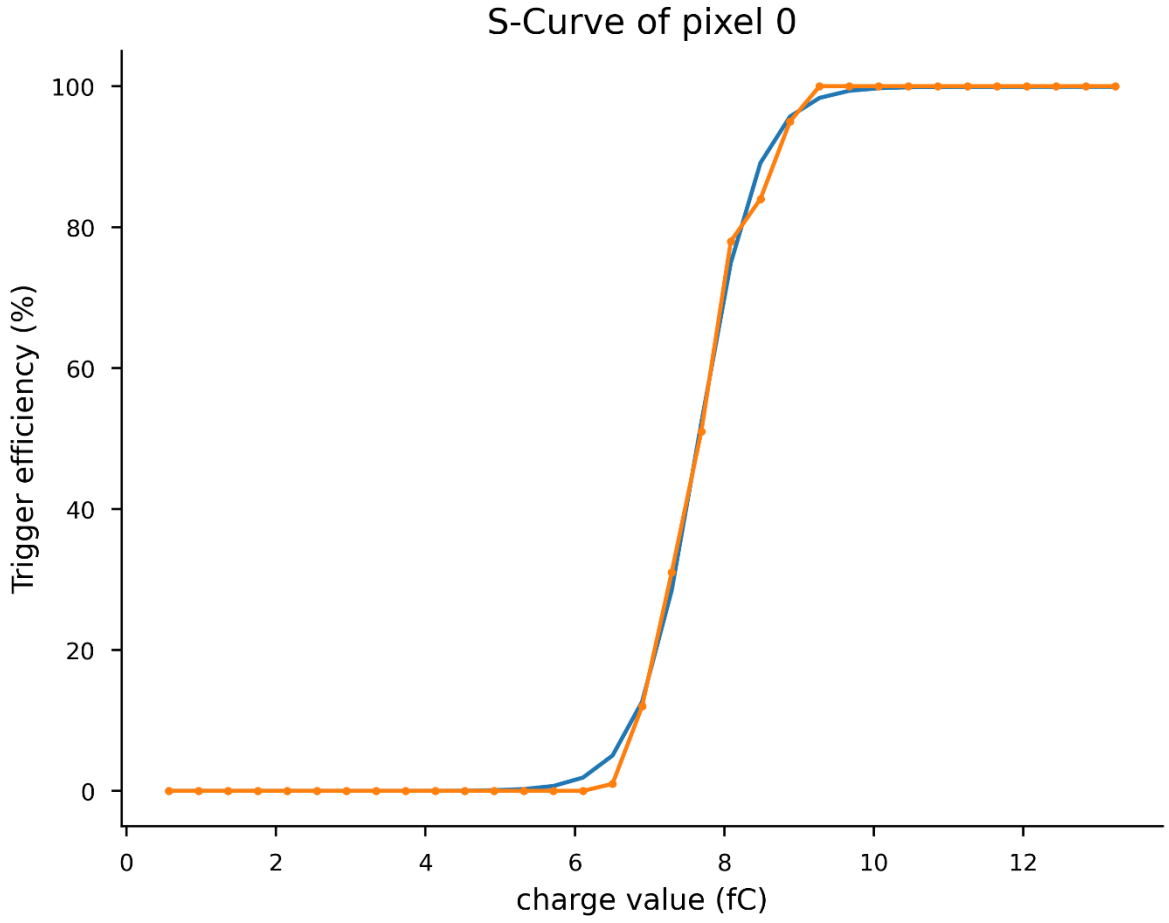


S-Curve correction with individual pixel correction DACs
(plots of card with sensor, correction @ 5 fC)

Minimum charge detected for channel 0

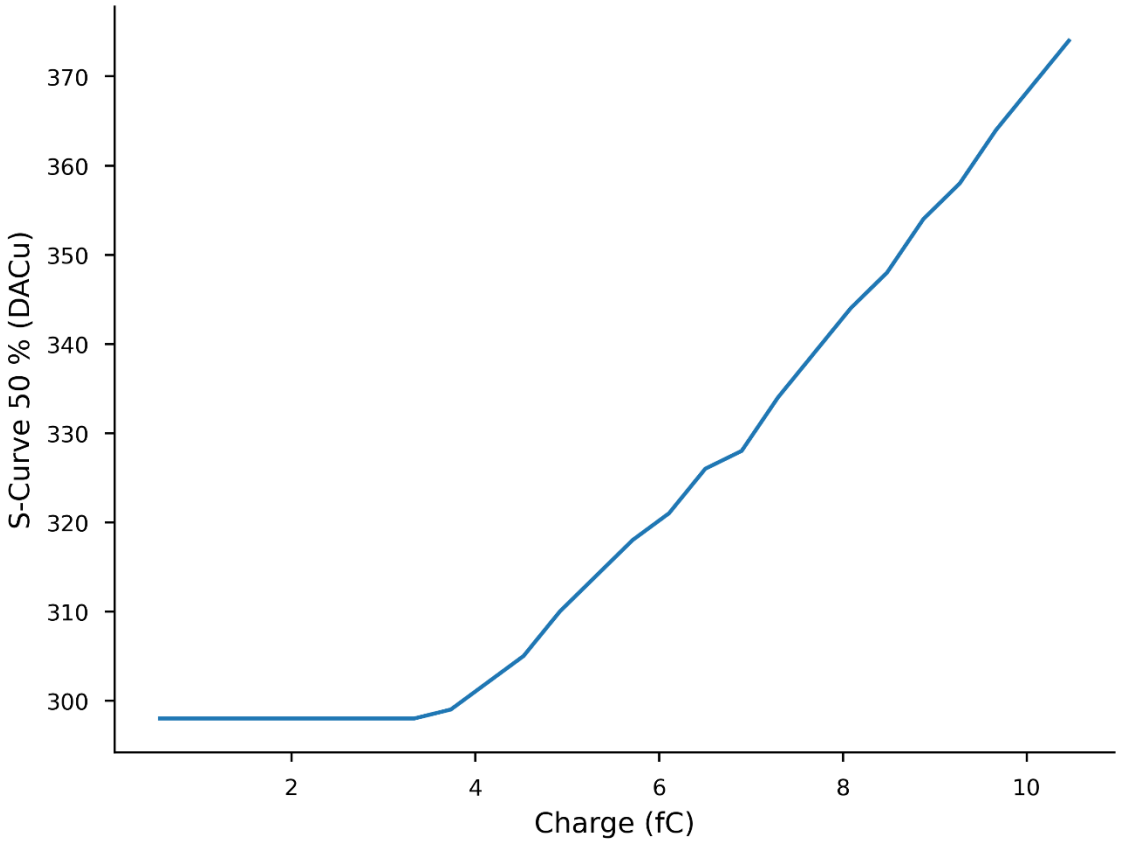


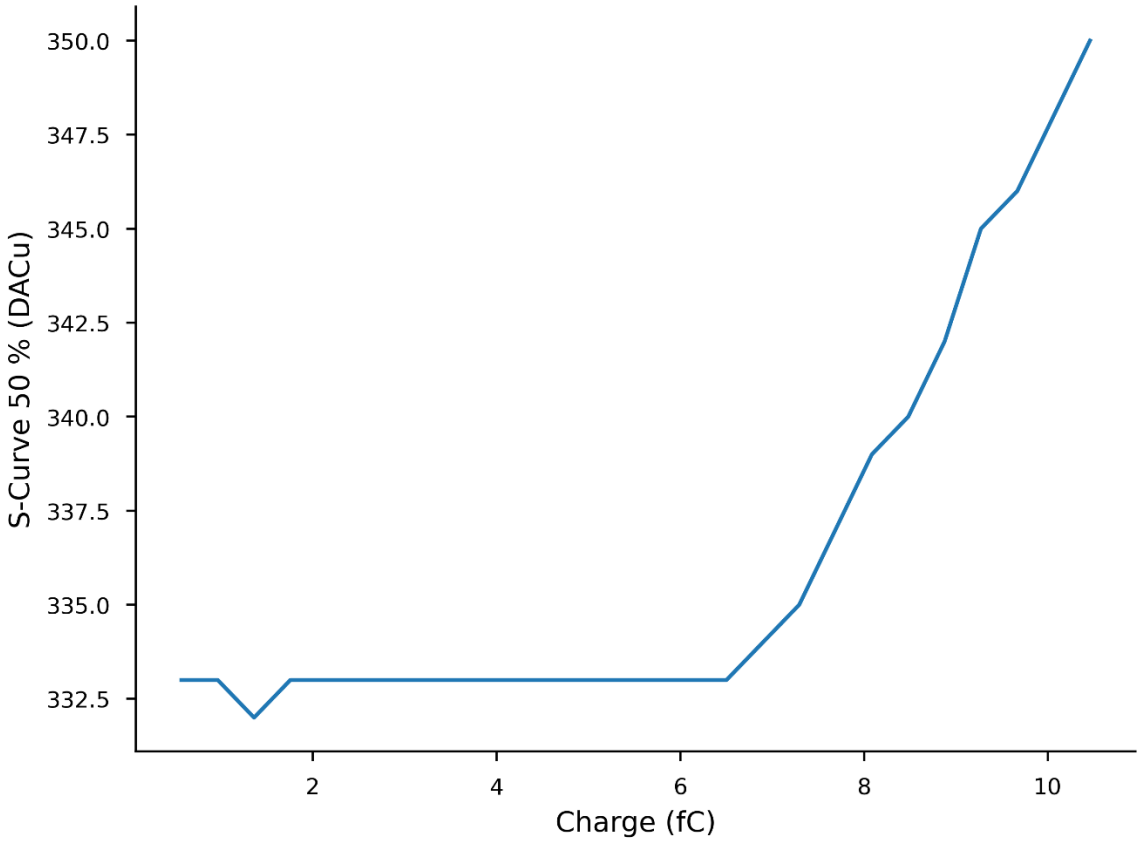
Without Sensor : 3.5 fC
Noise = 0.25 fC
Threshold = 300 DACu



With Sensor : 7.65 fC
Noise = 0.66 fC
Threshold = 340 DACu

S-Curve 50% vs charge for channel 0

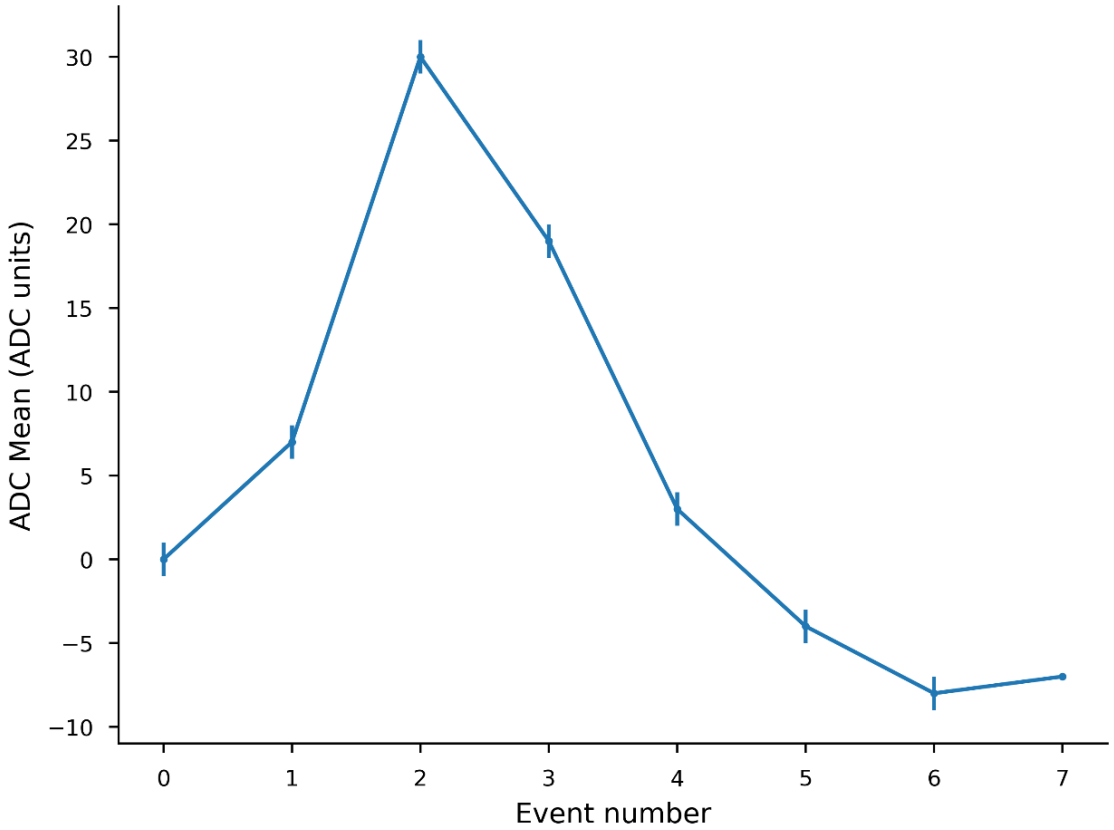




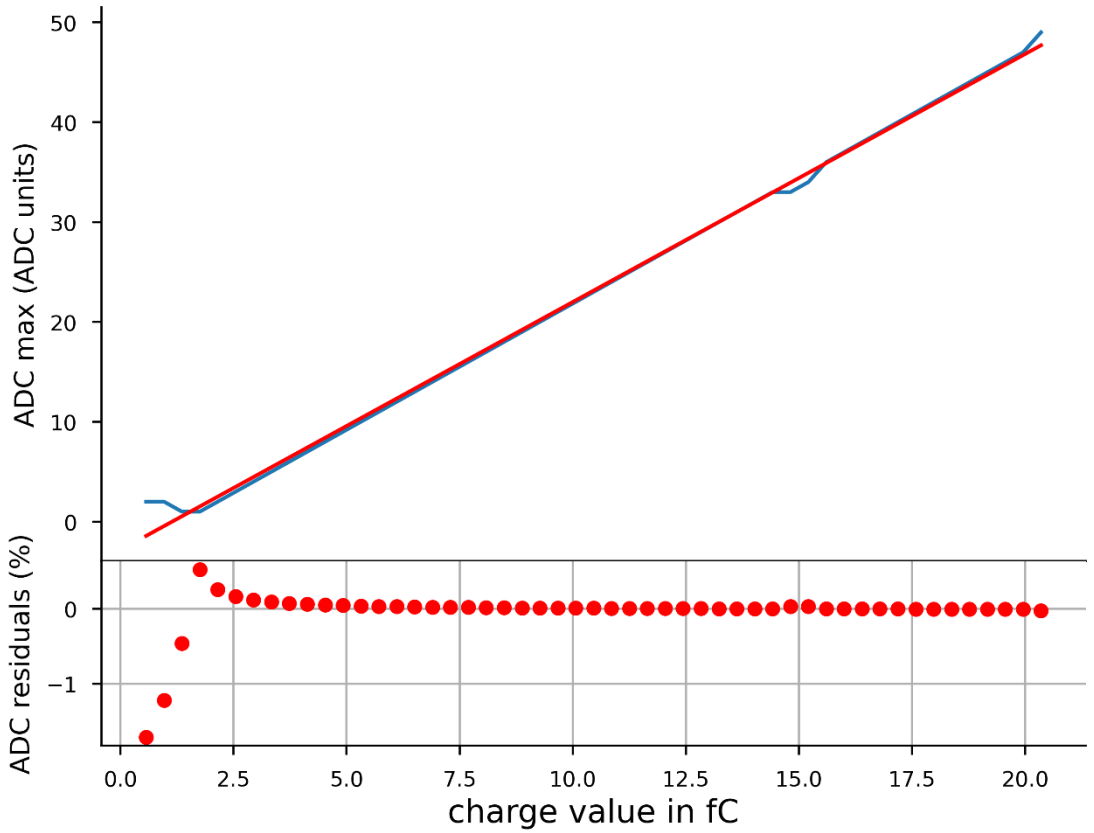
Without Sensor

With Sensor

ADC : Channel 0 – ASIC with sensor

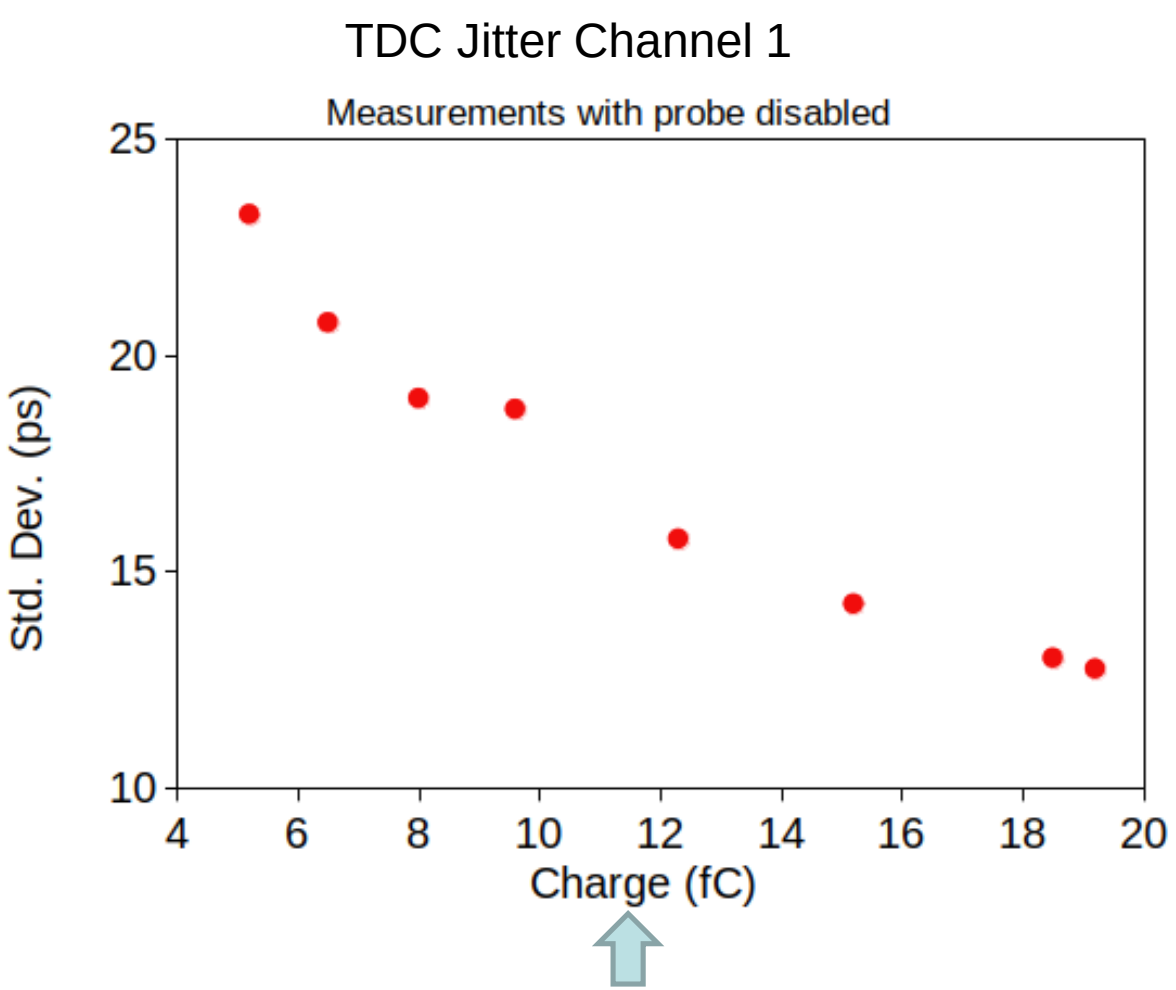


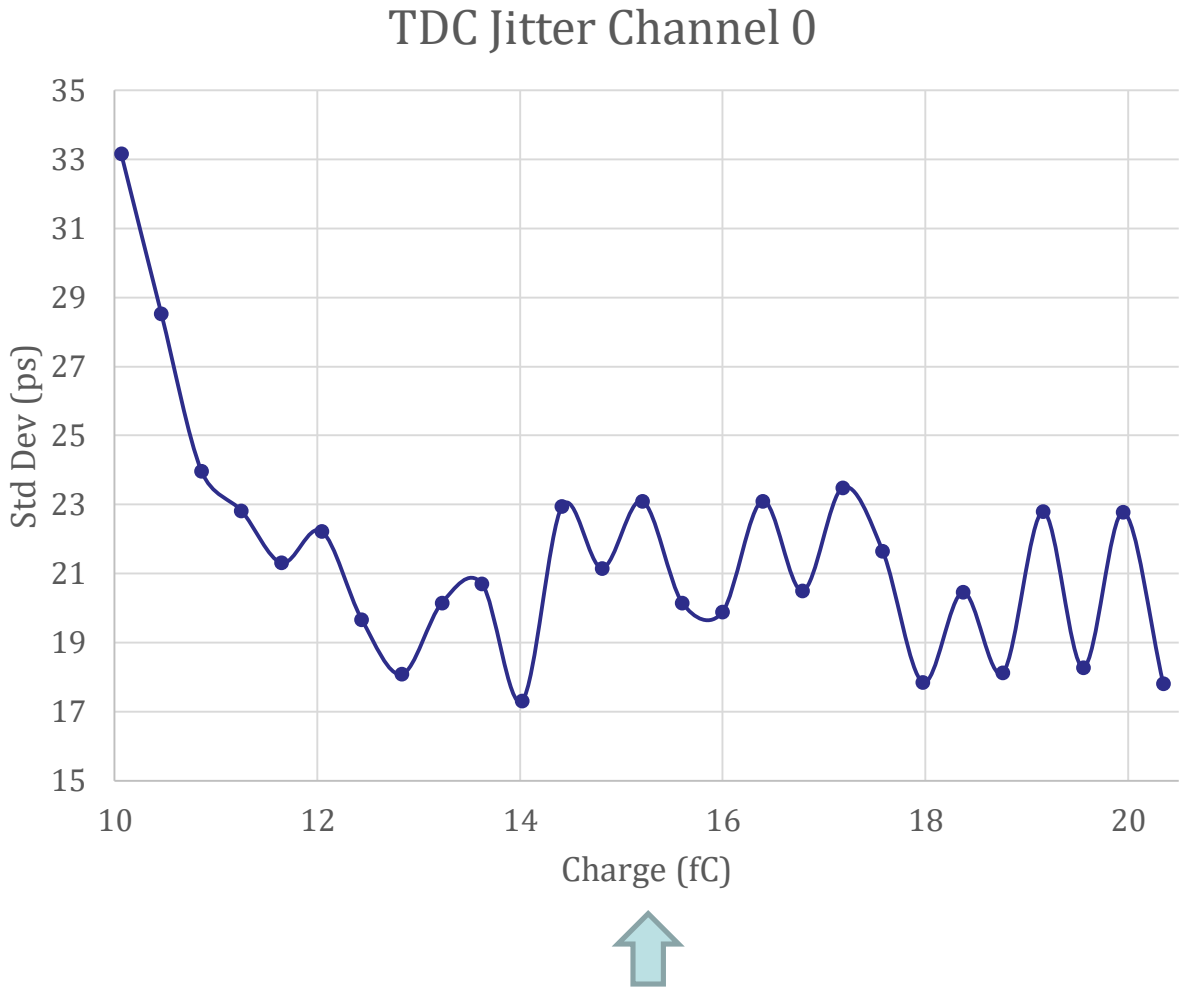
ADC Pulse reconstruction
(obtained with correction)



ADC max vs charge sweep

TDC Jitter





Without Sensor
Jitter ~17 ps @ 10 fC
~12.5 ps @ 20 fC
Threshold = 135 DACu

With Sensor
Jitter ~33 ps @ 10 fC
~20 ps @ 20 fC
Threshold = 340 DACu

EICROC0 measurement summary

Measurement	ASIC Without Sensor	ASIC With Sensor
Min. detected charge	3.5 fC	7.65 fC
Noise value	0.26 fC	0.66 fC
TDC Jitter @ 10 fC	17.5 ps	33 ps
TDC Jitter @ 20 fC	12.5 ps	20 ps

Next measurement steps :

- Full characterization of a few ASICs (with and without sensors, bump bonded sensors, flip chip…)
- TDC non linearity calibration/correction
- Cross talk measurements (with ADC, S-Curves or probe signals)
- Beta source & laser measurements (BNL, IJCLab)
- Test beam within the "AC-LGAD" working group (spring 2025?)

EICROC ASICs : Status & perspectives

- EICROC0 is a testbeam prototype => sensor characterization
  - Present power ~2 mW/ch + 4*20 mW « analog probe preamp »
  - ADC power + shaper/driver to be reduced from ~1 mW to 100 µW/ch => EICROC0A
  - Submission @ end of 2024

- EICROC1 will address larger dimensions 4x16 or 8x16 or 4x32 or 8x32
  - Address floor planning and power distribution
  - Option for selective readout : hit + 8 neighbouring channels
  - Status : layout started based on EICROC0, adding more testability
  - Still EICROC0-like readout
  - Submission @ end of 2024

- EICROC2 final size : 32x32