ePIC-TOF Frontend Electronics

Wei Li (Rice University) for the WP2

TOF and AC-LGADs Workfest@ePIC collaboration meeting
July 26, 2024

Electron-Ion Collider

BROOKHAVEN NATIONAL LABORATORY | Jefferson Lab | U.S. DEPARTMENT OF ENERGY | Office of Science

New TOF DSC ORG

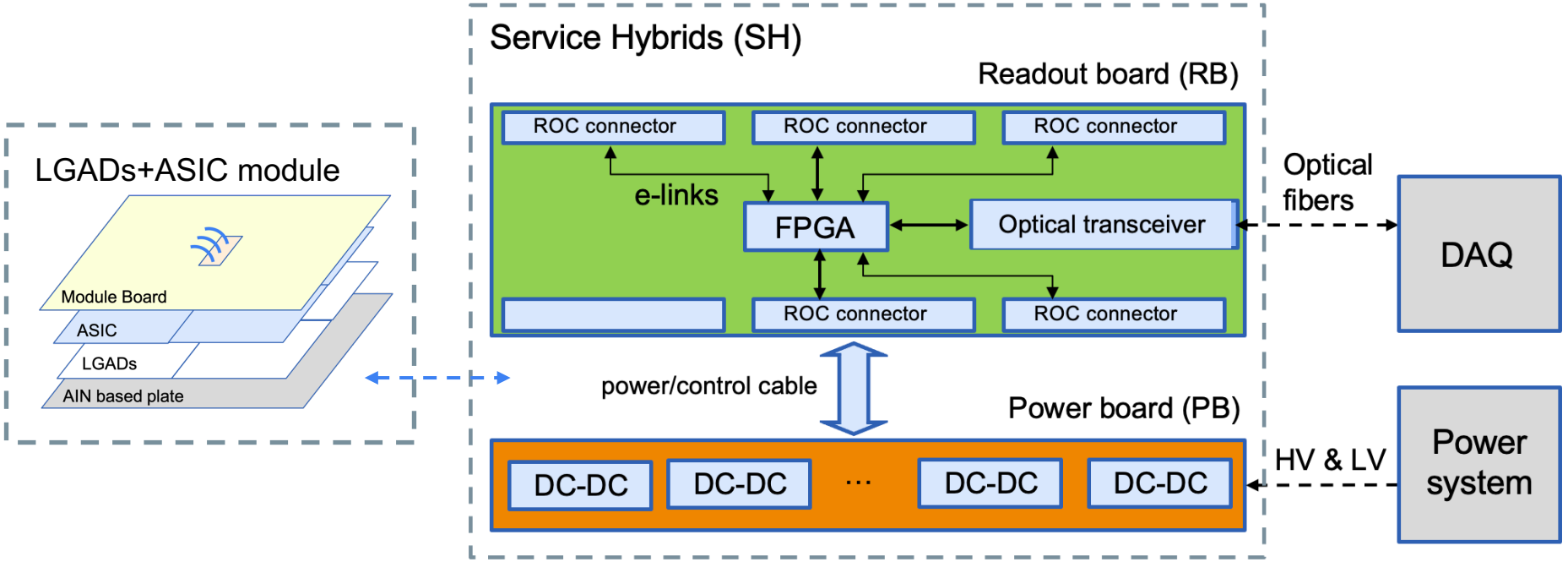
Position	Candidate(s)
1 Detector Subsystem Leader	Zhangbu Xu
1 Deputy DSL	Satoshi Yano
2 Detector Subsystem Tech. Coordinators	Mathieu Benoit, Matthew Gignac

- **Leadership Structure**
- **Work packages combining BTOF and FTOF**
  1. Sensors (2 coordinators)
     Simone Mazza, Japanese colleague
  2. Frontend Electronics (all electronics that are on the detector) (2 coordinators)
     Wei Li, TBD
  3. Module local integration and assembly (2 coordinators)
     Mathieu/Matthew, Asian colleague
  4. System tests and validation (2 coordinators)
     Prithwish Tribedy (FF Liaison)+Takashi Hachiya
  5. Mechanical structure, cooling and global integration (2 coordinator)
     Andy Jung, Yi Yang
  6. DAQ & Clock distribution (1 coordinator)
     Tonko Ljubicic
  7. Power system, Detector slow control, monitor and safety system (1 coordinator)
     Frank Geurts
  8. Simulations, software & calibration, Database(1 coordinator)
     TBC?

WP2 meets every other Friday at 10am CDT: https://indico.bnl.gov/category/546/

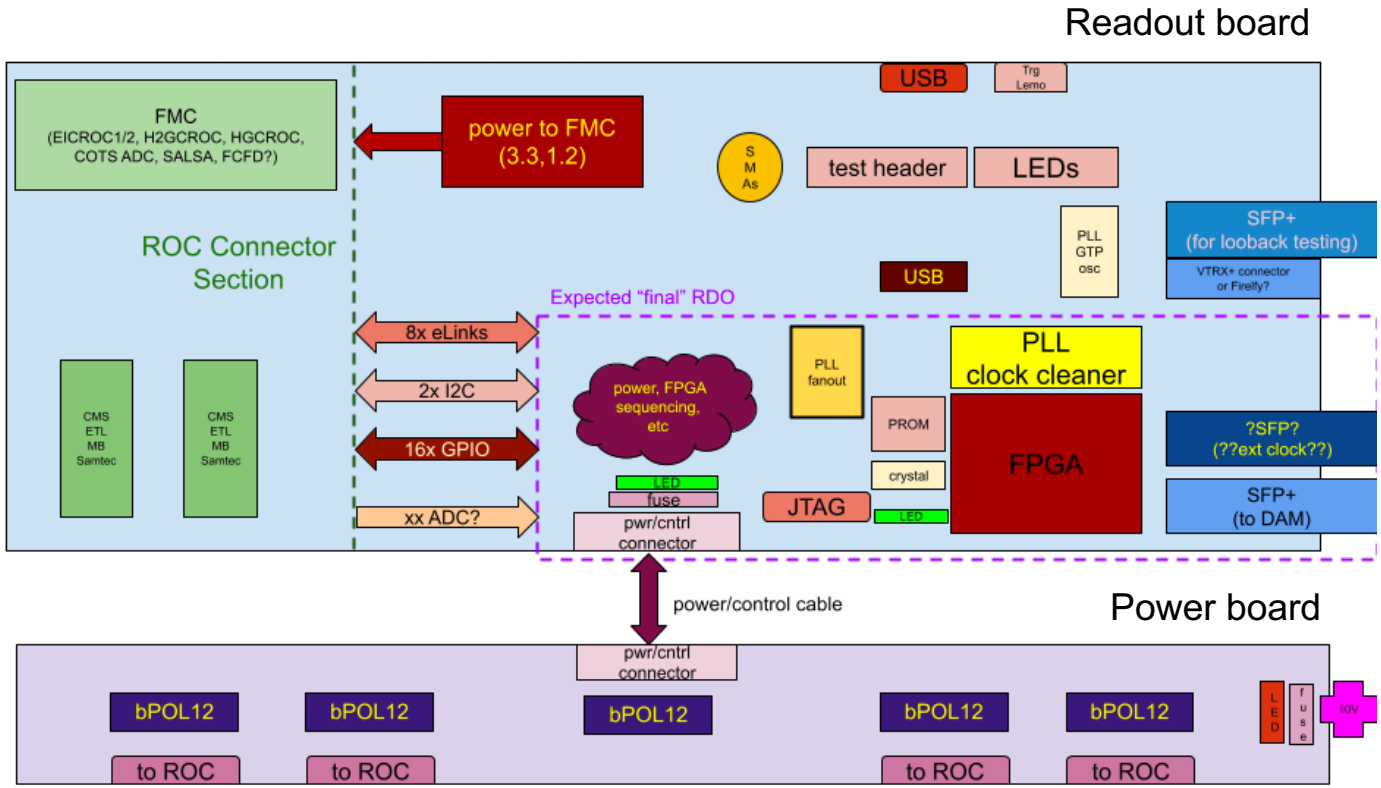
TOF frontend electronics overview

FEE covers all electronics on the detector: **ASICs** and **Service Hybrids (SH)**



See talk by Christophe et. al. for ASIC development

Sketch of first SH pre-prototype schematics



Aims to keep only 1 SFP+ in final RBs

Roadmap and timeline of SH development

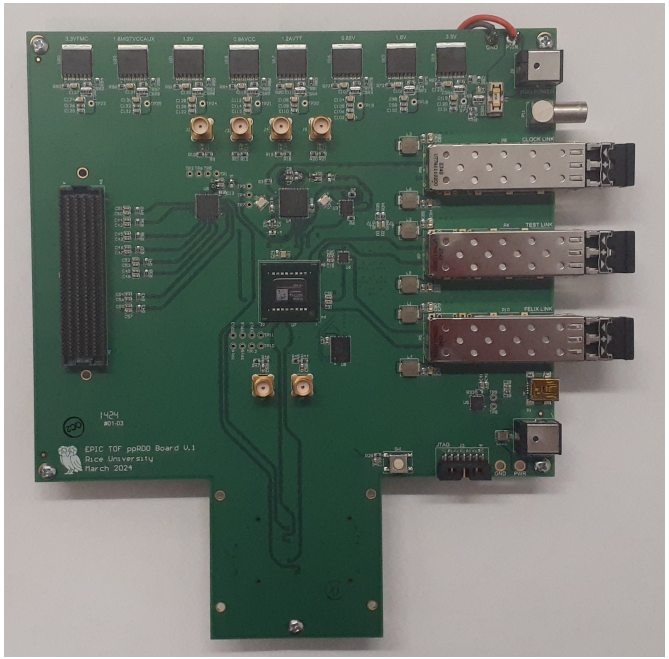
2024: **Prototype v0** (pre-prototype): establish all essential functionalities and readout chain.

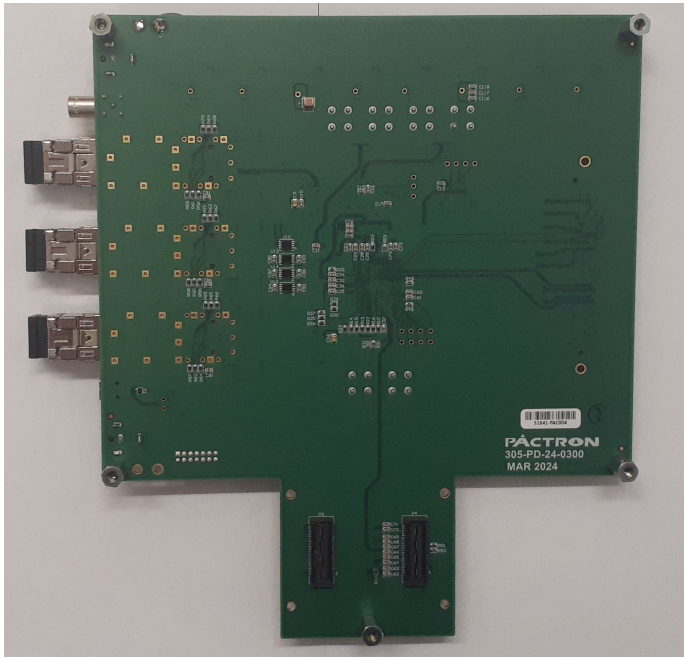
2025: **Prototype v1**: first prototype with realistic dimensions, and meeting requirements/constraints for FTOF and BTOF, and other AC-LGADs subsystems.

2026: **Prototype v2**: final prototype

First pre-prototype readout board v0 (ppRDO)

First ppRDO designed and fabricated (Rice U.)





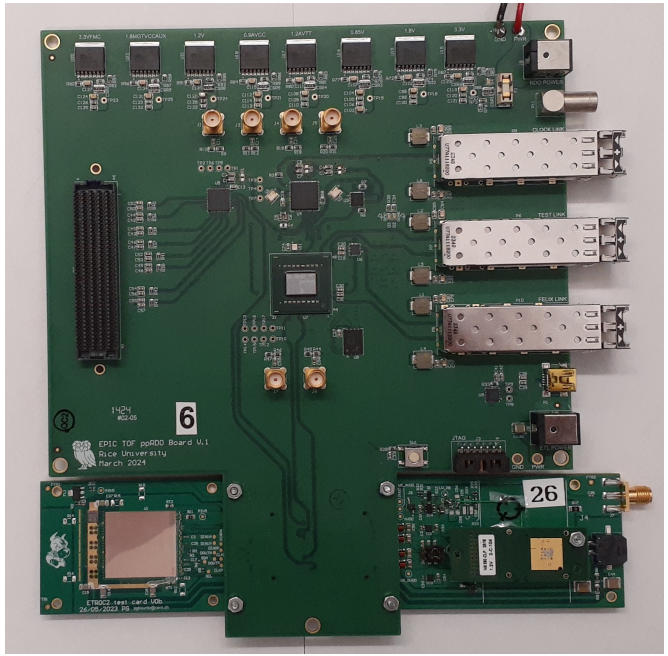
Six boards:

- Board #1: Rice
- Board #2: Zagreb
- Board #3: Rice (→LBNL)
- Board #4: BNL,
- Board #5: CEBAF
- Board #6: Rice, with the ETL Module Board, accessible remotely

Documentation: https://twiki.cern.ch/twiki/bin/view/Main/EpicSH

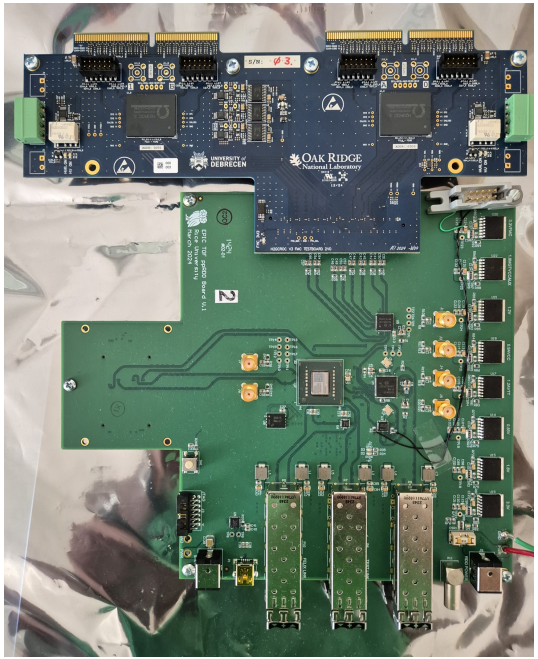
First pre-prototype readout board v0 (ppRDO)

Interface with ETROC module board v0 (CMS)



@Rice

Interface with HGCROC test board



@Zagreb

Documentation: https://twiki.cern.ch/twiki/bin/view/Main/EpicSH

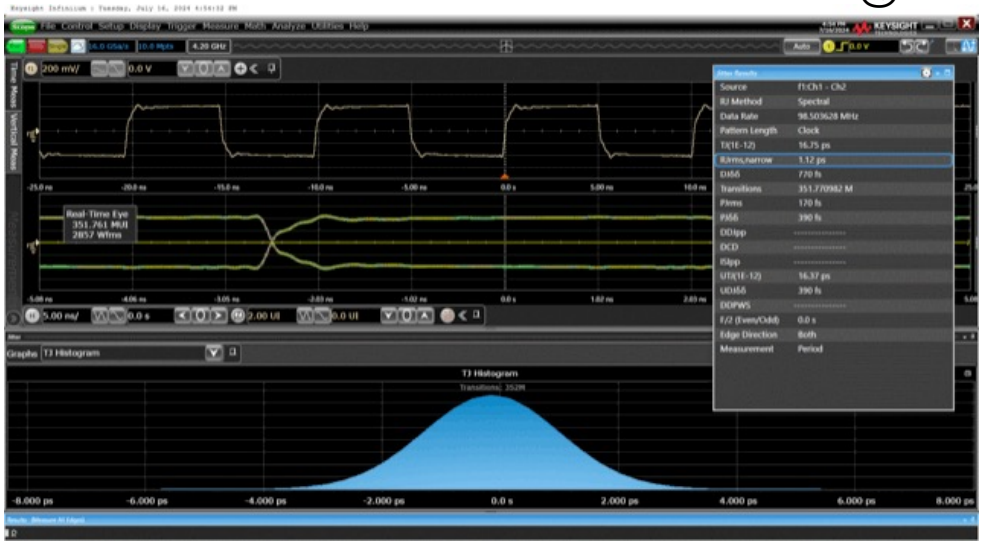
TOF ppRDO testing status and plan

- FPGA firmware being developed – Rice
- Current, voltage and power measurements to proceed, once firmware is available – BNL
- Clock cleaning and recovery measurements ongoing – BNL, JLab
- Integration with ASICs (ETROC, EICROC1) ongoing – LBNL, BNL
- Radiation tests: have to tolerate up to **100 kRad and immune to SEU effects.** An idea of placing it in STAR during the RHIC Run25 being explored (SEU tests). Test procedure and location in controlled environments being investigated.

Clock cleaning and recovery measurements

TOF requires high precision clock jitter: **< 5ps**

@BNL



Preliminary measurements of clock jitter

- **~1.12 ps** out of the clock cleaner with an input 98.5 MHz clock measured with new precision scope at BNL (deterministic jitter ~770 fS).
- Similar efforts and conclusion from measurements at JLab.

More work to follow up:

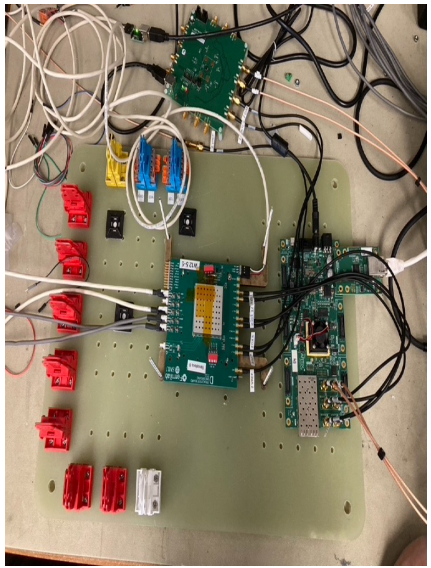
- Jitter measurement with various fiber optic cable lengths underway
- Reconstruct the clock from the FELEX link to remove the SFP+ dedicated for the clock
- Clock distribution and synchronization scheme to be worked out

Integration with ASICs

Firmware to communicate with ETROC2 using FPGA evaluation kit being developed

Once completed, establish communication between ETROC2 with ppRDO. Plan to place 1-2 ETROC2 planes in the test beam.

@LBNL



Roadmap and timeline of SH development

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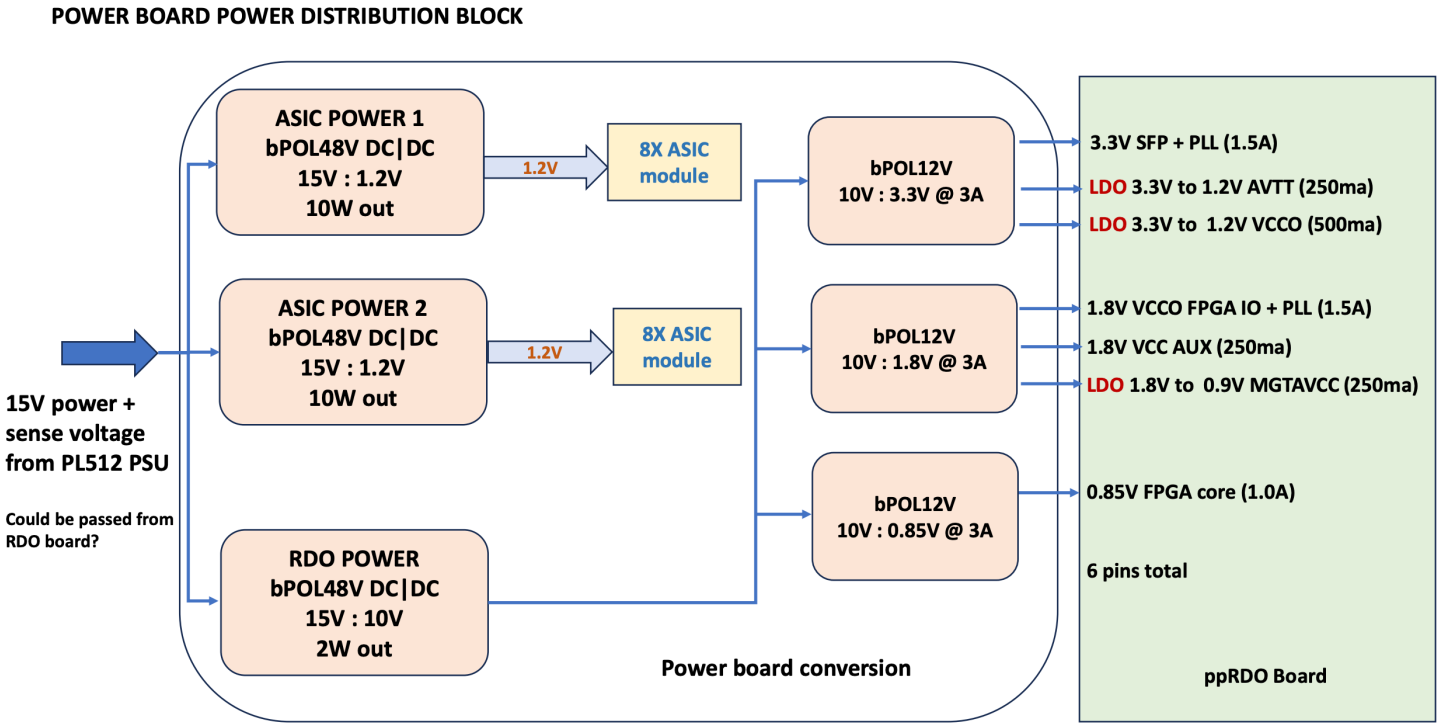
2025: **Prototype v1**: first prototype with realistic dimensions, and meeting requirements/constraints for FTOF and BTOF, and other AC-LGADs subsystems.

- Focusing on FTOF first

2026: **Prototype v2**: final prototype

FTOF Power board prototype v0 (FY25)

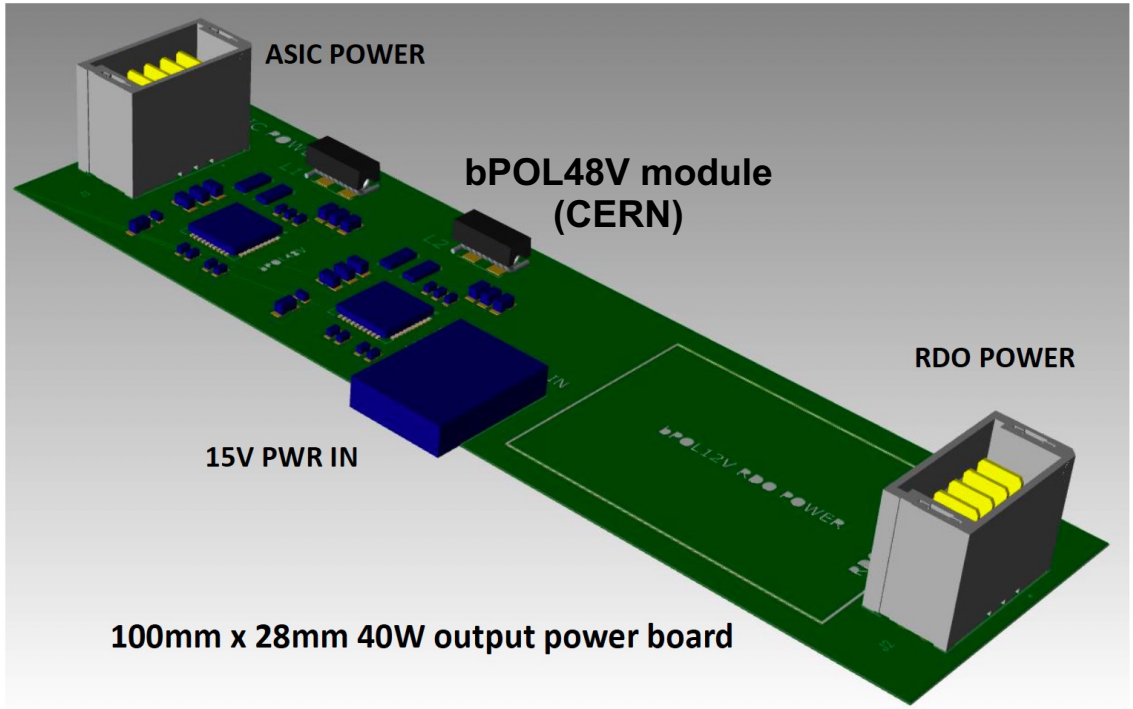


Preliminary tests indicate that commercial DC/DC converters will not meet the radiation requirement so the team is evaluating the CERN bPol48V and bPol12V converters as the potential option

FTOF Power board prototype v0 (FY25)

Preliminary schematics:

Dimension based on FTOF PB3 design



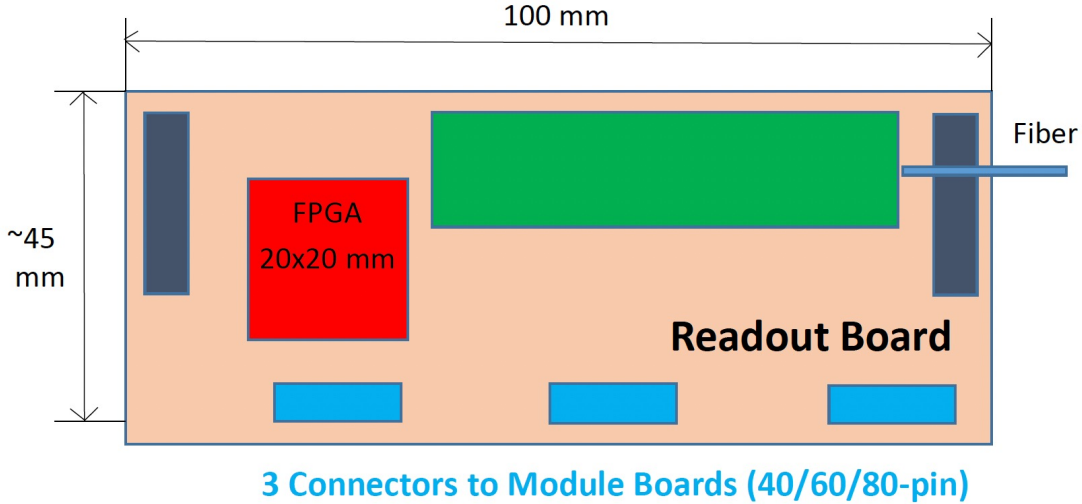
Tim Camarda (BNL)

Many details to be worked out and open questions to be addressed

FTOF Readout board v1 (FY25)

PB and RB design must be coordinated and kept compatible

Preliminary schematics (Mike Matveev, Rice U.):



Open Issues and Questions:

- Can PB provide all voltages needed?
- SFP+ occupies large space, do we have enough space for all other parts?
- Location of FPGA – how to cool it?
- LV/HV connectors on the RB or PB?

The list and number of signals to/from each ASIC to be determined: diff clock (2), diff control input (2), diff data output (2 or 4), I2C control (2), address (4/5/6), ASIC monitoring outputs (2/3/4).

Summary

The first pre-prototype readout boards have been produced and under evaluation and further development.

- On track to achieve the goal of establishing all essential functionalities of TOF RB by the end of 2024

The next iteration of service hybrids prototyping planned for 2025

- First realistic readout board prototype (v1) for FTOF
- First power board prototype compatible with RBv1

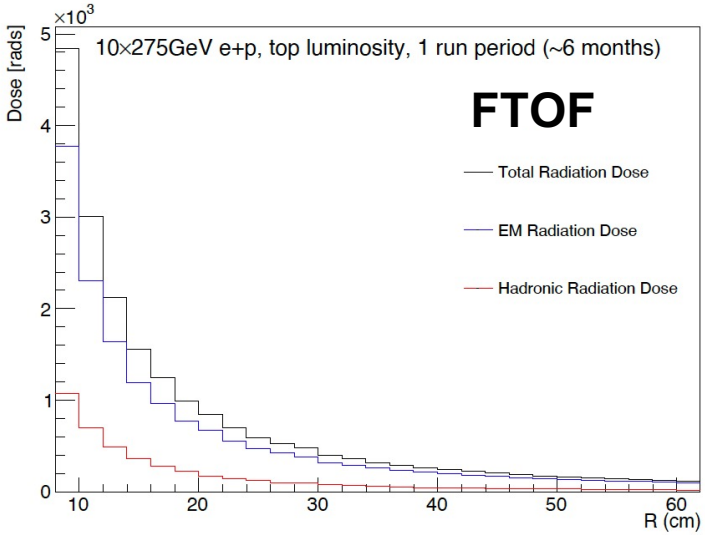
Tremendous progress has been made by a strong team. Still lots of work ahead and many open issues and questions to be resolved.

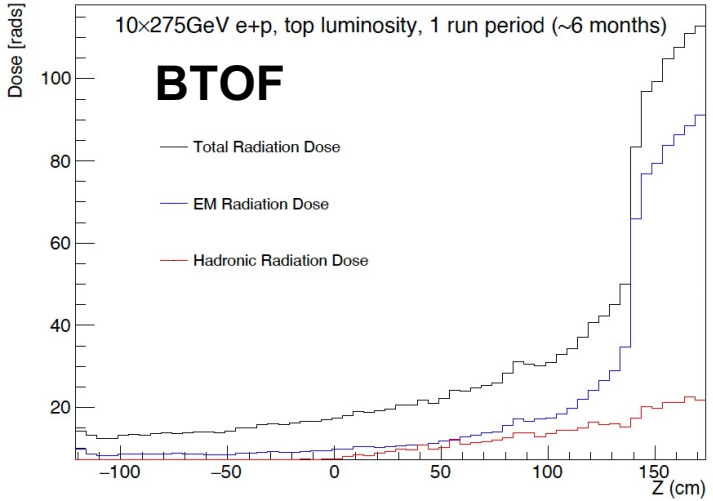
Backups

FTOF radiation dose

Signal+beam gas (updated)

Xiao Huang





Assuming 10 years of operation and a safety factor of 2, the most inner part of FTOF expects **~ 100 kRad**

FY25 FEE R&Ds via eRD109

A	B	C	D
Institution	Contact	Milestones	Approximate dates (assuming Oct. 1, 2024 as start date)
Rice	Wei Li	RBv1 schematics 50% complete; Order major parts	January 2025
		RBv1 schematics 100% complete (with internal review); Order all parts	March 2025
		RBv1 PCB layout complete (with internal review)	May 2025
		RBv1 fabrication and assembly complete. Boards delivered.	July 2025
		Basic electrical & power Q&A. Initial FPGA firmware tests	August 2025
		RBv1 FPGA firmware development	September 2025
LBNL	Zhenyu Ye	Beam tests of ppRDO with ETROC2	January 2025
		Radiation tests of ppRDO	March 2025
		FCFD emulator design 50% complete	May 2025
		FCFD emulator design 100% complete	June 2025
		FCFD emulator fabrication and assembly complete	July 2025
		FCFD emulator testing with ppRDO	August 2025
		FCFD emulator testing with RBv1	September 2025
BNL	Prithwish Tribedy	PBv0 schematics 50% complete; Order major parts	January 2025
		PBv0 schematics 100% complete (with internal review); Order all parts	March 2025
		PBv0 PCB layout complete (with internal review)	May 2025
		PBv0 fabrication and assembly complete. Boards delivered.	July 2025
		Basic electrical & power Q&A. Power efficiency measurements	September 2025
		EICROC1 interface with ppRDO when available	May 2025
		EICROC1 interface with RBv1 when available	September 2025