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SVT Readout

J. Schambach

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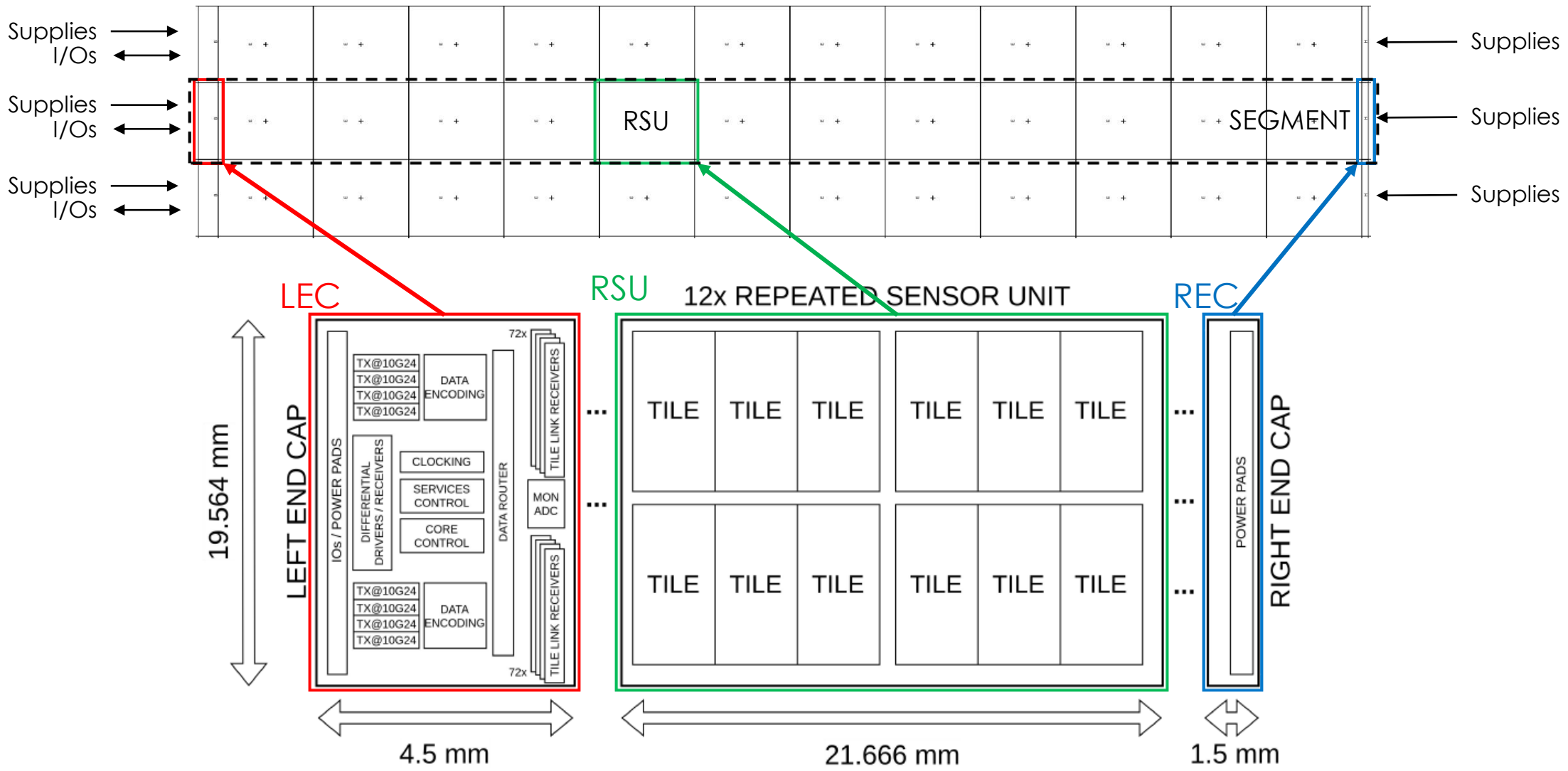
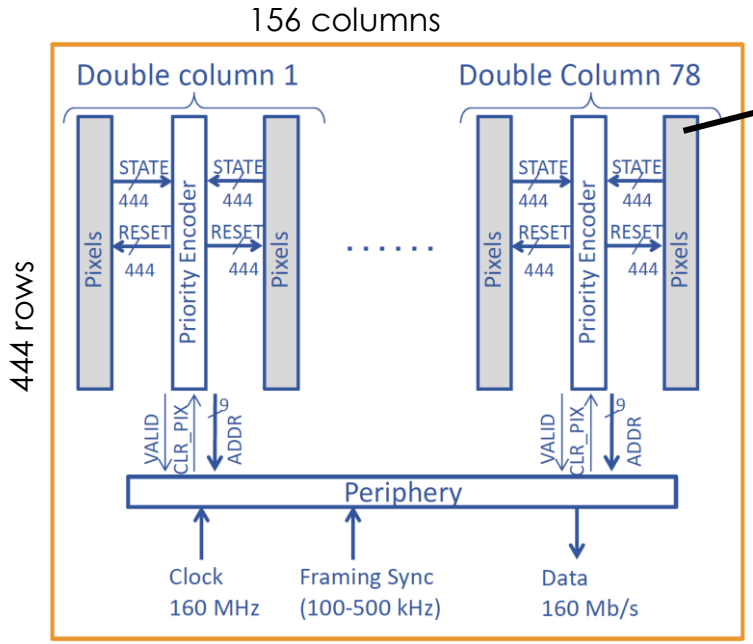
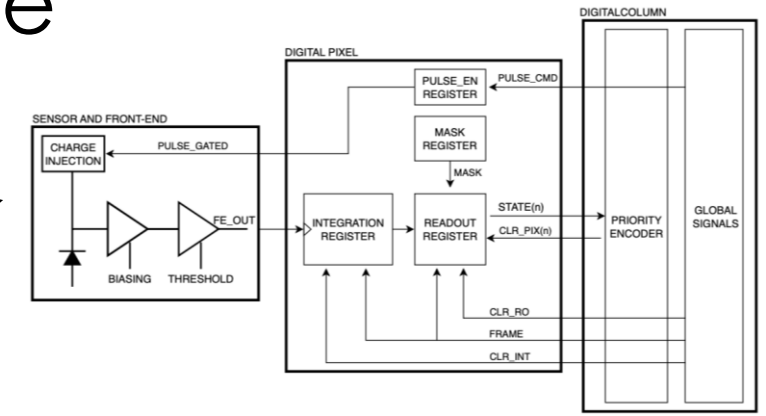
U.S. DEPARTMENT OF ENERGY

MOSAIX Architecture



Domain (Tile) Architecture





444 x 156 pixels / domain
831168 pixels per RSU
144 domains / segment
9.974 Mpixels / segment

20.8 µm x 22.8 µm pixel pitch(*)
Continuously active front-end (40 nW typ.)
Global shutter
Zero-suppressed matrix readout
Continuous readout mode
Integration time: 2µs to 2^{16}*25ns = 1.6384ms

(*) **Baseline: 20.8 µm * 22.8 µm**
Abs. Max: 22.5 µm * 25 µm

In pixel:

- Amplification
- Discrimination
- Hit integration register and readout register
- Test charge injection
- Digital pulsing
- Masking

Digital pixel designed with low-leakage, high reliability std cells

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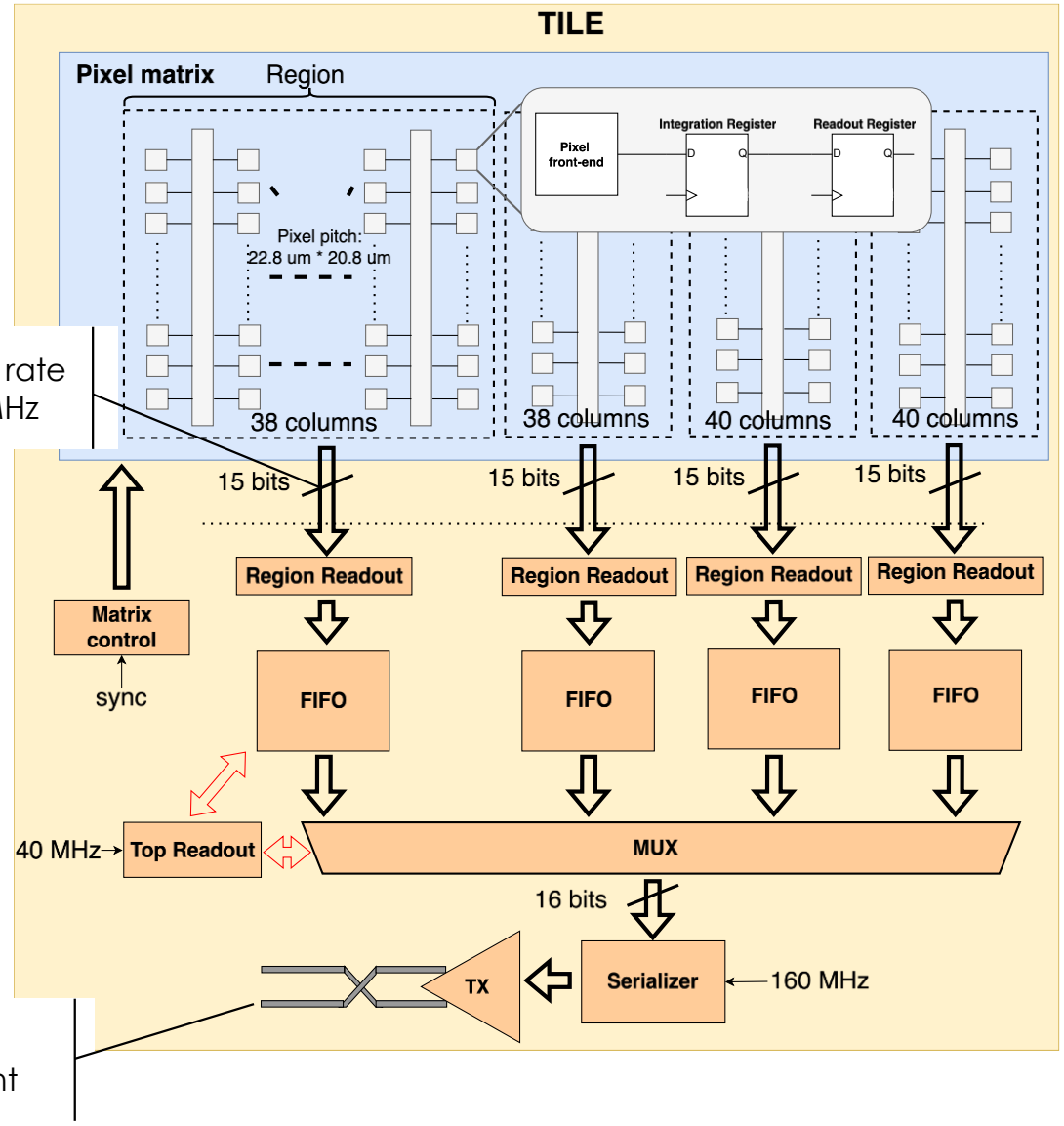
On-chip Readout Scheme in the Periphery

- Framing time base re-generated in each TILE periphery
  - FRAME local signal synchronizes pixels, Region Readout and Top Readout
  - Global SYNC input signal *aligns in time* the integration intervals across tiles
- Four parallel readout processes in each tile
  - Regions have 38 or 40 columns
  - Double columns in one region are sequentially read out
  - Region data packet is stored in FIFOs
  - Double columns and full regions can be masked
- Serial transmission of tile packet to LEC
  - Top readout aggregates region data packets for the same frame interval
  - Tile transmits one data packet for each frame interval, in order



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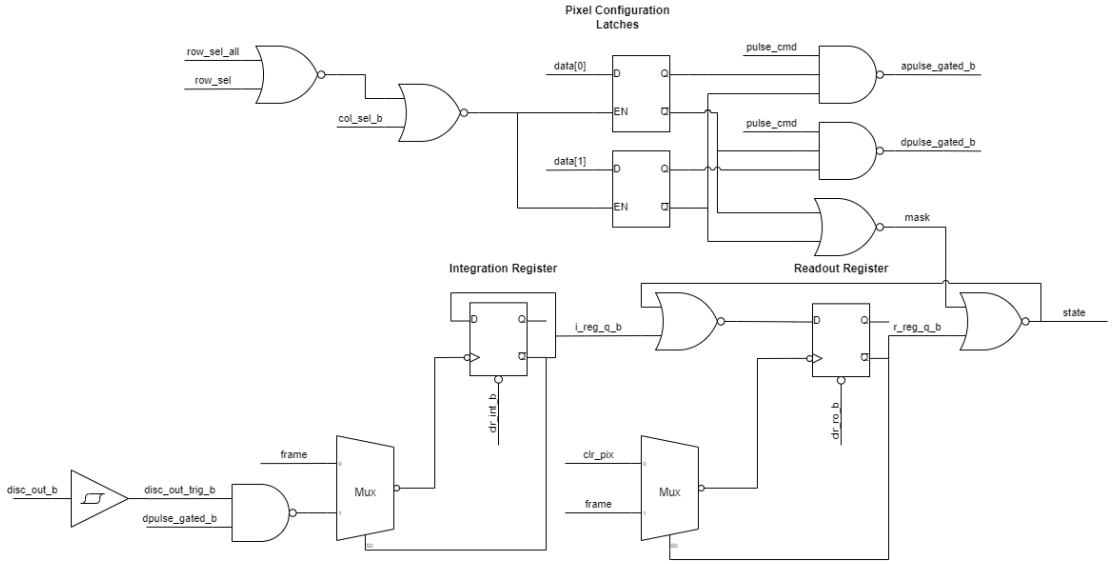
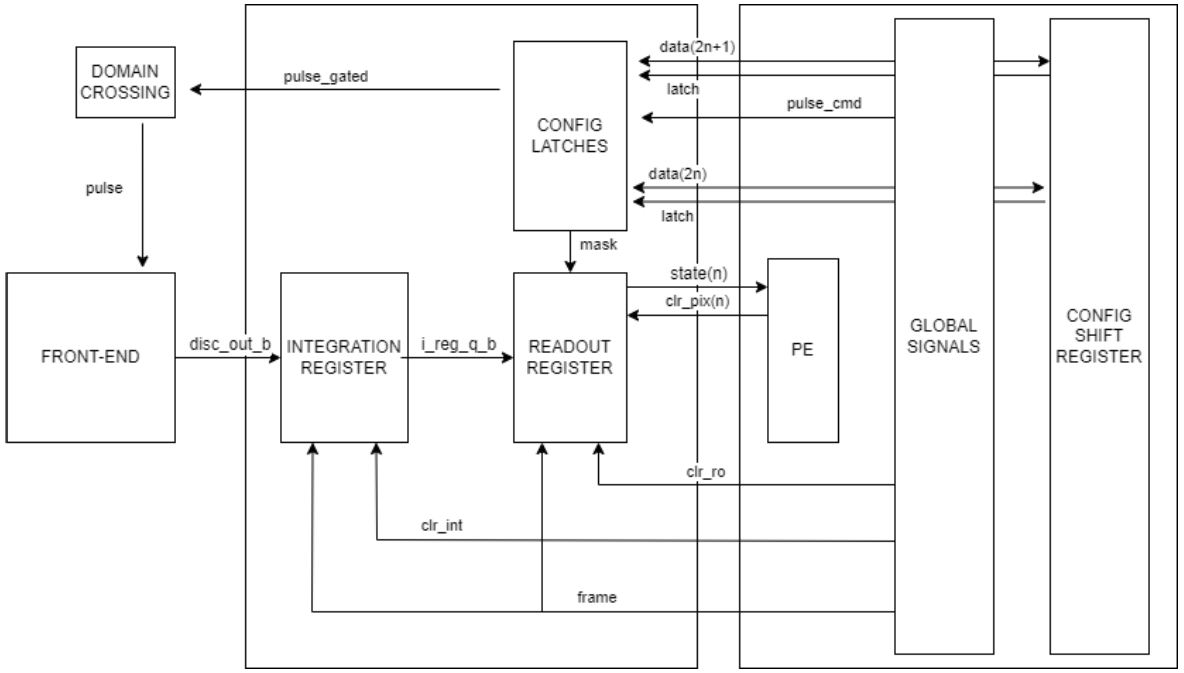
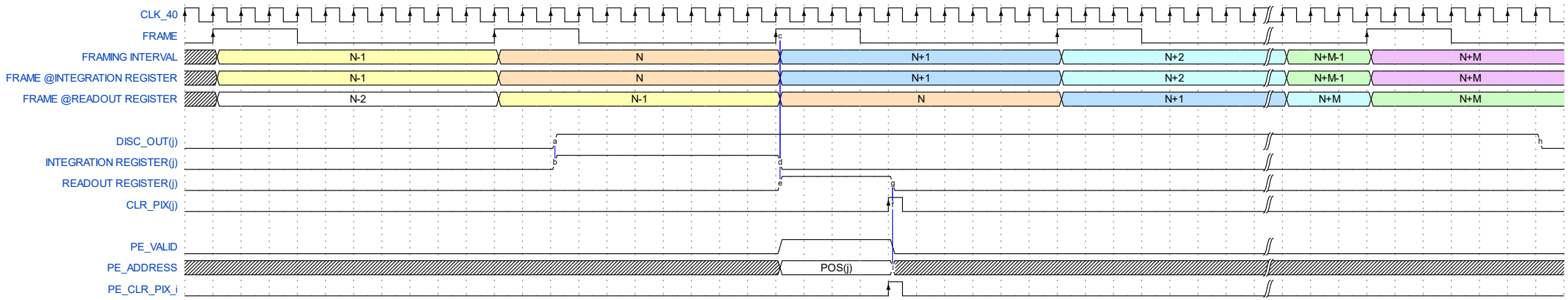
Tile Data Output







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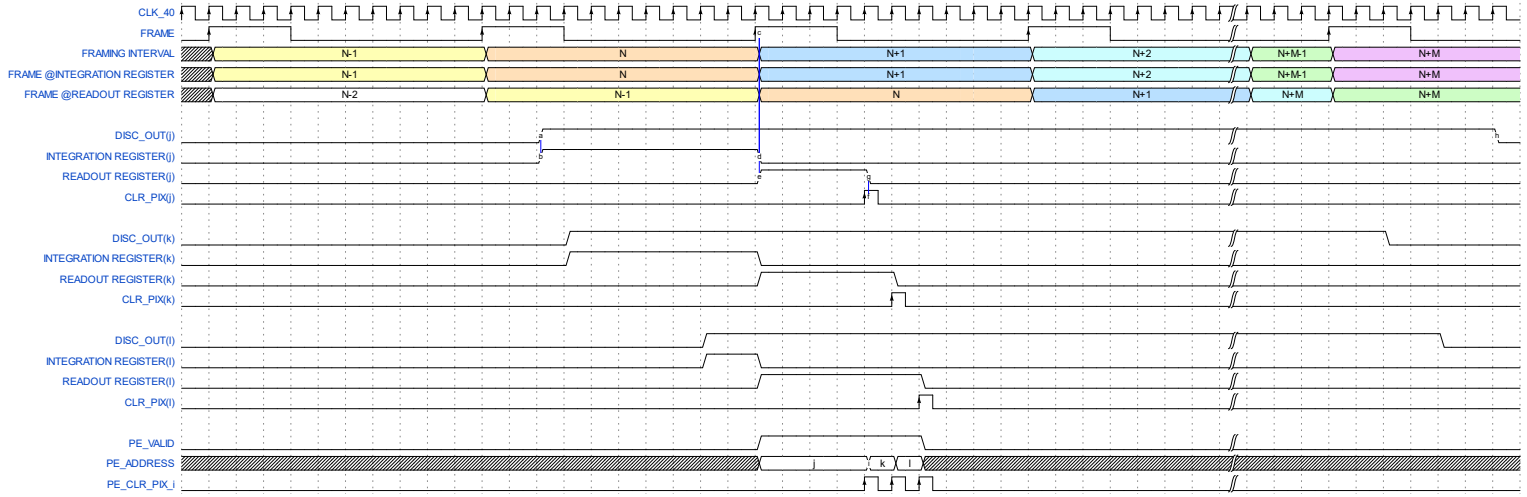
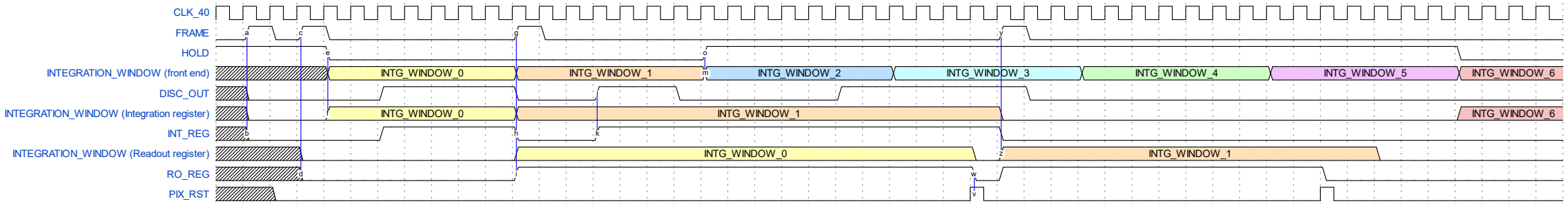
Pixel Array Readout Waveforms

Hits from one collision can be recorded in consecutive frame packets (time walk and spread of FRAME signals)



Region frame readout time can exceed the framing interval (from drop mode with priority to earliest frames)



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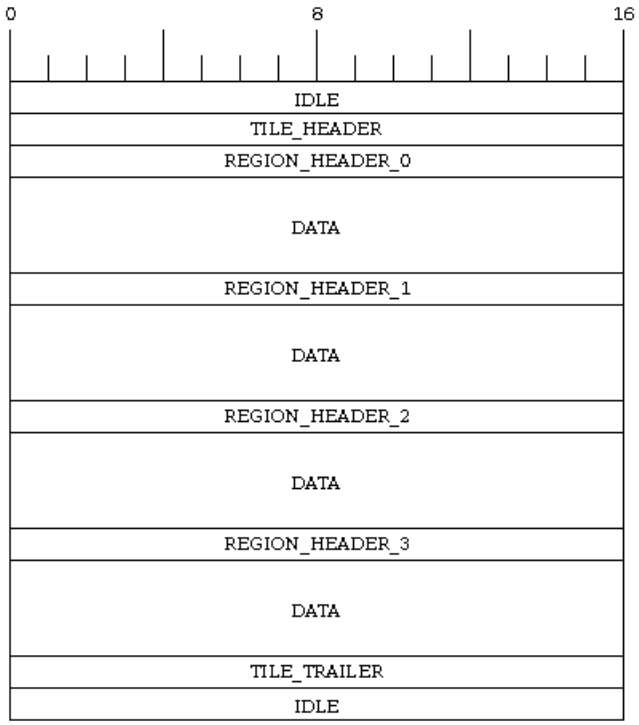
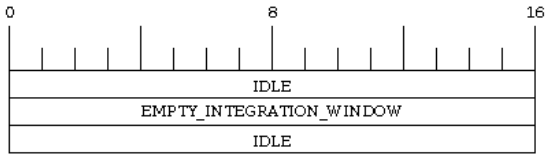
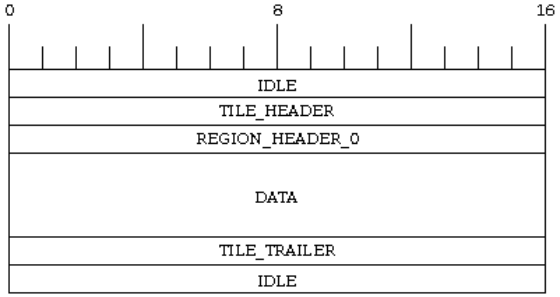
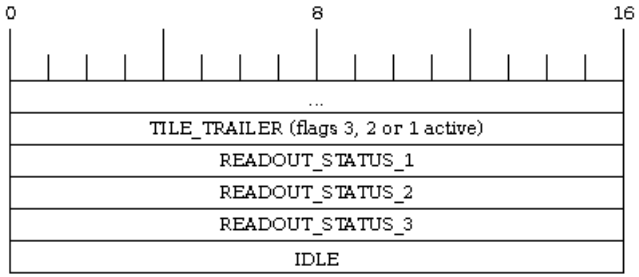
Tile Data Protocol

READOUT PROTOCOL																
Word type	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TILE_HEADER	1	1	0	0	0	Reserved[1:0]		Tile_Address[8:0]								Top/Bottom
REGION_HEADER	1	0	0	RRUAddress[1:0]		Integration_Window_Counter[10:0]										
DATA	0	Pixel_Address_X[8:0]									Pixel_Address_Y[5:0]					
DATA_EXTENSION	1	0	1	0	0	Pixel_Hit_Map[8:0]										
EMPTY_INTEGRATION_WINDOW	1	0	1	0	1	Integration_Window_Counter[10:0]										
TILE_TRAILER	1	0	1	1	Tile_Trailer_Flags[3:0]				Checksum[7:0]							
READOUT_STATUS_1	1	1	0	1	Readout_Status_Flags[3:0]				Integration_Window_Counter[31:24]							
READOUT_STATUS_2	1	1	1	0	Integration_Window_Counter[23:12]											
READOUT_STATUS_3	1	1	1	1	Integration_Window_Counter[11:0]											
IDLE	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0









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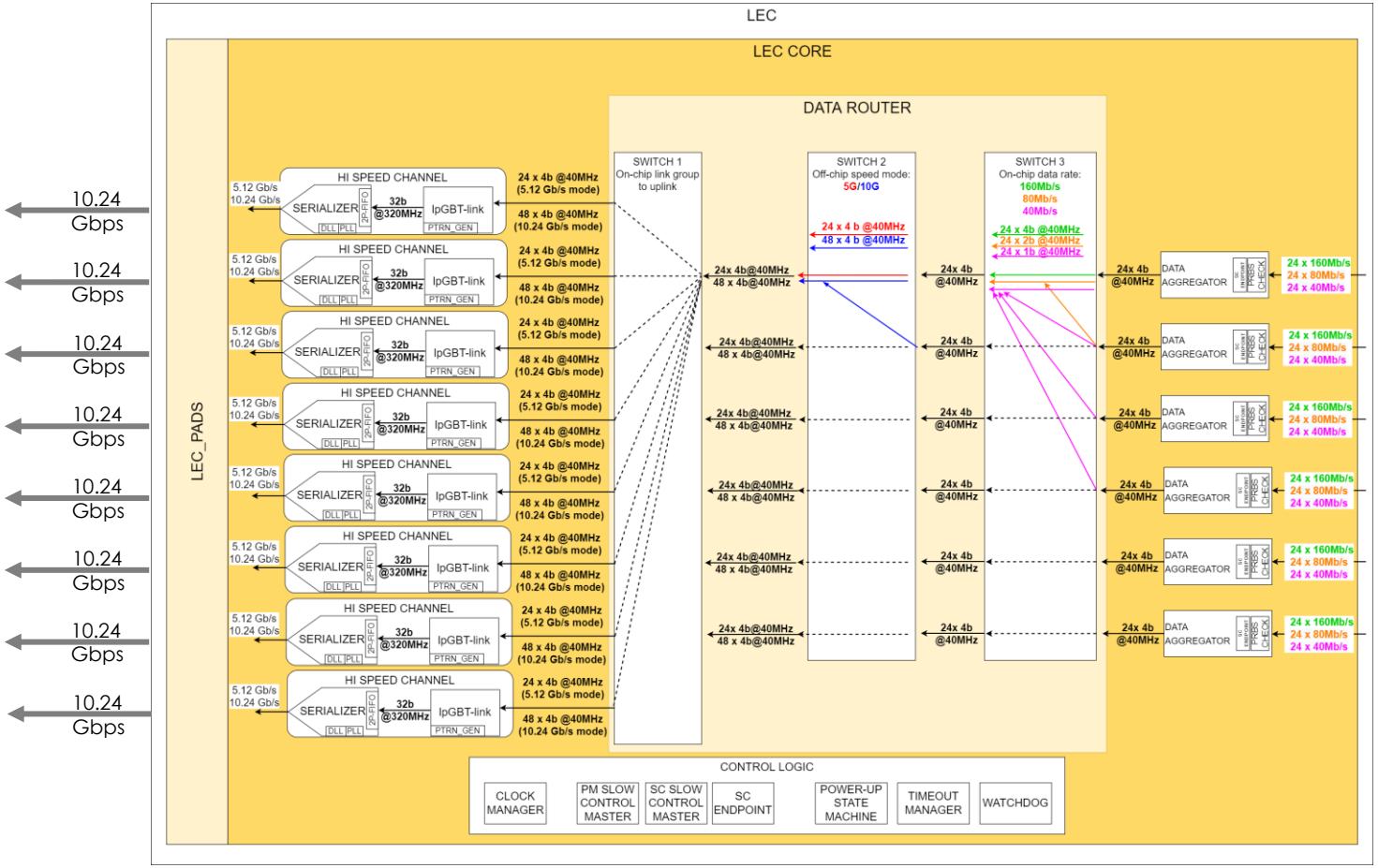
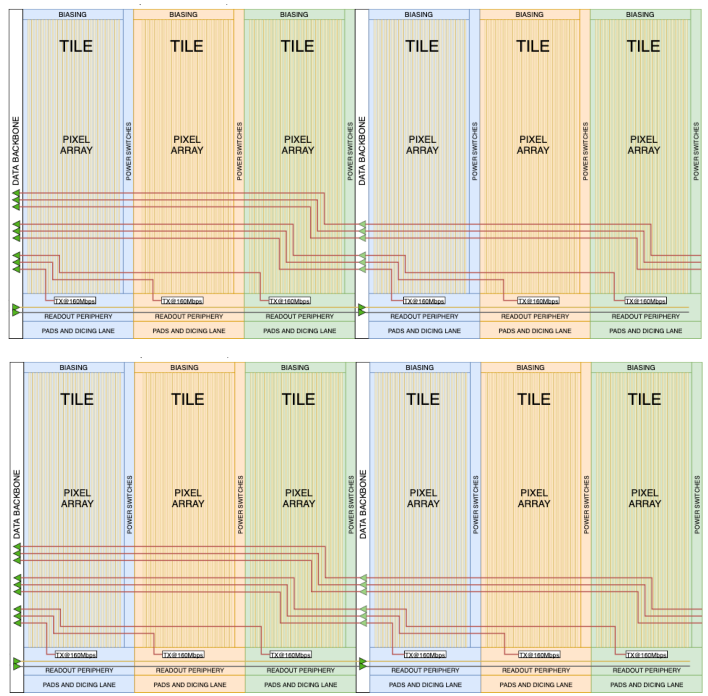
Data Flow – From Tiles to Left Endcap



72 Links

72 Links

x 12 RSU



12-RSU MOSAIX (SVT IB)

The data encoding block is the **lpGBT's TX** core
160 Mbps x 144 = 22.5 Gbps
Full capacity: 8 HS serializers = 80 Gbps (10 Gbps each, only 3 used)
Fallback: 40 Gbps, 5 Gbps each (6 used)
4 serializer data outputs drive one VTRx+

SVT Outer Barrel & Disks

6-RSU LAS
72 Tiles
1 HS serializer = 10 Gbps

5-RSU LAS
60 Tiles
1 HS serializer = 10 Gbps

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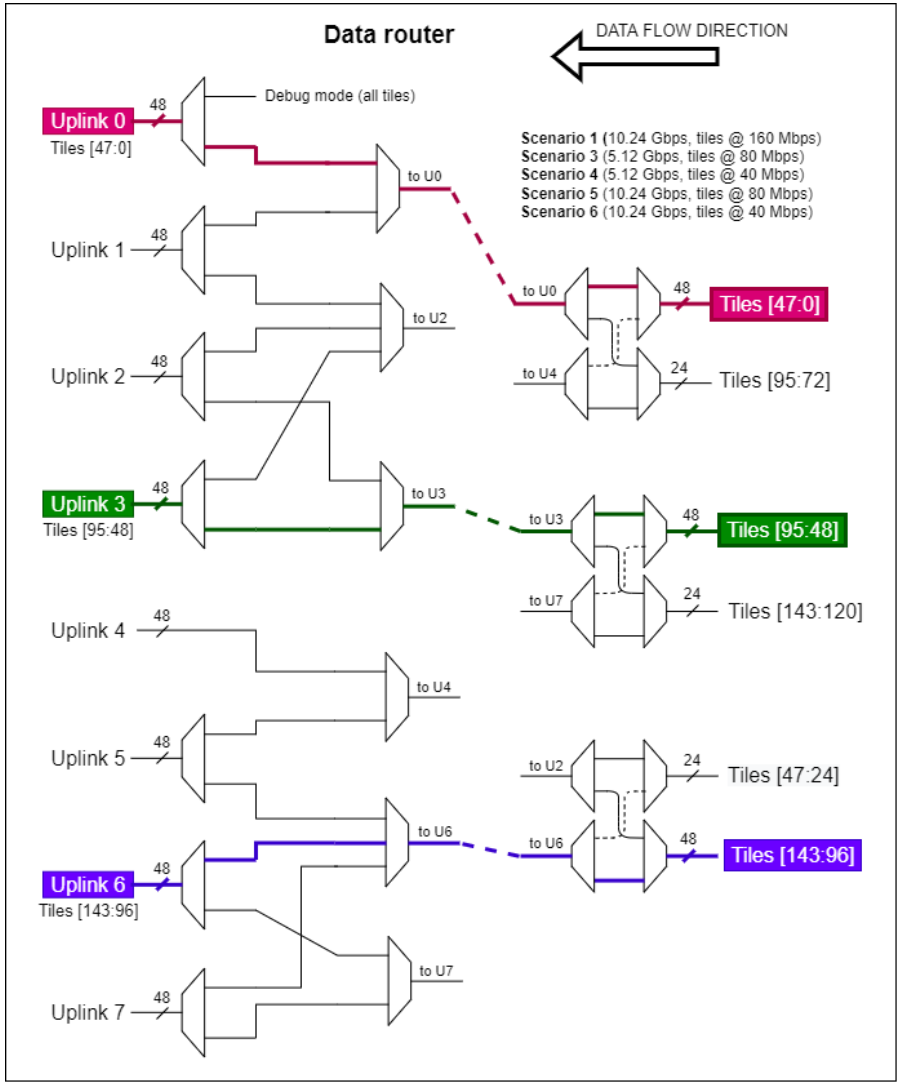
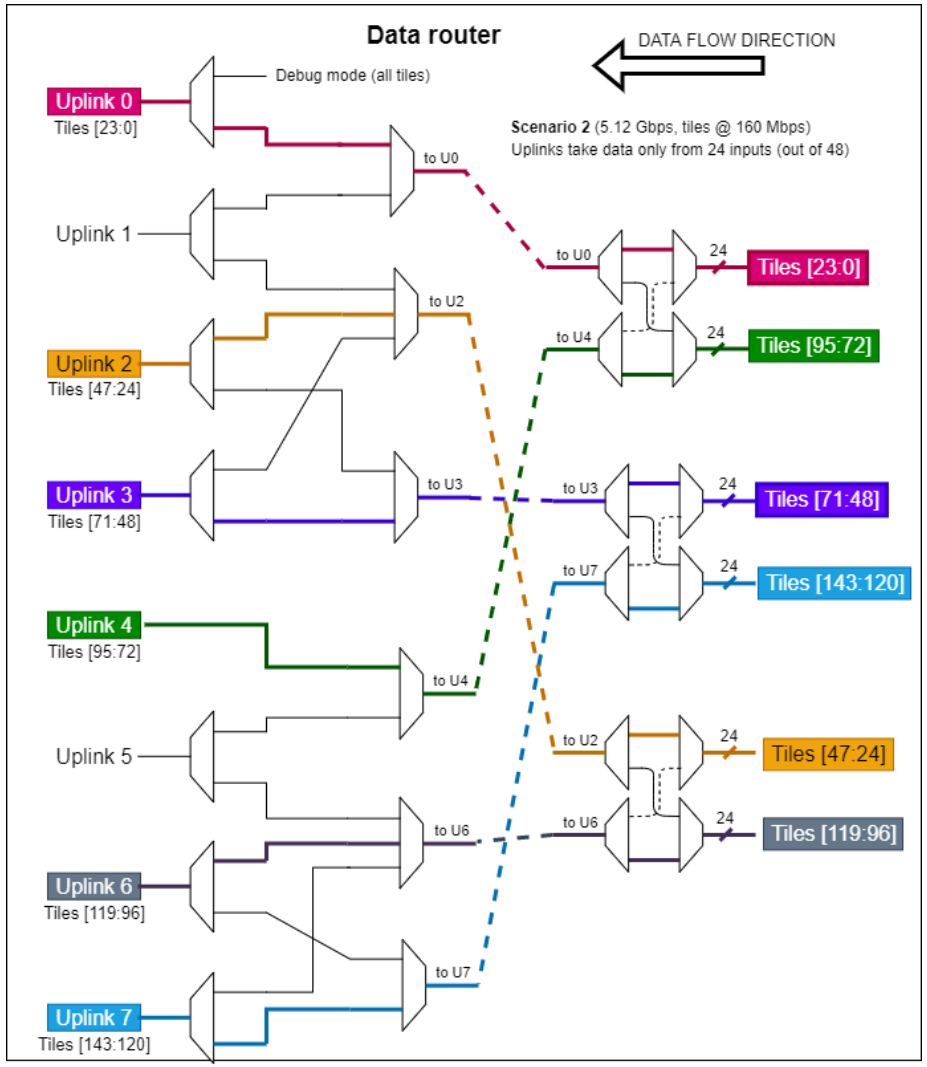
LEC Data Routing





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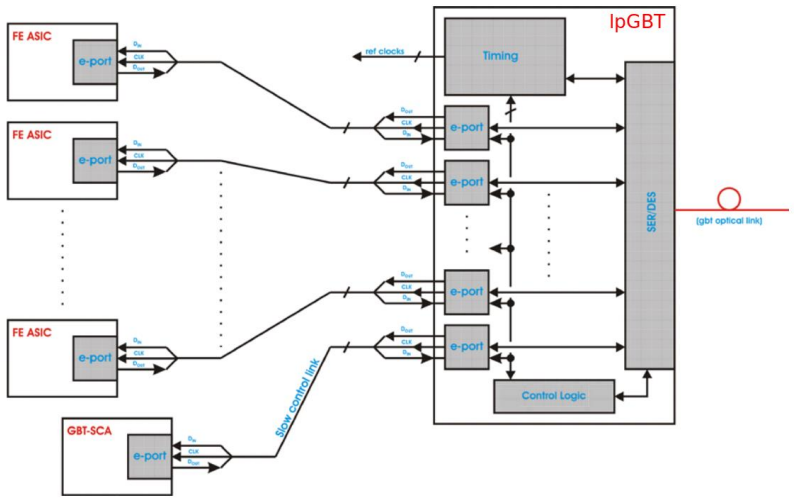
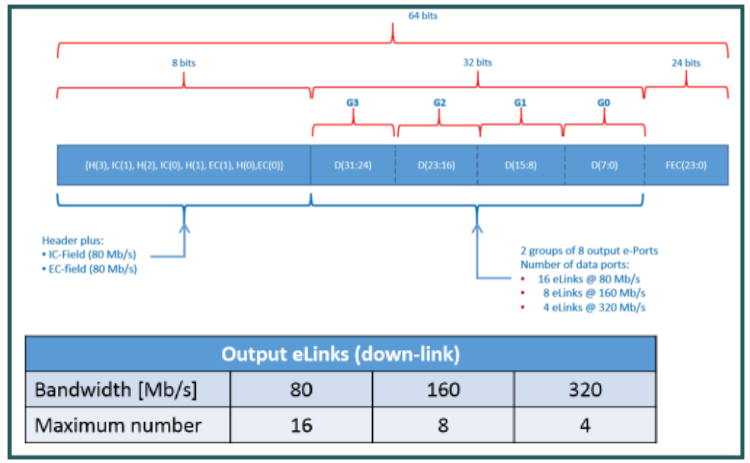
lpGBT Protocol



- Front Ends connect to “e-links”
- The fiber protocol includes “Forward Error Correction”
- Downlink runs at 2.56 Gbps
  - Downlink frame is 64bit wide, of which 32 bits are payload
  - 1.28 Gbps payload
  - Up to 16 e-links @ 80 Mbps
- Uplink runs at either 10.24 Gbps or 5.12 Gbps
  - Uplink frame is either 128bit or 256bit
  - 256bit frame contains 192bits of payload (7.68 Gbps)
  - Up to 24 e-links at either 160 Mbps or 320 Gbps



Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

Downlink

Line Rate: **2.56 Gbps**
32 out of 64 bits are data:
Payload = **1.280 Gbps**

Data Uplink

192 out of 256 bits are data:
Payload = **7.680 Gbps**

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Field	5.12 Gbps FEC5	5.12 Gbps FEC12	10.24 Gbps FEC5	10.24 Gbps FEC12
Frame [bits]	128		256	
Header [bits]	2		2	
IC [bits]	2		2	
EC [bits]	2		2	
D [bits]	112	96	224	192
FEC [bits]	10	24	20	48
LM [bits]	0	2	6	10
Correction [bits]	5	12	10	24
# of eLink groups	7	6	7	6

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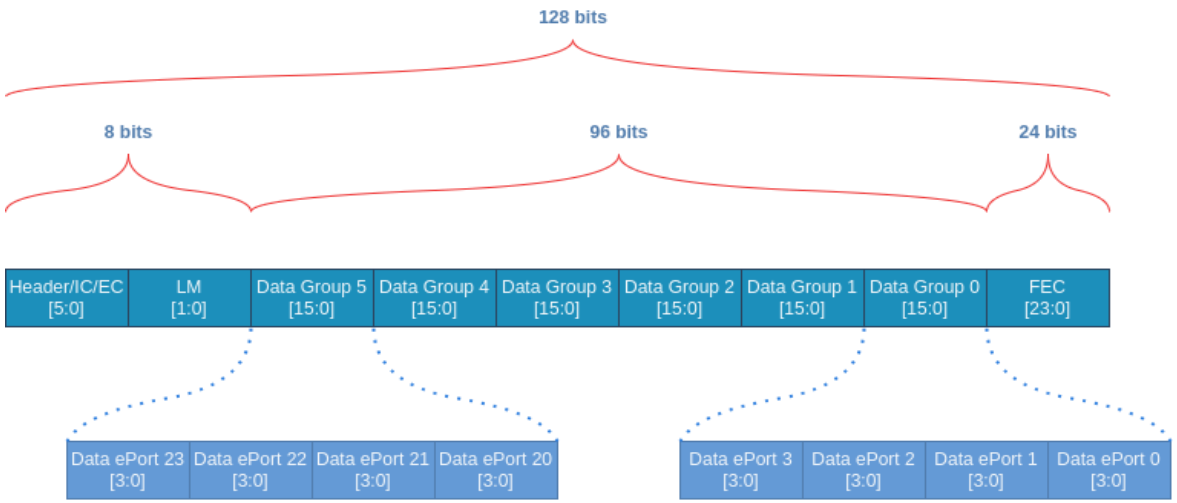
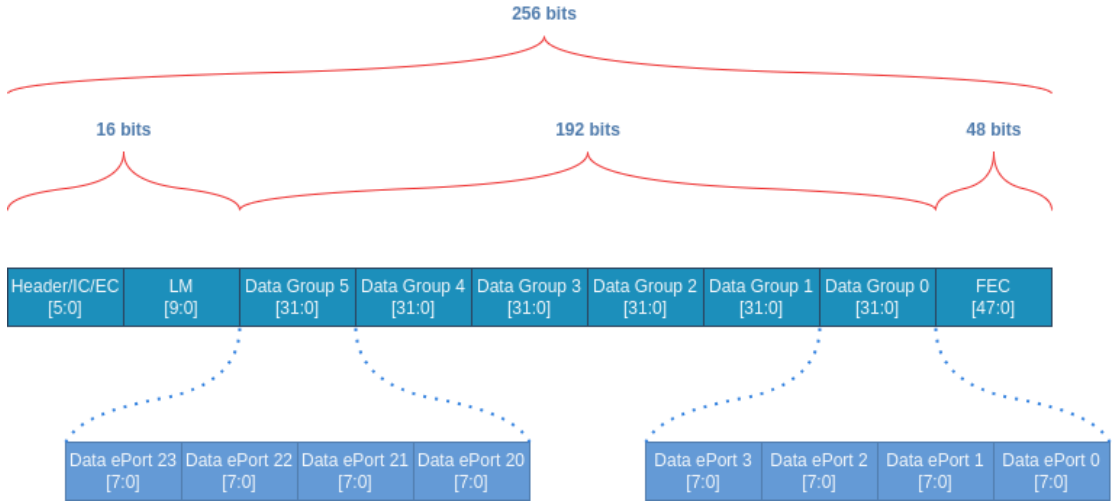
lpGBT ePort Routing

5.12Gbps



10.24Gbps



MOSAIX uplink						
Uplink bandwidth (Gbps)	5.12			10.24		
FEC Coding	FEC12			FEC12		
Tile bandwidth (Mbps)	40	80	160	40	80	160
Tiles per uplink [1]	48	48	24	48	48	48
Bits per tile	1	2	4	1	2	4
Tiles per ePort	2	2	1	2	2	2
Bits per ePort	4	4	4	8	8	8
Used bits per ePort	2	4	4	2	4	8
Bandwidth efficiency	50%	100%	100%	25%	50%	100%

1. To simplify routing scheme, 48 tiles are connected in instances where there are bandwidth enough to support a higher number of tiles.

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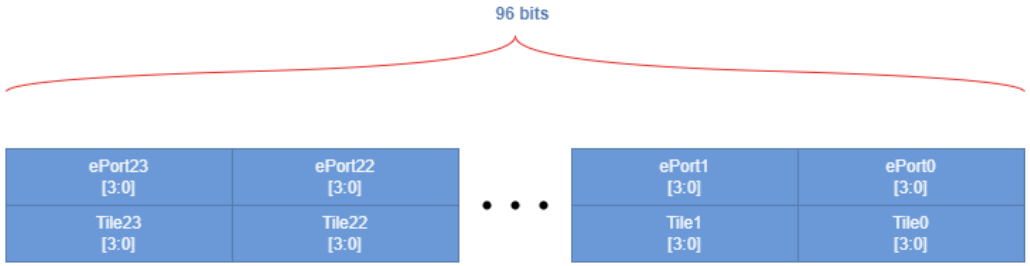
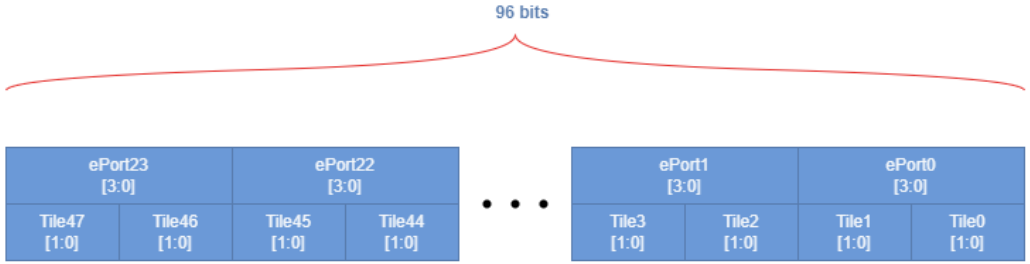
LEC Data Routing

5 Gbps / 160 MHz



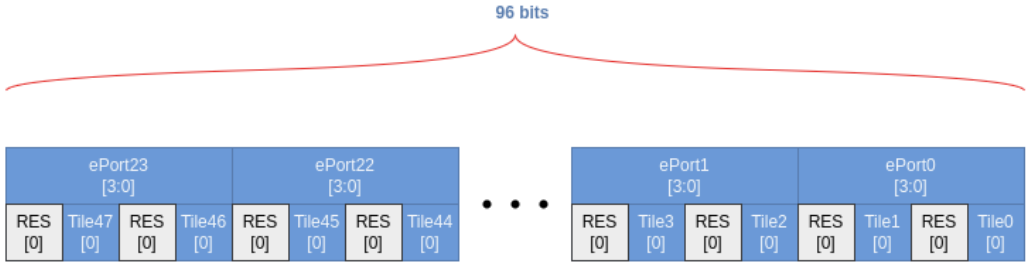
4 frames to reconstruct tile word

5 Gbps / 80 MHz



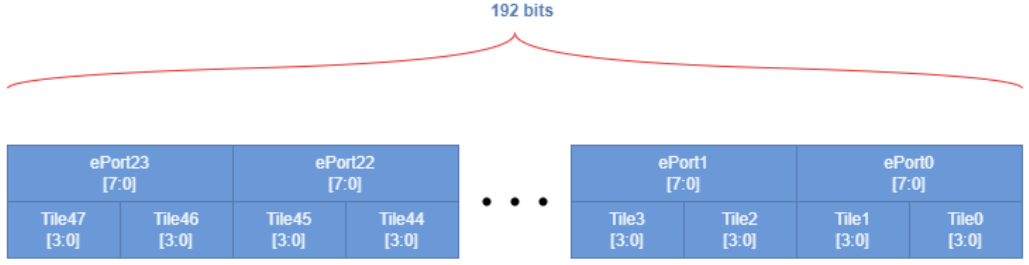
8 frames to reconstruct tile word

5 Gbps / 40 MHz



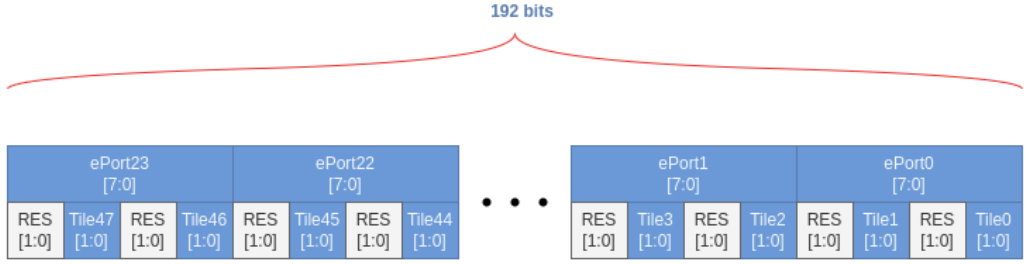
16 frames to reconstruct tile word

10 Gbps / 160 MHz



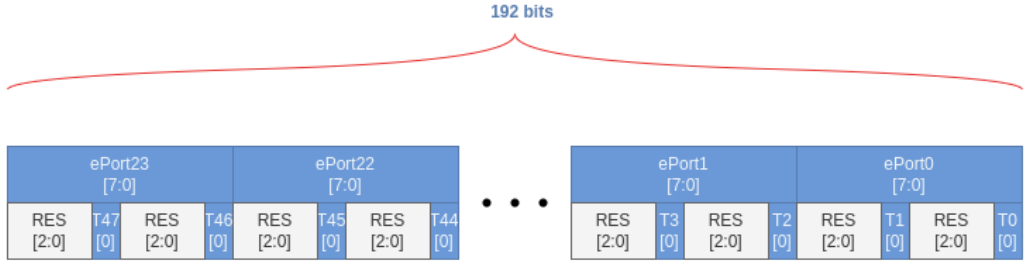
4 frames to reconstruct tile word

10 Gbps / 80 MHz



8 frames to reconstruct tile word

10 Gbps / 40 MHz



16 frames to reconstruct tile word

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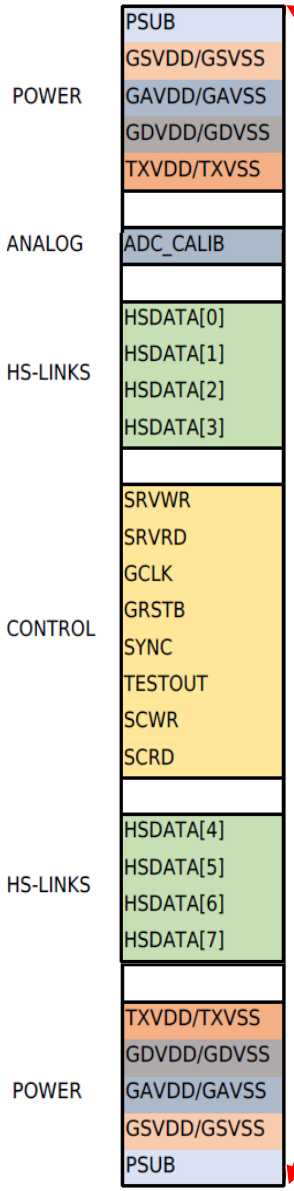
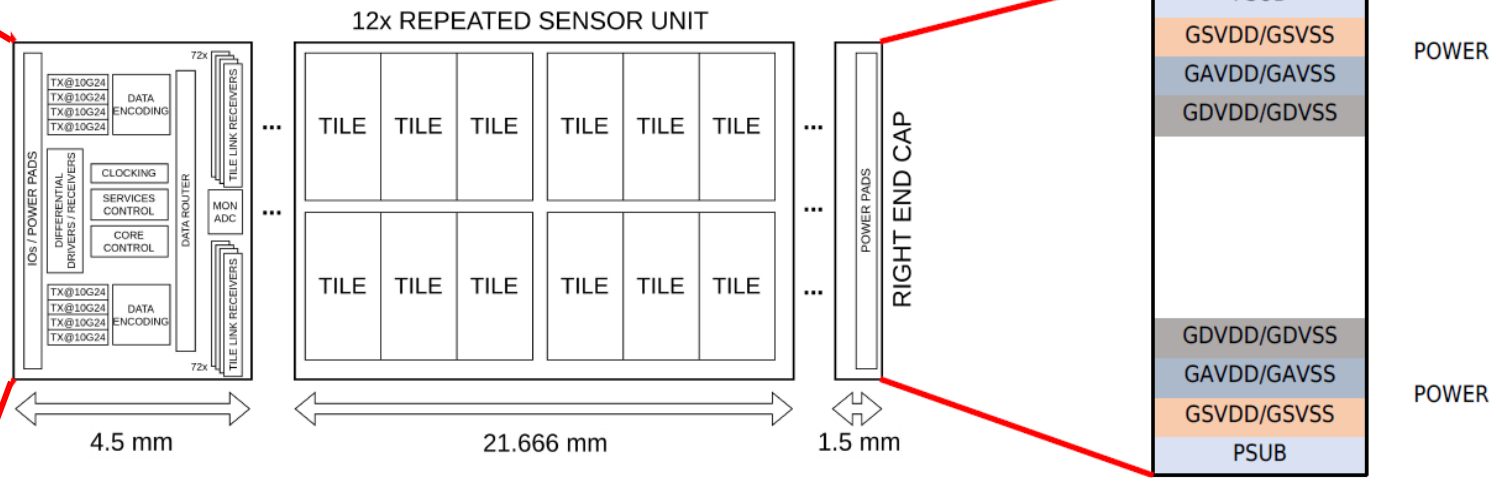
Supplies and I/Os





All I/Os are differential

8x 10.24 Gb/s data outputs

1x clock at 160 MHz

2x slow control buses at 5 Mbps

2x synchronization signals

(slow controls via lpGBT: 1 clk, 4 elink down, 2 elink up, 1 spare down)

Global analog and digital supplies per *segment*

On-chip supply segmentation and control

Reverse biasing of substrate (PSUB)

SVT LAS has power only from the LEC, no REC on LAS

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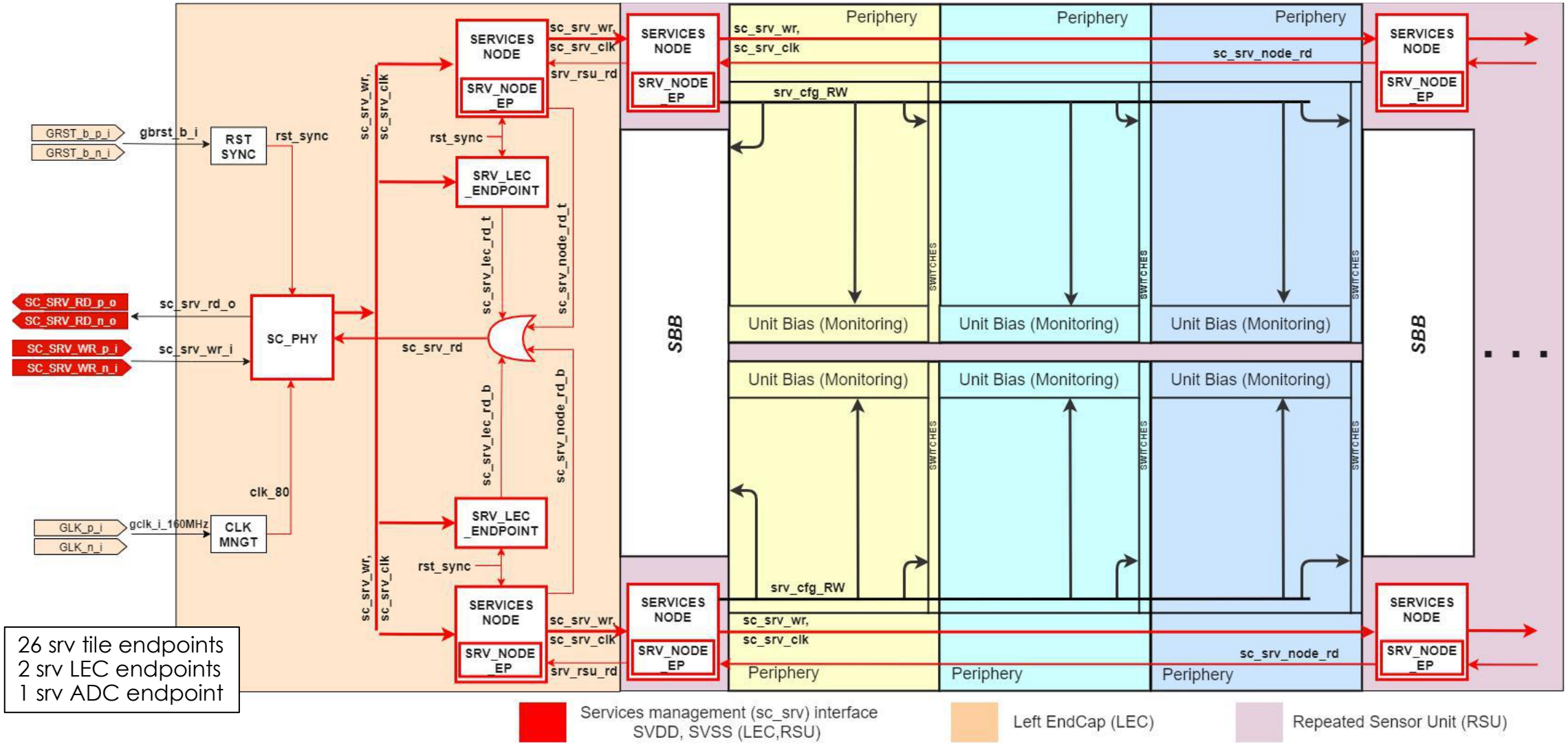
Slow Controls Architecture: Services Control



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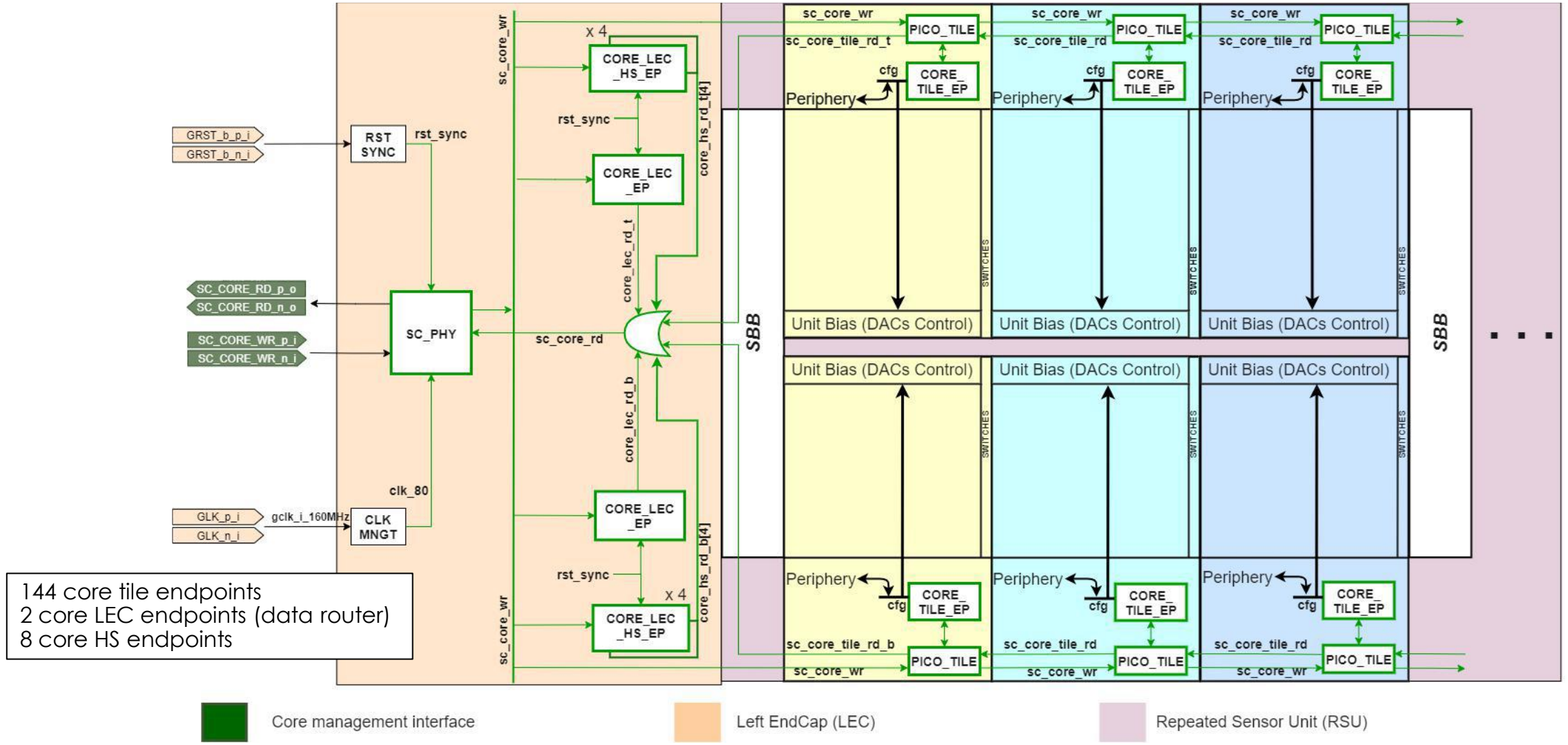
Slow Controls Architecture: Chip Control



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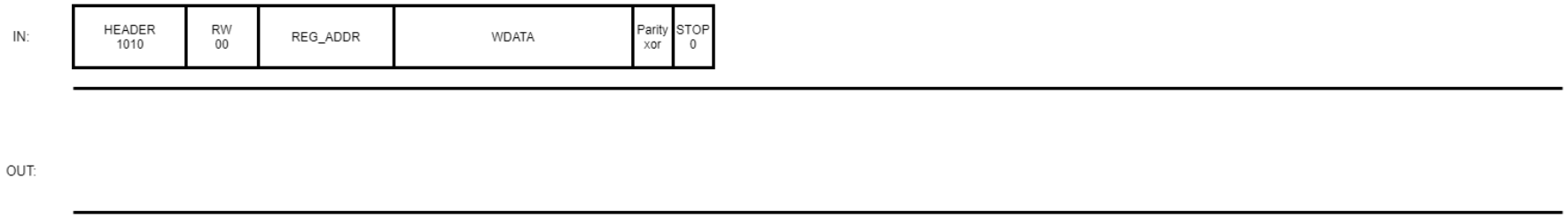
Slow Control Protocol

Field ID	Field Name	Width	Description
A	HDR	4	Fixed 4bit (4'hA) value that indicates a start of transaction
B	RW	2	Two bit field to indicate transaction type. 0: WRITE_posted transaction, 1: WRITE_non-posted transaction 2: READ transaction
C	EP_ADDR	8	Endpoint address
D	REG_ADDR	8	Register address
E	REG_DATA	16	Register write or read data
F	PARITY	1	Transaction parity bit (bit-wise xor of RW, EP_ADDR, REG_ADDR and REG_DATA fields)
G	STOP	1	Stop bit: 1'b0: Fixed 1bit (1'b0) value that indicates end of transaction

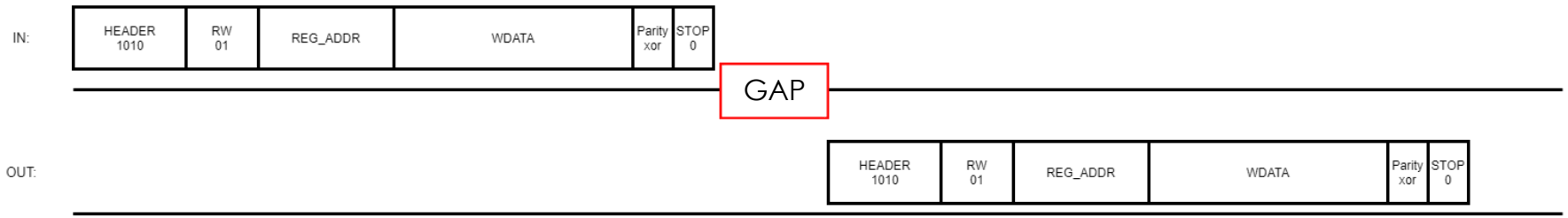
Transaction type	Direction	HDR	RW	ADDR	DATA	PARITY	STOP
WRITE_posted	Input to the ASIC	4'b1010	2'b00	Any valid register address	Data to write to the register	*xor* (HDR, RW, ADDR, DATA)	1'b0
WRITE_non-posted	Input to the ASIC	4'b1010	2'b01	Any valid register address	Data to write to the register	*xor* (HDR, RW, ADDR, DATA)	1'b0
WRITE-response	Output of the ASIC	4'b1010	2'b01	Register address as specified in the corresponding WRITE_non-posted transaction	Value of the register	*xor* (HDR, RW, ADDR, DATA)	1'b0
READ	Input to the ASIC	4'b1010	2'b10	Any valid register address	16'd0 (or 8'd0)	*xor* (HDR, RW, ADDR, DATA)	1'b0
READ-response	Output of the ASIC	4'b1010	2'b10	Register address as specified in the corresponding READ transaction	Value of the register	*xor* (HDR, RW, ADDR, DATA)	1'b0

Slow Control Transactions

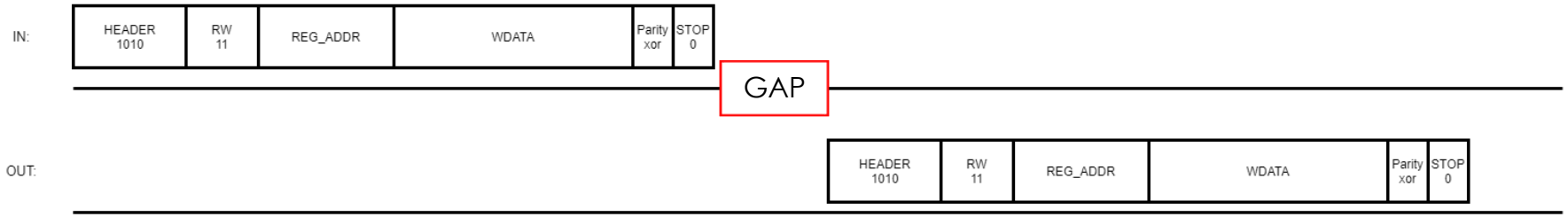
Posted Write Operation



Non-Posted Write Operation



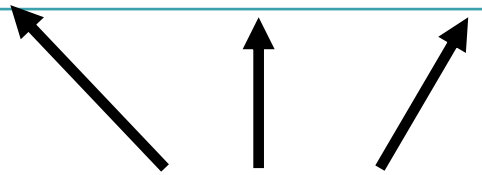
Read Operation



How long does it take to run calibration scans?

- Duration largely depend on parallelism
- In final readout system, full parallel scans possible
- Sequential scans probably required for wafer testing

	Powering (s)	Matrix configuration (s)	Integration (s)	Readout chip (s)	Readout backend (s)	Total
Parallel	0.5	121	568	92	538	**20 minutes**
Sequential	72	9212	81838	13258	538	**29 hours**



Main contributors

Assumptions:

- Threshold scan
- DAC resolution: 256
- Pulses per settings: 50
- Integration window: 100 us
- Gap between rows: 1000 us
- Readout polling: 500 us

How long does it take to configure the pixel matrix?

- Pixels configuration via periphery slow control endpoint
- Configuration accomplished by 4 actions:
  - Set configuration value
  - Select rows
  - Select columns
  - Commit

- Assuming the need to mask 1% of pixels:
- **Time to configure 1 tile: 0.028 seconds**
- **Time to configure a segment: 4 seconds**

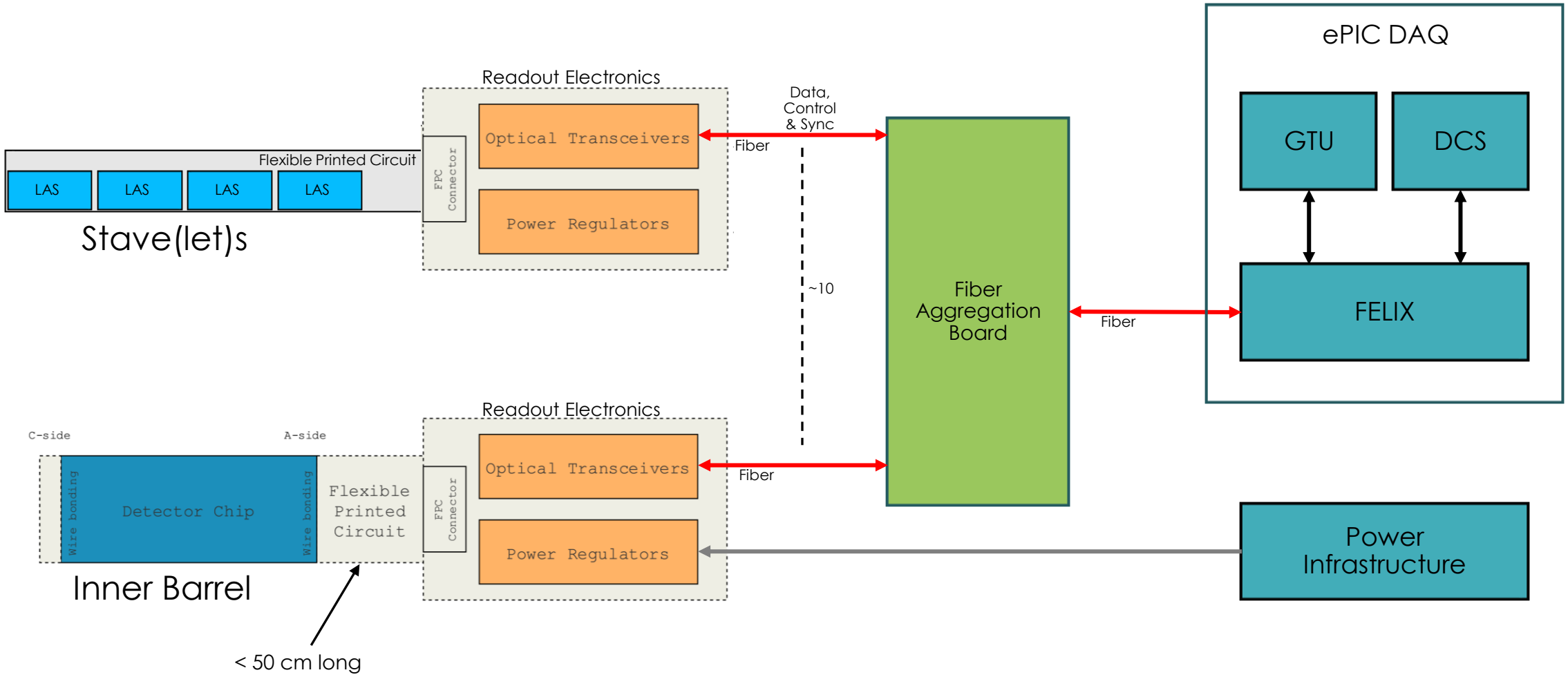
Configuration Scrubbing & Monitoring

- To ensure that all pixels keep their configuration during a run, the configuration should be updated with regular intervals.
- For scrubbing, individual pixels must be addresses, to avoid overwriting any non-default configuration

- Time to execute scrub cycle 1 tile: 2.8 seconds
- **Time to execute scrub cycle segment: 7 minutes**

- Tile readout monitoring:
  - Assuming less than 50 registers to monitor per tile
  - **< 200 ms** per segment

SVT Electronics – Simplified Overview



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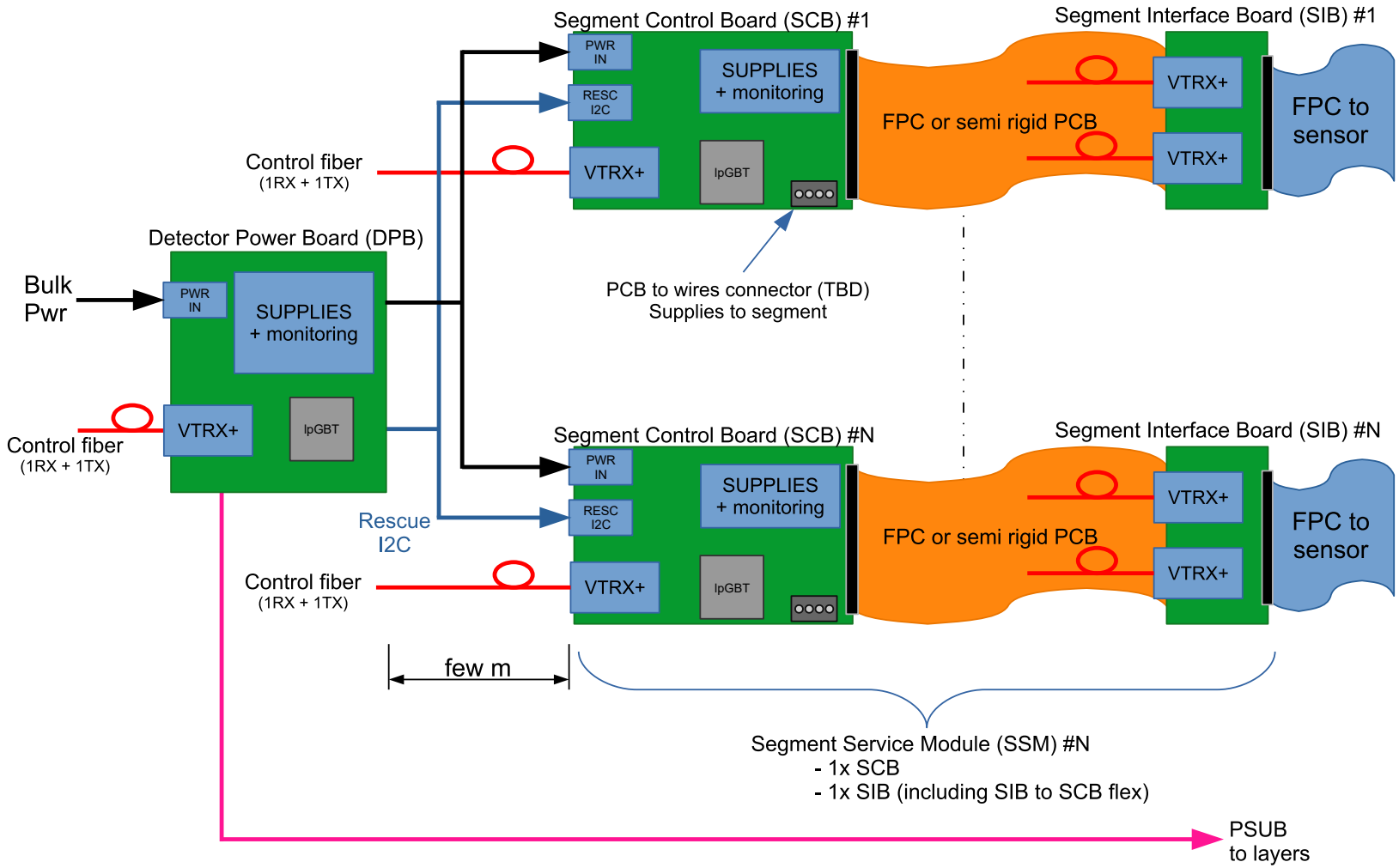
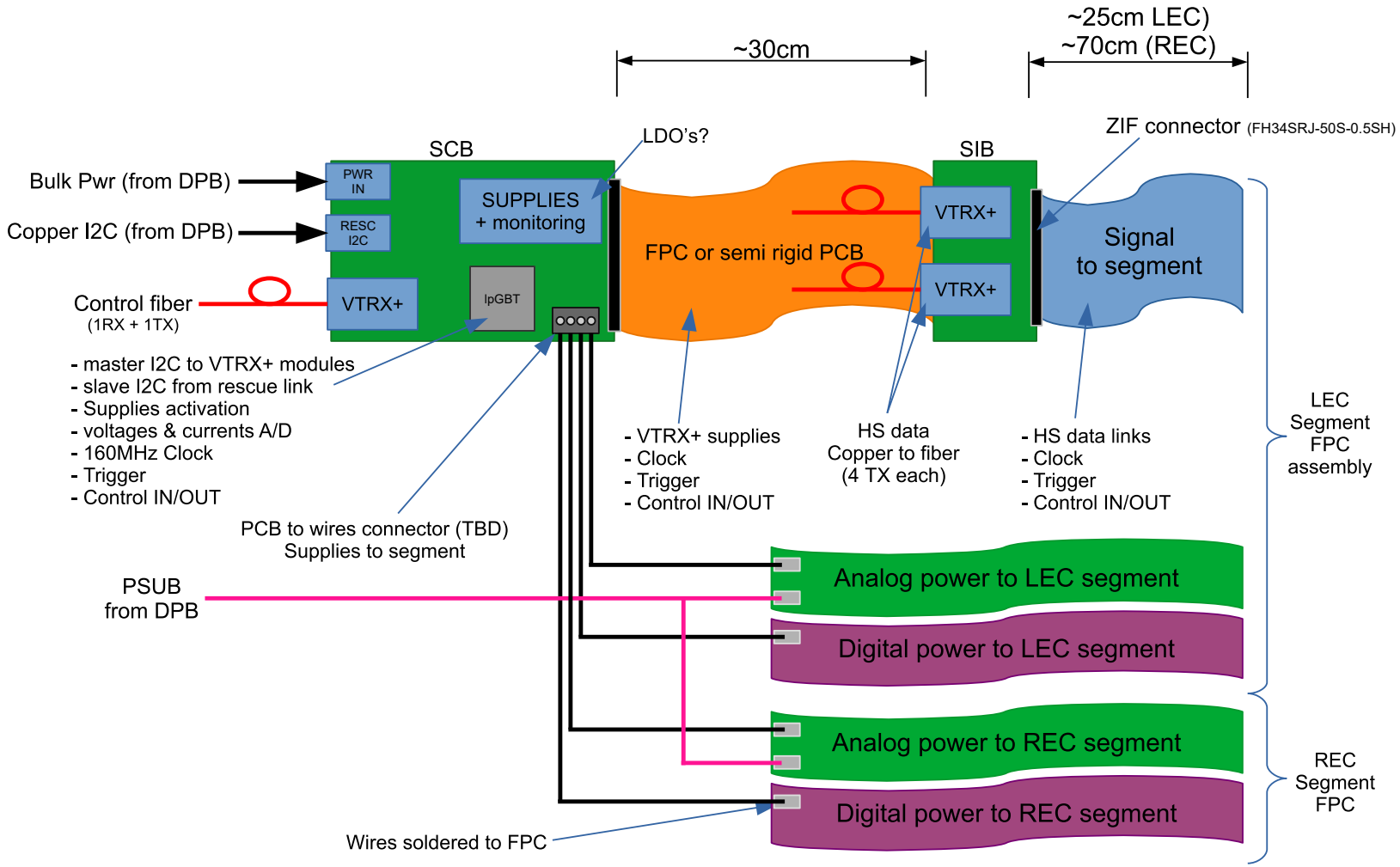
IB Readout Architecture

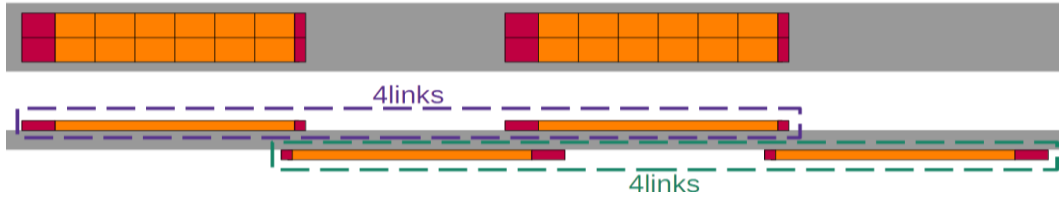


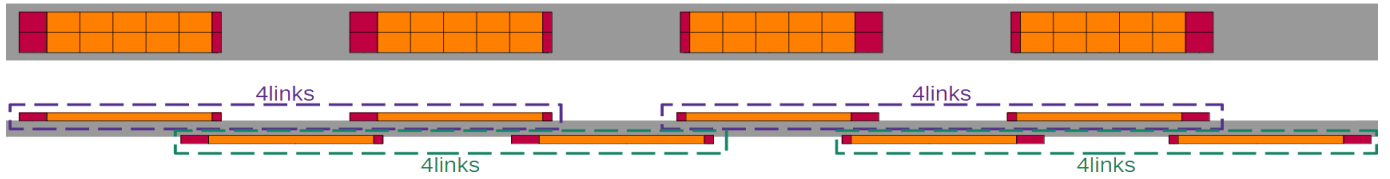
Readout Segment Architecture



Disk/Outer Barrel Readout Configuration

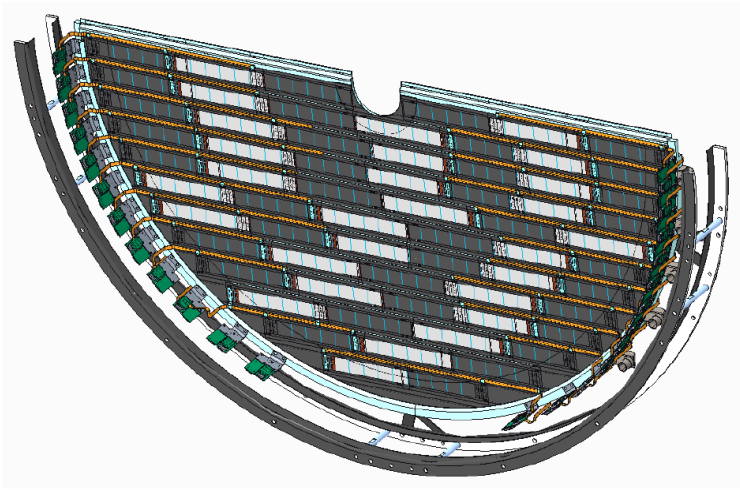
Outer Barrel Layer 3



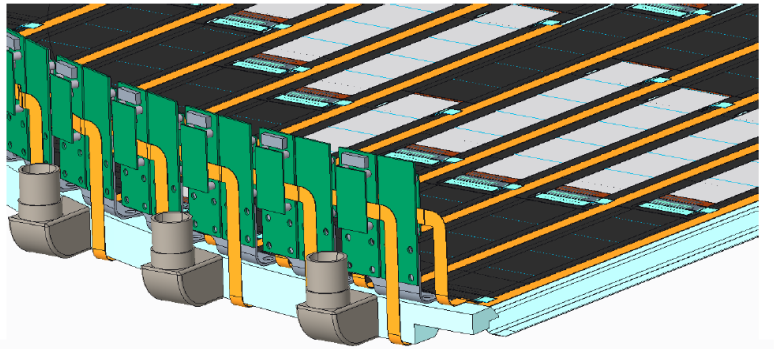


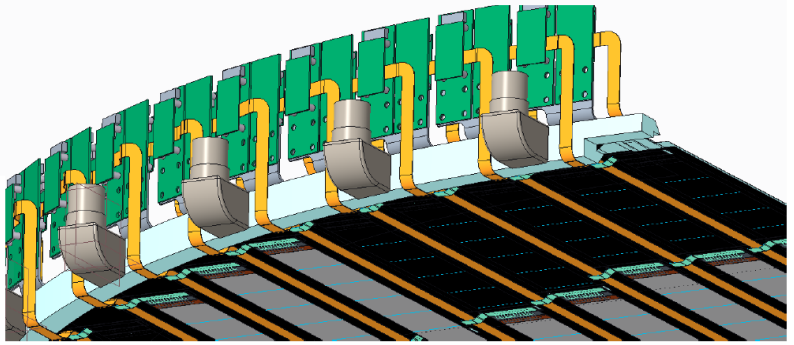
Outer Barrel Layer 4

Readout boards



Disks

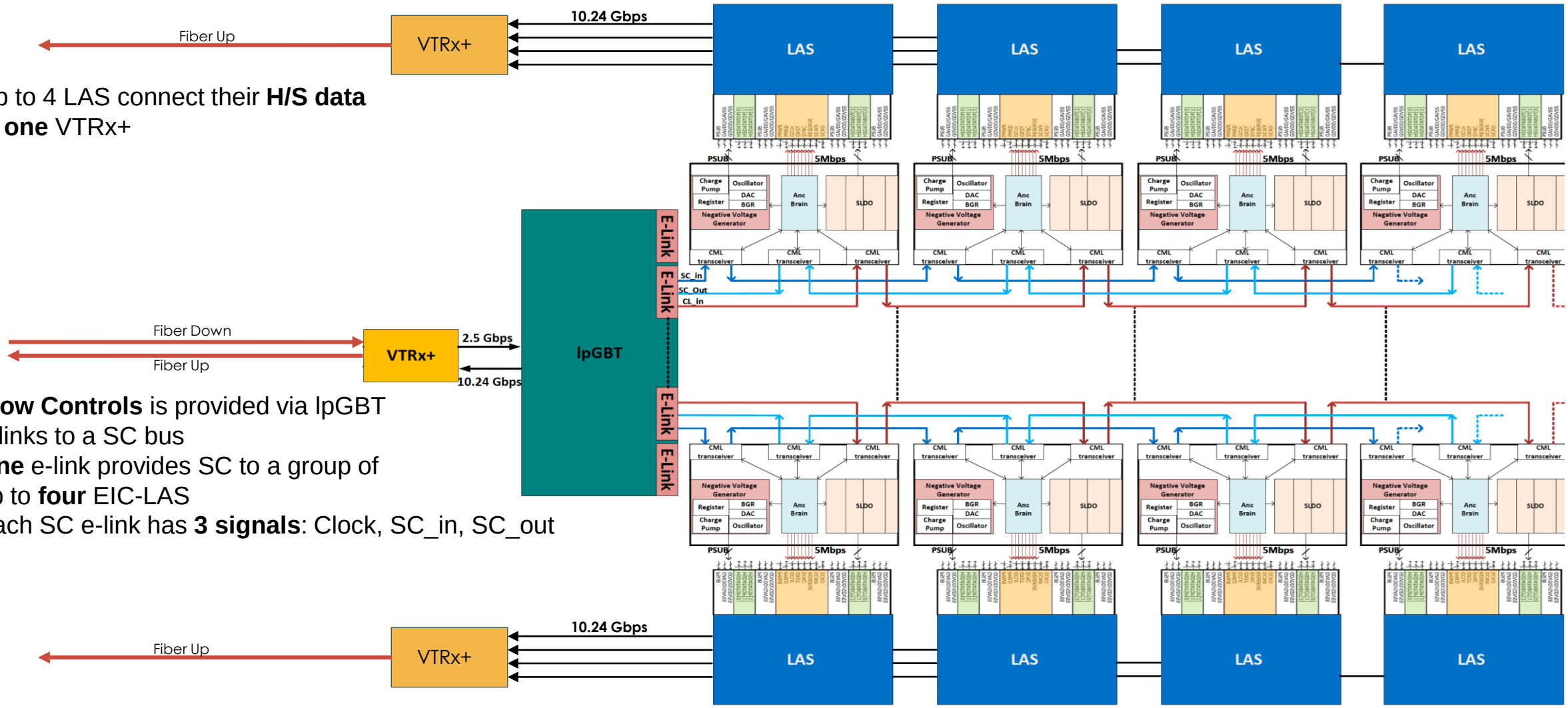




Outer Barrel and Disk Readout Electronics

Up to 4 LAS connect their **H/S data** to **one** VTRx+

Slow Controls is provided via lpGBT e-links to a SC bus
One e-link provides SC to a group of up to **four** EIC-LAS
Each SC e-link has **3 signals**: Clock, SC_in, SC_out



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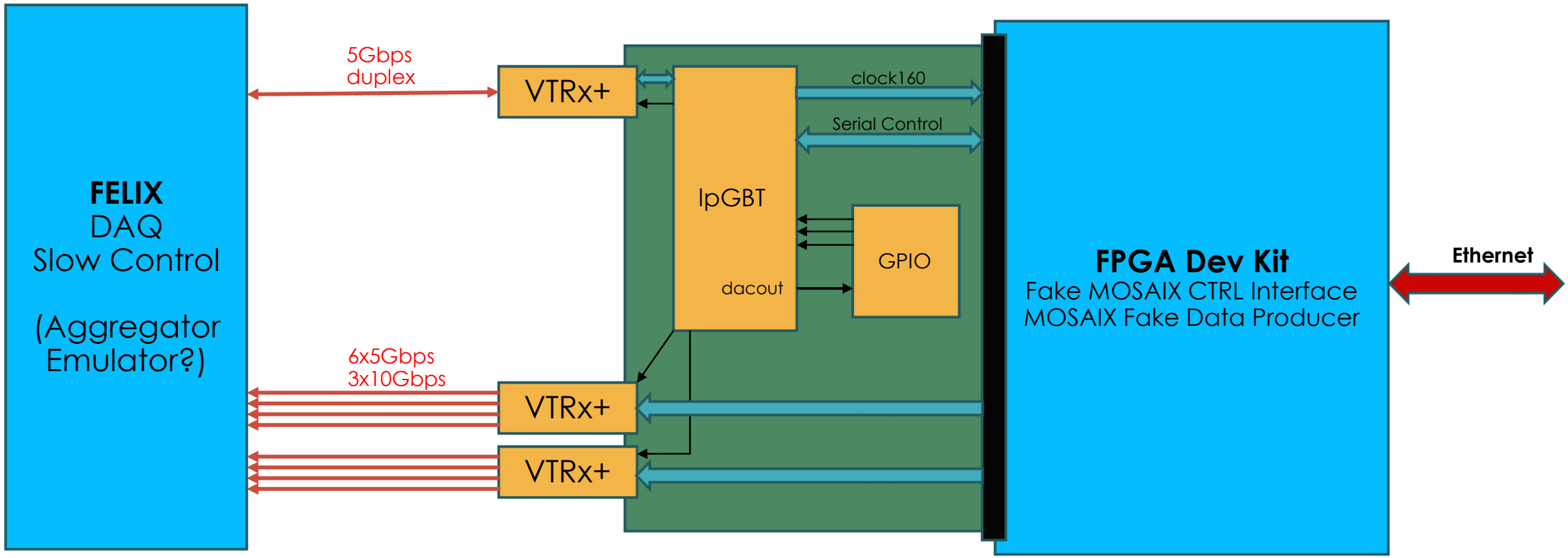
Assumptions for SVT lpGBT & VTRx+ Needs

- Each VTRx+ has 4 TX and 1 RX fiber
- Each lpGBT provides **16** output elinks on downlink side
  - Up to **4** of those are used for RDO internal use
  - Up to **12 down elinks** are available for slow controls
  - Uplink count needs are equal or smaller than downlink count needs
- For data up to 4 Readout links are connected to 1 VTRx+ where geometrically possible
- For slow controls on the **IB**, each of the 5 downlink control lines are connected individually to lpGBT output elinks
  - Each lpGBT is assumed to be used to serve (up to) **2 Segments**
- For slow controls on the **OB** and **Disks**, each "Module" (up to 4 LAS) is multiplexed to 1 elink (up and down)
  - Each lpGBT is assumed to be used to serve (up to) **8 "Modules"**
- Each lpGBT requires 1 VTRx+ (1 TX & 1 RX used)

SVT Counts

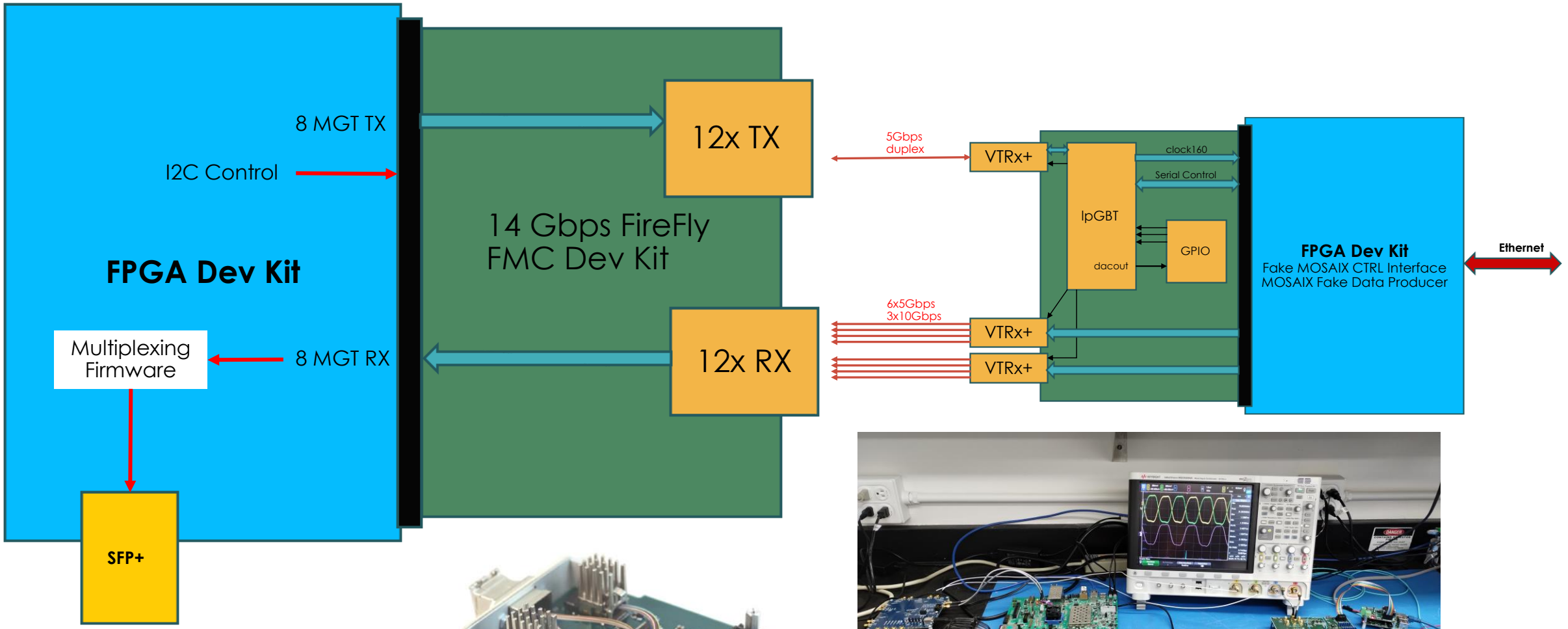
	width (mm)	length (mm)		# pixels per RSU														
Reticle size	19.564	21.666		**831,168**											Average Cluster size	4		
Pixel size	0.0208	0.0228																
																1.00E-08		
Barrel				**Sensor**													**10x100GeV**	
Layer Index	**radius (mm)**	**z (mm)**		**Area (mm^2)**	**RSU in width**	**RSU in length**	**# of sensors in r-phi**	**# of sensors in z**	**# pixels**	**# sensors**	**Notes**	**# Readout Links**	**# Staves**	**# Data VTRx+**	**# SC lpGBTs**	**Hit Rate / s**	**Hits/pixel/ 2us frame**	**Hit Rate / s**
L0	36	260		58,811	3	12	4	1	119,688,192	4	bent ITS3	96		24	6	4.50E+06	6.99E-08	2.73E+07
L1	48	260		78,414	4	12	4	1	159,584,256	4	bent ITS3	128		32	8	4.85E+06	5.65E-08	2.94E+07
L2	120	260		196,035	5	12	8	1	398,960,640	8	bent ITS3	320		80	20	1.41E+06	6.57E-09	8.55E+06
L3	270	520		882,158	1	6	96	4	1,915,011,072	384	6 -RSU LAS	384	48	96	12	8.55E+05	8.30E-10	5.19E+06
L4	420	840		2,216,706	1	5	148	8	4,920,514,560	1184	5-RSU LAS	1184	74	296	37	8.89E+05	3.36E-10	5.39E+06
e-endcap																		
Disk index	**z (mm)**	**inner r (mm)**	**outer r (mm)**			**5-RSU LAS**							**Readout Modules**					
ED0	-250	36.76	240	176,710		96			339,116,544	96	5-RSU LAS	96	26	26	4	3.66E+05	2.01E-09	2.22E+06
ED1	-450	36.76	415	536,815		334			1,388,050,560	334	5-RSU LAS	334	96	96	12	4.00E+06	5.36E-09	2.43E+07
ED2	-650	36.76	421.4	553,632		334			1,388,050,560	334	5-RSU LAS	334	96	96	12	3.97E+06	5.32E-09	2.41E+07
ED3	-850	40.0614	421.4	552,835		334			1,388,050,560	334	5-RSU LAS	334	96	96	12	3.74E+06	5.01E-09	2.27E+07
ED4	-1050	46.3529	421.4	551,127		334			1,388,050,560	334	5-RSU LAS	334	96	96	12	3.35E+06	4.49E-09	2.03E+07
h-endcap																		
Disk index																		
HD0	250	36.76	240	176,710		96			339,116,544	96	5-RSU LAS	96	26	26	4	3.92E+06	2.15E-08	2.38E+07
HD1	450	36.76	415	536,815		334			1,388,050,560	334	5-RSU LAS	334	96	96	12	4.45E+06	5.96E-09	2.70E+07
HD2	700	38.52	421.4	553,216		334			1,388,050,560	334	5-RSU LAS	334	96	96	12	4.48E+06	6.00E-09	2.72E+07
HD3	1000	53.43	421.4	548,909		334			1,388,050,560	334	5-RSU LAS	334	96	96	12	3.83E+06	5.13E-09	2.32E+07
HD4	1350	70.14	421.4	542,422		334			1,388,050,560	334	5-RSU LAS	334	96	96	12	3.25E+06	4.36E-09	1.97E+07
TOTAL				**8,161,315**					**19,296,396,288**	**4448**		**4976**		**1348**	**187**	**4.79E+07**	**hits/s**	**2.90E+08**
																5.71	**Gbps**	**34.61**
									# of segments:	4500								
									# of SC links down	22500								
									# of SC links up	9000								

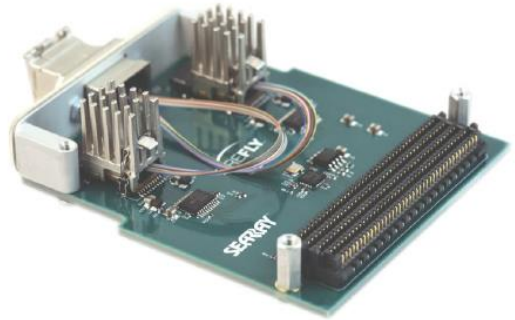
MOSAIX Hardware Mockup



VTRx+ connected to FMC HPC (8 MGT available), emulate typical packets

Aggregator Board Prototyping





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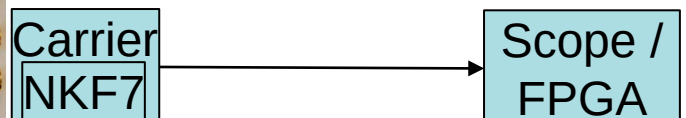
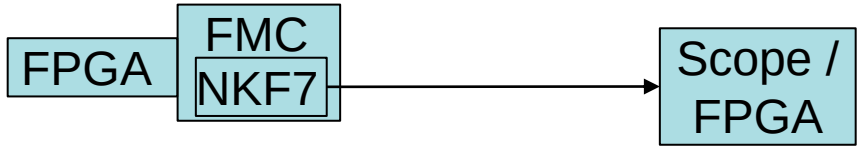
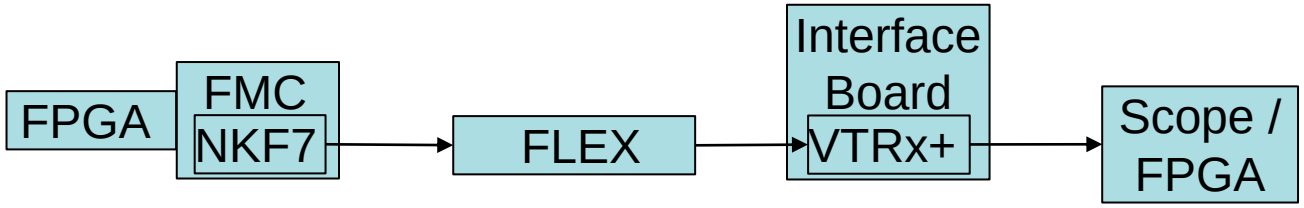
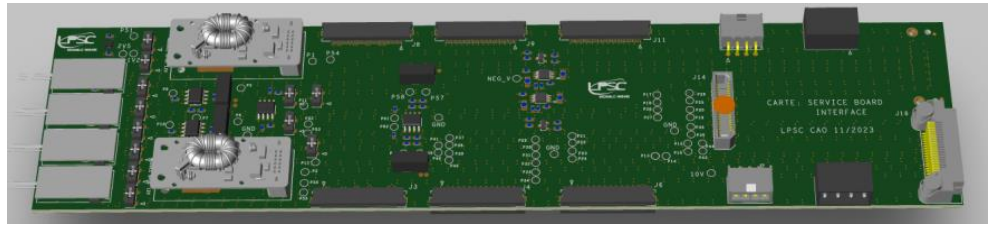
NKF7 Serializer Test Steps

- Characterize NKF7 with fixed 16-bit pattern
  - Scope eye-pattern
  - FPGA BER test
  - Radiation test with Prague 32 MeV protons
- Characterize NKF7 with variable pattern
- Characterize NKF7 + Flex (design by Antoine)
  - Scope eye-pattern
  - FPGA BER test & statistical eye
- Characterize NKF7 + Flex + VTRx+ Transceiver
  - Scope eye-pattern (optical probe or after minipods on CRU)
  - Receiver (minipod / FPGA / CRU) BER test







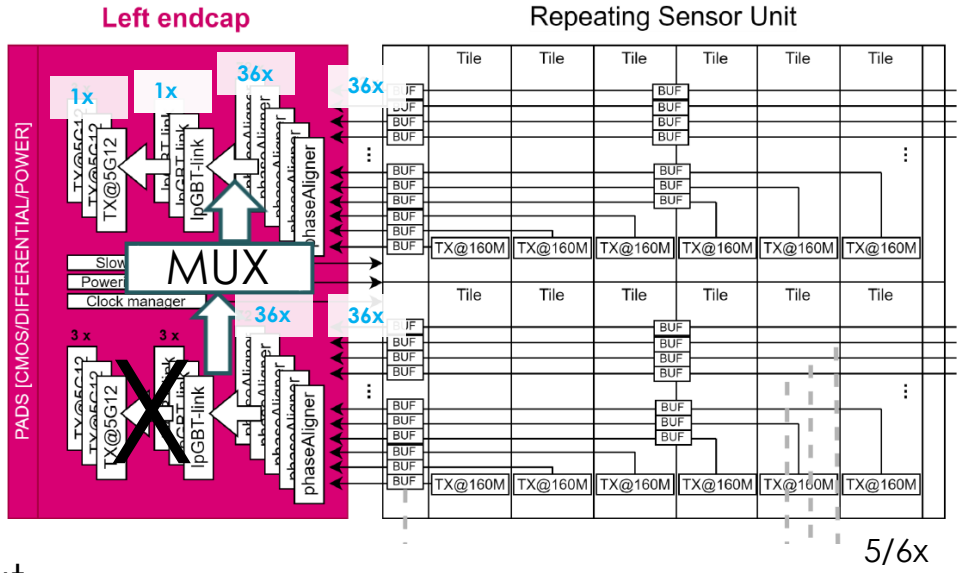


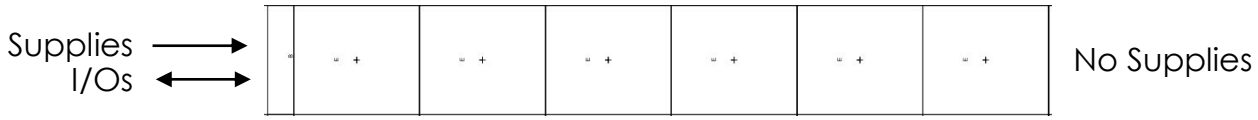
Backup

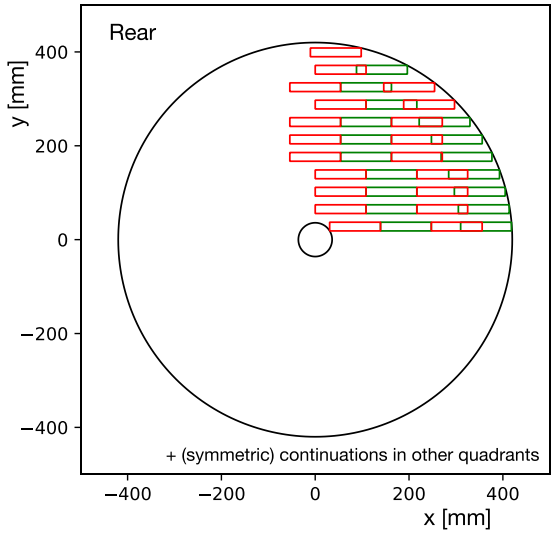
ePIC SVT: "Large Area Sensor" (LAS)

- **Inner Barrel** (Layers 0,1,2) will reuse ITS3-like sensors as is
  - **Layer 0:** 4 sensors in r-phi, 3 segments of 12 RSU
  - **Layer 1:** 4 sensors in r-phi, 4 segments of 12 RSU
  - **Layer 2:** 8 sensors in r-phi, 5 segments of 12 RSU
- EIC **variant** for the **Outer Barrel** (Layers 3,4) and **Endcap Disks**
  - "Large Area Sensor" (LAS)
  - Will be stitched, but not to wafer scale
  - Likely 1 Segment of 5 or 6 RSU (no need for right endcap)
  - The intention is to multiplex Tile data lines to **1** High-Speed output
  - More conventional carbon composite mechanical support with integrated cooling

6-RSU LAS







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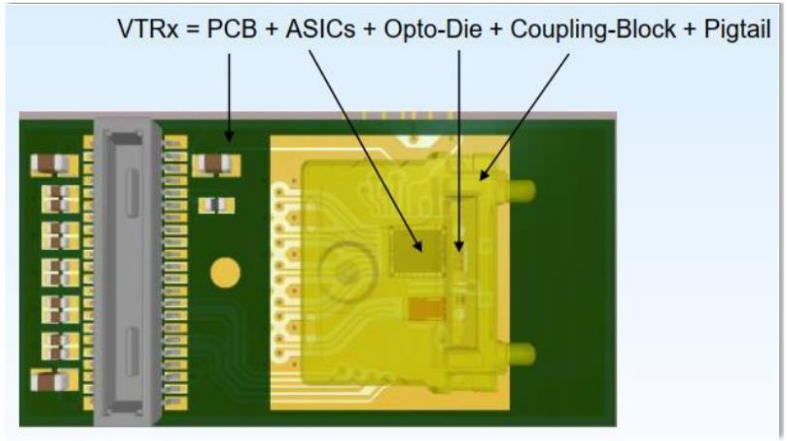
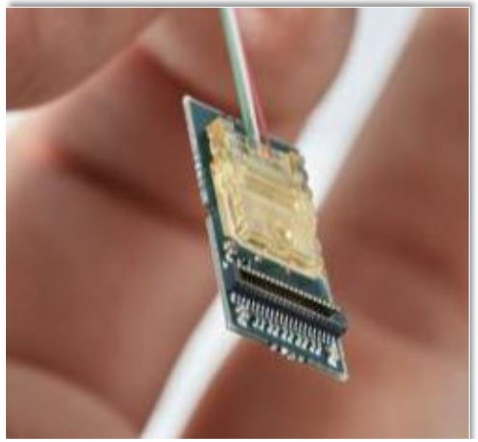
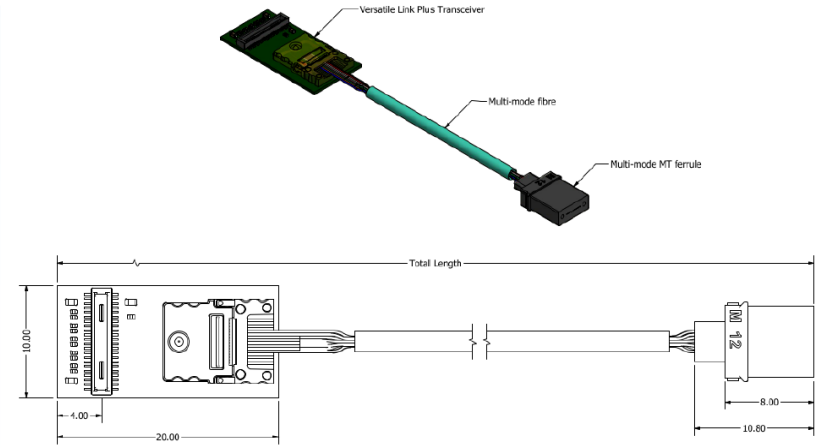
VTRx+ Front-end Module

- **Versatile**
  - Up to 4 Tx + 1 Rx, configurable by masking channels
- **Miniaturised**
  - 20 x 10 x 2.5 mm
- **Pluggable**
  - Electrical connector
- **Data-rate**
  - Tx: up to 4×10 Gb/s, Rx: 2.5 Gb/s
- **Environment**
  - Temperature: -35 to + 60 °C
  - Total Dose: 100 Mrad
  - Total Fluence: $1x10^{15}$ n/cm^2 and $1x10^{15}$ hadrons/cm^2
- **Status**
  - Pre-production ongoing
  - Solving problems with module assembly
    - Alignment of optical components
  - Ramping up to 2k modules/month in 2023







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Remark on timing

Projections for timing resolution

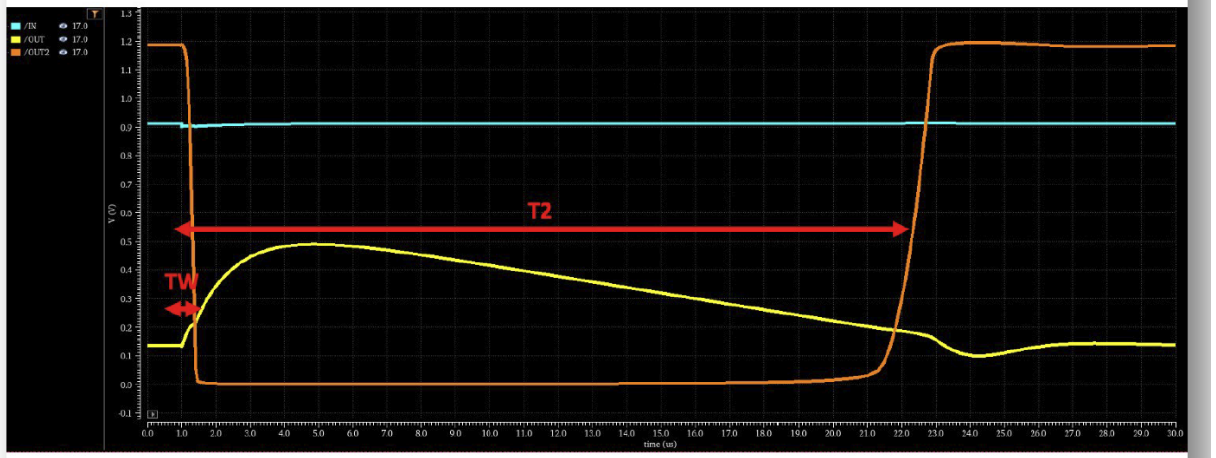
Targeting figures similar to ALPIDE

- Continuous mode readout
- Integration period: 5 / 10 / 20 us
- Frame rate: 200 / 100 / 50 kHz

Low power constrains response speed

- MOSS pulse duration 40 us @ 1 ke
- MOSS time walk ~3.3 us
- Reviewing timing specs for next design

Discriminator time window (MOSS, nominal bias for low power)



Discriminator time window