OAK RIDGE National Laboratory

RDO thoughts, plans

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Tonko's slide I

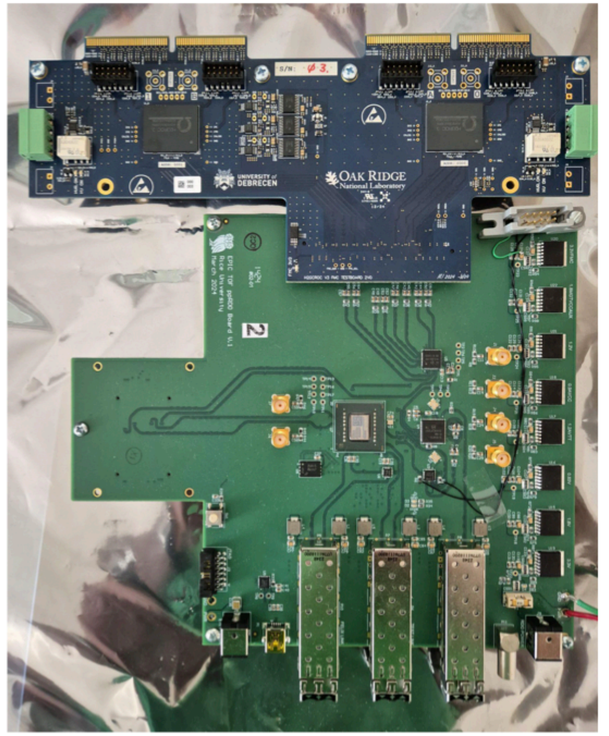
Project Definition & Goals

- ppRDO is a pre-prototype EPIC DAQ Readout Board (RDO)
  - sub-project under FY24 eRD109
  - NB: "pre-prototype" means that it is developed before detector specific prototype RDOs → generalized
- Goals
  - design and produce a prototype board with all the elements which are expected to be common to most/many EPIC detector's Readout Boards
    - **Xilinx Artix+ FPGA** (modern, cheap, CERN TClink compatible)
    - **SFP+ fiber optics interface** (standardized, ~10 Gbs)
    - **Clock cleaner PLLs** → *jitter goal: 5ps for timing detectors* (TOF, HRPPD, Roman Pots, etc)
    - **Clock recovery mechanism using the RX of the SFP ala CERN's TClink** ("Option A") [William's presentation]
      - but additionally establish Option B: direct clock transmission over a dedicated fiber
  - detailed measurement of (all sources of) clock jitter using the above schemes [William's presentation]
  - detailed measurement of power for all voltages used
    - remember: we need 5 different voltages!
  - reasonably accurate cost estimate
  - provide hardware interfaces to EPIC's ASIC prototype boards for testing (FMC connector)
  - firmware
    - establish procedures to readout most/many EPIC ASICs
    - develop common streaming readout scheme in concert with DAQ Group's protocols
  - radiation testing
    - provide framework (and test FW) for SEU upset handling & measurement
    - potential use of entire board for irradiation measurements

Tonko's slide II.

Current Status

- we produced 6 boards – all working after minor fixes [Mike]
- fiber & clock recovery in progress [William]
- general firmware in progress [TL]
  - PLL I2C setup, ADC readout of various monitored voltages, temperature etc.
  - TBD: remote PROM programming and readback
- readout of CMS ETL ETROC ASIC in progress [Mike, TL]
  - I2C working, basic "fast command" interface working, basic data readout working
  - goal is to make sure we know how to readout the data into the FPGA, align it on word boundary, check data coherence with CRC etc and do this at rather high rates of ~1280 Mbs
- readout of H2GCROC ASIC via their test board in progress [TL, Norbert, Miklos] ⇒
  - board recently obtained from the EPIC Calorimeter group (Norbert et al)
  - Miklos et al provided low level readout firmware & general expertise
  - BTW, we expect these specific interfaces to be ~similar to the future EICROC2 & CALOROC which is why it's of interest now
- DAQ readout firmware, in progress [TL]
  - plan is a full 32x ASIC readout scheme where the ASICs will be emulated in VHDL
  - this will enable us to design & vet DAQ Group's fiber protocols
  - and will be used as "test firmware" to
    - a) measure SEUs
    - b) provide schemes and algorithms to handle SEUs
  - the final output of the full emulation is a set of files which contain data very close to what our streaming DAQ will deliver → can be used by software groups



RDO ideas, power, etc

We plan this will be a future development:

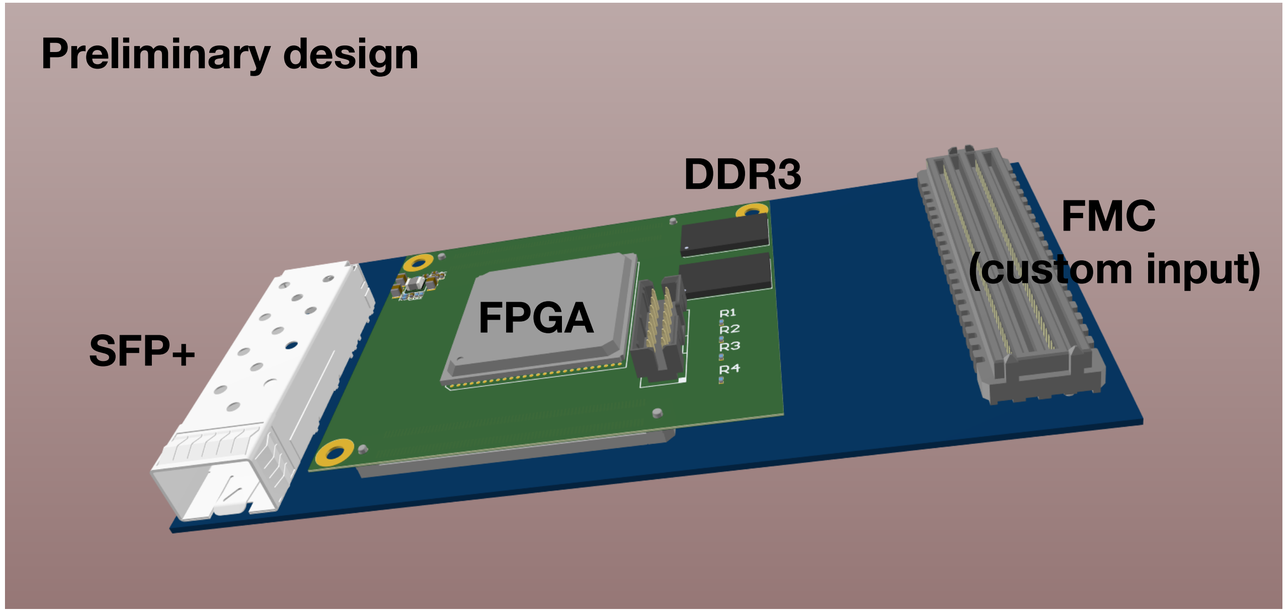
- Design a versatile RDO board to with flexibility to use different FPGA for different detectors
- Easy exchange of FPGA on the board within the same packaging
- Compact design

FPGA choices, power and # ASIC

	Reduce the common Memories 126 >> 64 and 6BRAM/ASIC				
	FPGA	Nr. Of BRAM	SUM (W)75%	Max. Nr. Of ASIC	USD
Basic Artix Ultrascale+	XCAU10P-2FFVB676E	100	4.1	4	277
	XCAU15P-2FFVB676E	144	5.7	12	347
	XCAU20P-2FFVB676E	200	7.4	20	499
	XCAU25P-2FFVB676E	300	10.4	32	596
Kintex Ultrascale+ (more powerful)	XCKU3P-2FFVB676E	360	?	48	2 198
	XCKU5P-2FFVA676E	480	?	64	2 922
Kintex Ultrascale (What we use now, reference only)	KCU 040 FPGA	600	10	64	-

Baseline

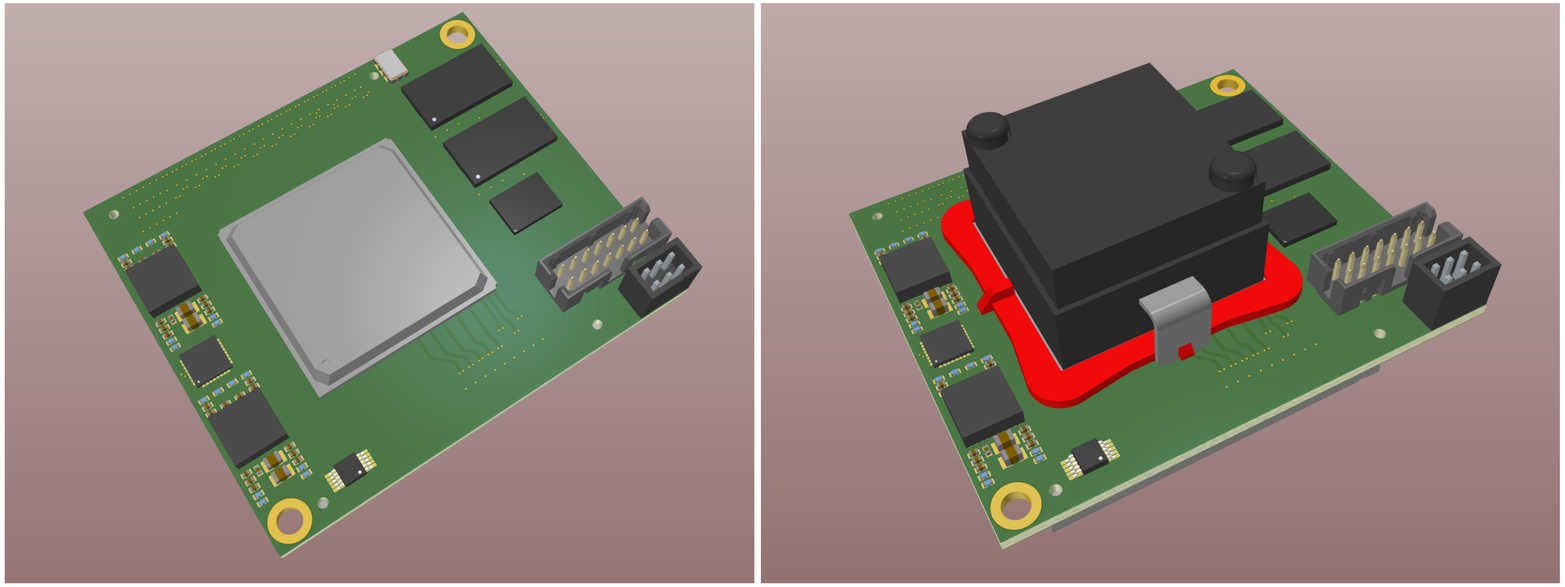
Same footprint, we can use any of these FPGA on the board



All RDO's would look the same:

- Choose the XCAU20P Artix Ultrascale+ as a baseline for now:
  - All of the above chips has the same footprint, they are interchangeable on the board - if one needs more ASIC/RDO ratio or more computing power
  - Daughter card
- Should be applicable on other detectors also
  - Front FMC connector can be changed as needed

RDO daughter card



Daughter card will be flexible and re-placable:

- Highly versatile design
- Can accommodate different detector needs/different readout needs:
  - This can vary as rapidity changes etc.
- Cooling can be air for the first prototypes
- Power needs are all on the daughter card
- Memory will help with buffering:
  - Can save some high-occupancy data - for safety
- 56x64 mm large:
  - This is not optimized, just initial design

Starting of a PED request

Building on the effort started by Tonko et al:

- Starting a development of a versatile, interchangeable readout board
  - Daughter card with the FPGA and memory
    - All services will be present on it
    - 6 different FPGA compatibility from the Ultrascale+ family
  - Base card:
    - Input connectors:
      - Highly detector specific
    - Output:
      - SFP+ connector with fiber compatibility (can be also ethernet)

PED request is in progress of writing. This might also help other detectors if they need a readout board