Electronics developments for the GEM-μRWELL Endcap Tracker

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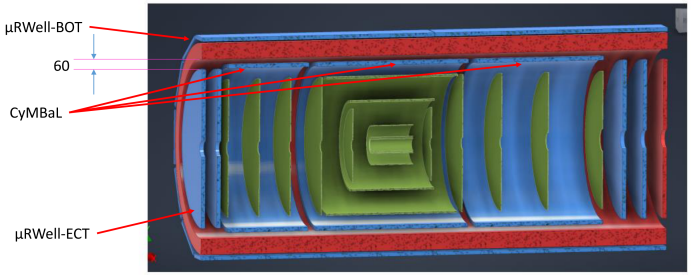
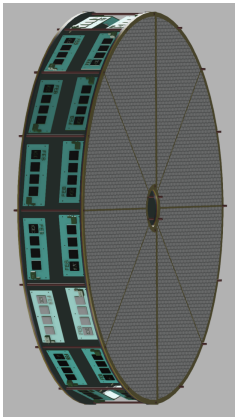
Introduction to MPGDs electronic developments

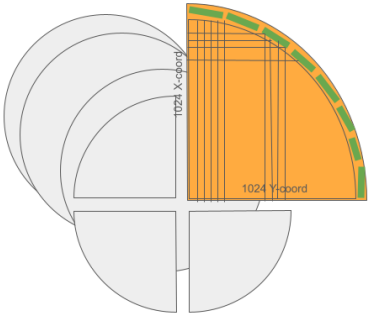


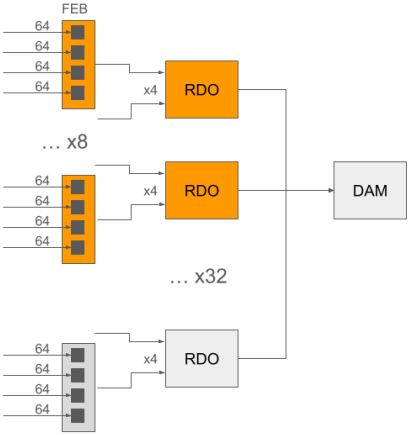
- EndCap Tracker shares common electronics and data acquisition approach with other MPGDs detectors:
  - development of various levels of electronics:
    - FE ASIC developed by Saclay group
    - RDO board developed by eRD109 group
  - solutions for power distribution and dissipation
  - strategy on cable media type and lenght and electronics placement
- Several topics now on discussion
- INFN (RM Tor Vergata and Genova) personnel started connection in the last weeks with people already involved

EndCap Tracker Figures

- 4 disks each composed of 4 quadrants
- Each quadrant has 1024 X-strip and 1024 Y-strip (2048 channels)
- Assuming FE ASIC is 64 channels, grouped in 4 chips FEB, 4 to 1 connection FEB-RDO
- Each quadrant will need 32 ASICs, 8 FEBs, 2 RDOs
- Total amount for ECT is 32k Channels, 512 ASICs, 128 FEBs, 32 RDOs

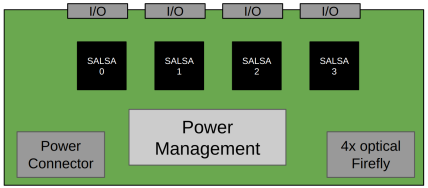


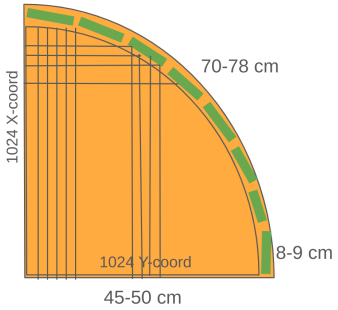


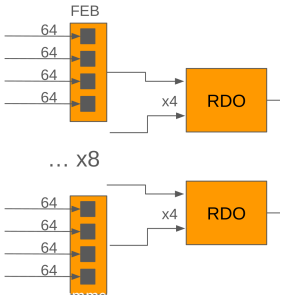


Initial Activities

- Work started in order to understand:
  - Development of custom FE board
  - Possible development of custom RDO board
- First issues arising:
  - FE board length should be within 9 cm
  - how much is width constraint?
  - (x,y) computation should be performed at RDO level, this a single RDO should receive data from an entire quadrant

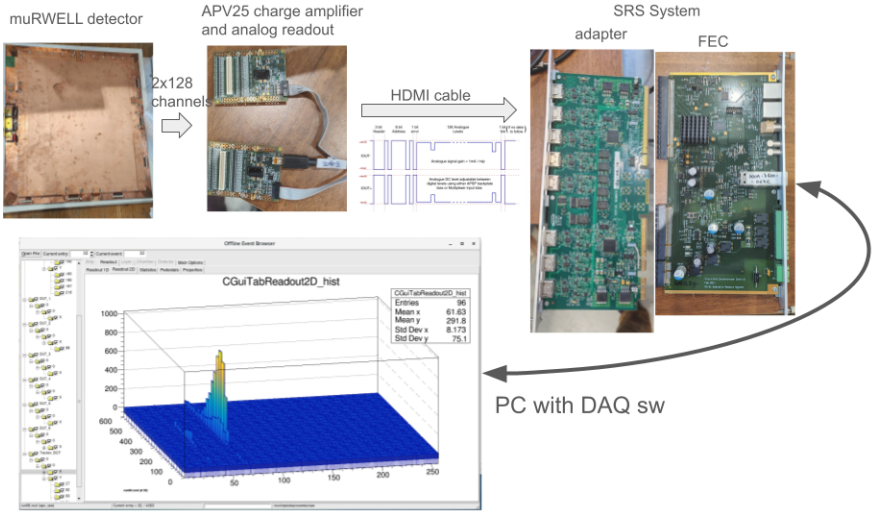






Actual Experimental Setup

Our Setup in LNF for preliminary development of μRWELL detector

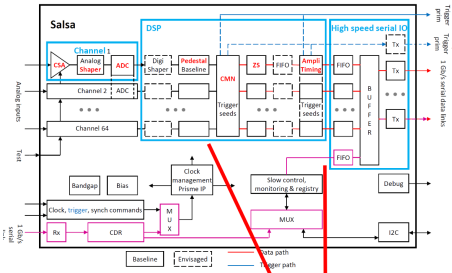


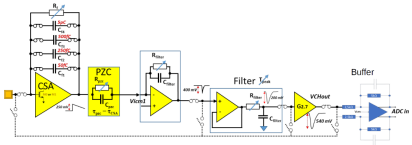
Collected second-hand material from 2012, but working up to 256 channels

FE Emulation preliminary ideas

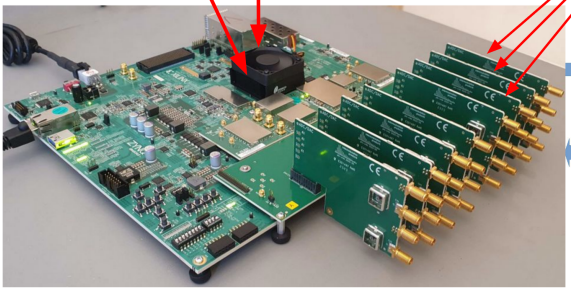
- SALSA chip could be available in late 2026 for first integration in Front-End boards
- interfacing with detector could happen even later
- Saclay group has already though to emulate (part of) SALSA logic on low-cost FPGAs, to perform design verification
- one can think of extending this activity in order to connect the detector to a multi-channel, high sampling rate integrated ADCs FPGAs (ZCU216 board)
- there is some glue logic needed (charge amplifier) we can think to develop in very short time eventually in a simplified version
- having a single box with 16 channel readout complete with charge amplifier, ADC, SALSA ASIC logic and instrumented readout through the on-chip Processing System can be a good solution to both test the detector in development and test the SALSA ASIC features directly on real detector data.

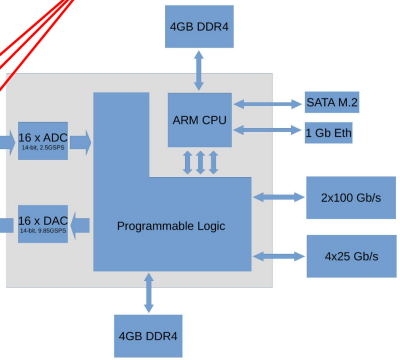
Just a pictorial idea





Scheme from P. Baron



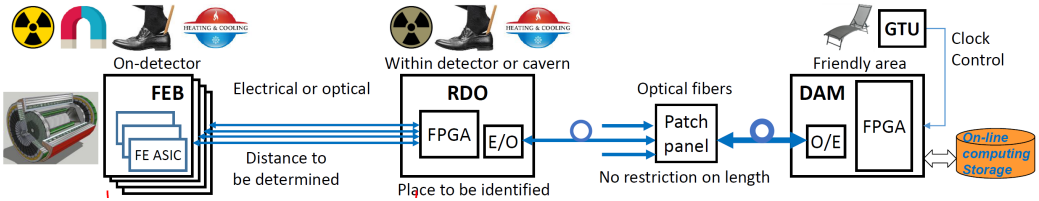


Backup slides

Experiment requirements for MPGD Detectors

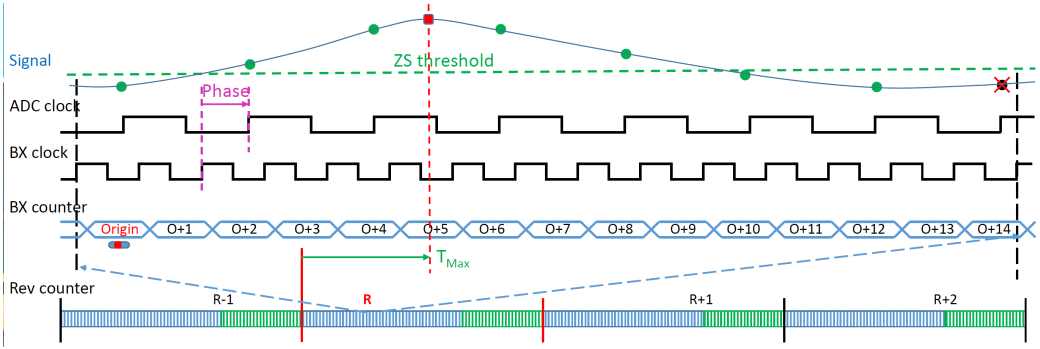
- Typical signal 1-1.5 keV resulting to 15-30 fC per channel
- Aimed dynamic range of 10 bits: Signal / noise of 60 dB
- Timing precision of O(10ns)
- Channel occupancy of $\sim$10 kHz: Including factor 5 of safety margin
- Streaming readout With support of in situ calibration and of on demand readout
- 1.8 T magnetic field
- Mild radiation environment
  - TID and neutron fluence after 10 years: 10 krad and $10^{11} n_{eq}/cm^2$
  - 20 MeV proton flux: 100 particle/cm^2/s
- Stringent space for detector readout and services

General Readout Organization



- FEB frontend board with readout ASICs → detector specific, common design among MPGDs detectors, different form factor
- RDO readout module first stage of FEB data aggregation, last stage to dispatch clock & control → Mostly common design framework between sub detectors, different form factor
- DAM data aggregation module interface with computing and global timing and control unit (GTU) → Common design for all sub detectors
- Downstream towards detector: clock, control, monitoring
- Upstream towards storage: physics, calibration, monitoring data

Readout Strategies for MPGDs



- Signal is continuously sampled with an ADC
- Signal samples above threshold are retained
- Nominal (physics data) readout: signal amplitude and timing is derived → Time of max (as on example) or time of arrival (fitting samples on rising edge)
- On demand readout: signal shapes or raw non ZS data are provided → Calibration, detector studies
- Guarantees best noise immunity and thus best S/N ratio → Allows on line common mode noise (CMN) subtraction before ZS

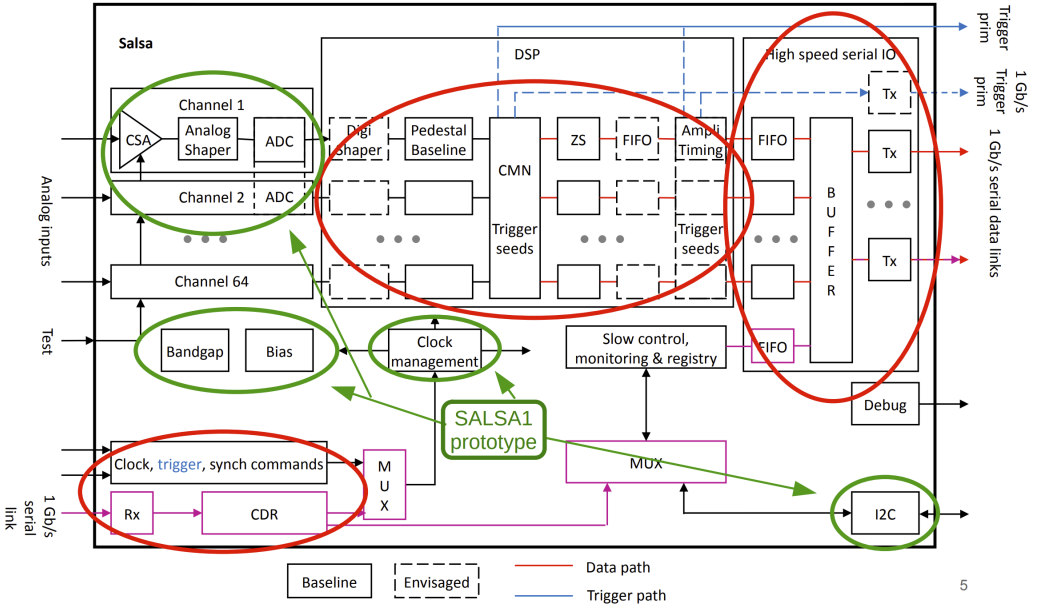
EndCap Tracker Data Bandwidth Estimations

- Physics Data: support two zero suppression modes
  - Nominal: peak finding readout $\rightarrow$ 12 bit amplitude, 12 bit time of max, 8 bit ToT
  - On demand: full signal shape readout $\rightarrow$ All samples (12 bit) above threshold (typically 15-25 samples)
- Estimated Physics data bandwidth per Salsa ASIC with channel rate 10 kHz:
  - Peak finding 40 Mbit/s
  - Signal shape 265 Mbit/s
- On line calibration: on demand readout
  - Programmable number of non ZS samples
  - Estimated calibration data bandwidth per ASIC $\sim$ 6 Mbit/s
- FEB RDO link occupancy: $\sim$30 % of one 1 Gbit link
- Overall physics frontend data of ECT:
  - $\sim$ 130 Gbit/s for on demand mode
  - $\sim$ 37 Gbit/s for nominal mode

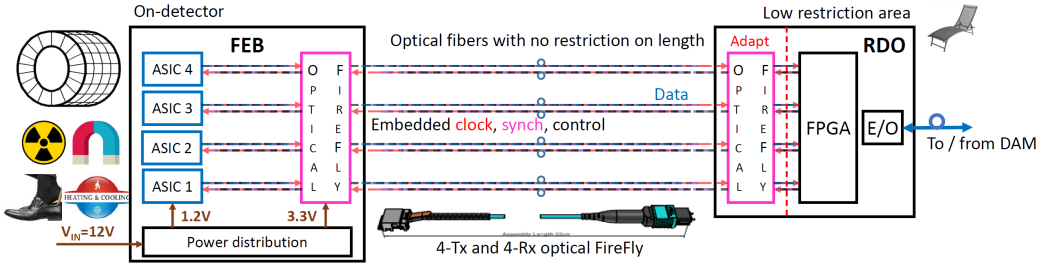
SALSA ASIC Characteristics

- Versatile front-end characteristics
  - Dedicated to MPGD detectors and beyond
  - 64 channels
  - Large range of peaking times: 50-500 ns
  - Large choice of gain ranges: 0-50, 0-250, 0-500 fC or 0-5 pC
  - Large range of input rates, up to 100 kHz/ch with fast CSA reset (limit assumed for EPIC: 25 kHz/ch)
  - Front-end elements can be by-passed
- Digital stage
  - Fast sampling ADC for each channel on 12 bits (¿ 10 effective bits) at up to 50 MS/s
  - Possibility under study to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction, treatment processes to be selected according to user needs
  - Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
  - Several 1 Gb/s output data links (will use one)
- General characteristics
  - $\sim$1 cm^2 die size, implemented on modern TSMC 65nm technology
  - Low power consumption 15 mW/channel at 1.2V
  - Radiation hardened (SEU, TID)

SALSA ASIC Characteristics

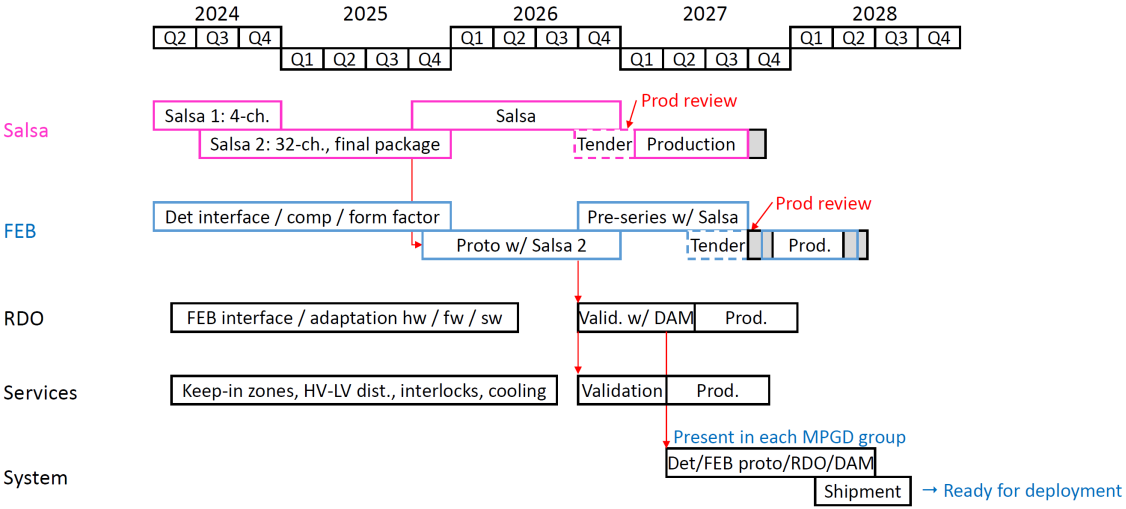


Aimed FEB Design



- ASICs directly connected to 4 lane bidirectional parallel optic FireFly transceivers from Samtec
  - Single 1 Gbit /s Rx line encoding clock, sync run control and asynchronous slow control and monitoring commands
  - Single 1 Gbit /s Tx line for physics, calibration, control and monitoring data
- Low active component count
  - Easier to adapt to challenging on detector environment
  - Samtec FireFly: reported to stand TID of 50-100 krad and neutron fluence of at least $5 \times 10^{11} n_{eq}/cm^2$
- RDO can be placed anywhere in experimental hall with no particular environmental restrictions

developement planning



RDO development via eRD109 (ppRDO)

- Aim is to produce a generalized RDO using the Xilinx Artix Ultrascale+ FPGA
- Used to finalize the timing distribution schemes
- It has an FMC connector and at least one 10gb connection (lpGBT to DAM)
- Allows flexibility with developing custom FMC daugher card for custom interconnections
- ppRDO is in the production stage