Comments on the CERN ASICs for EPIC TOF

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Readout Board (RDO) ASICs & devices

- “Translation” table of CERN ASIC technologies used in the RDOs compared to the current EPIC DAQ baseline:

	CERN	EPIC current baseline
“intelligence”: frontend ASICs data readout	lpGBT ASIC	Xilinx Artix Ultrascale+ FPGA
Frontend ASICs & RDO control (if needed)	GBT-SCA ASIC	subsumed in the FPGA
Optical Transceiver	VTRx+ ASIC with pigtail	SFP+

BTW: why did CERN develop their ASICs? ⇒ Radiation Hardness; which is their main advantage

CERN ASIC Eco-system Disadvantages

1. The CERN ASICs are very specific chips tailored to the CERN high radiation environment
   a. **EPIC doesn't expect such large radiation backgrounds** and we think that commercial components (FPGA & optical transceiver) will be sufficient
      i. e.g. STAR@RHIC uses commercial components and works for a number of years (15+) even in the highest luminosity pp500 or AuAu200
2. CERN ASICs are rigid in their function
   a. think of them as pre-programmed FPGAs that expect exact interfaces which **can't change**
   b. the readout ASICs serial data format needs to meet the e.g. lpGBT e-links format and speed
   c. they offer **no further intelligence** e.g. data reformatting, on-FPGA zero-suppression, or noise suppression
3. CERN ASICs have strong limitations in the clock and data rates
   a. **lpGBT only works at 40 MHz LHC clock *and no other* ⇒ a big problem for 100 MHz EIC!**
   b. downlink rates are fixed at the low 2.5 Gbs
   c. uplink rates are fixed at 10 Gbs
4. CERN ASICs are not commercial chips
   a. purchases need to be orchestrated with CERN
   b. more expensive than commercial products(?)
   c. we buy them from CERN on trust which might be or not be warranted (errata is typically not documented)
      i. support is probably lacking if at all
   d. EPIC board prototyping will be more difficult

VTRx+ vs SFP+ (response to Zhenyu's query to me)

	VTRx+	SFP+	
rad hardness	excellent	meets EPIC requirements? (also based on existing use); can be easily swapped out in a number of years or running if necessary	
power	lower (~200 mW?)	higher (<1 W)	
cost	$150(?)	$20-$50	
size	smaller electronics footprint (20x10x2.5?) but has an additional fiber pigtail	larger (57x14x10); fiber connection via standard LC connectors & fibers	
availability	**seems to need bulk purchase already in 2024!?**	simple purchase at any time in any quantity; many vendors	
fiber rates	only 2.5 Gbs downlink (RX); 10 Gbs uplink (TX)	10 Gbs up- and downlink; can be extended to 28 Gbs with SFP28	
other	4 uplink (TX) fiber drivers for high data volume needs (rarely required in EPIC, if at all?)	1 fiber uplink (TX) but that is more than sufficient for TOF e.g.	

Transceiver Images

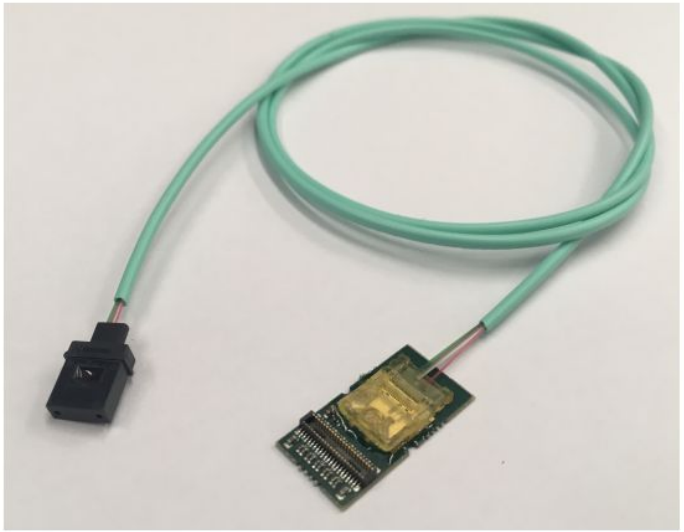

Figure 2: Photo of VTRx+ module showing module, pigtail, and MT connector.

20 x 10 x 2.5 mm electronics circuit
+ pigtail + MT connector

SFP+

57 x 13 x 9 mm
(cage 49 x 14 x 10 mm)

Conclusion

- transceiver: TOF can technologically work with SFP+ or VTRx+
  - TOF should follow general EPIC Electronics & DAQ decisions
- lpGBT: will likely work in TOF in terms of pure readout & control of EICROC *however* I don't see how we can easily solve the 40 MHz clock limitation of lpGBT
  - but again, TOF should follow general EPIC Electronics & DAQ decisions

Today's email from Fernando

We are requesting your input in three areas of the Electronics & DAQ (these are in one file for simplicity):

Qmin/Qmax – this is the minimum signal of interest and the expected maximum signal presented to the FE electronics. This information will supplement the current ASIC specifications and as requested by the designers.

VTRX+ - there is urgency in determining the number of VTRX+ modules needed and in starting the procurement process with CERN. Updated specifications show that the Tx is over 10 Gbps and the Rx is over 5 Gbps.

Development responsibility assignments – As we approach CD-2/CD-3 we need to have institutions/groups committed to developing the various RO chain elements per sub-detector: Adapters, FEBs, RDOs, GTU, DAM. It is understood that we will maximize synergies in these developments, conforming to the ePIC architecture, and that there will be single developments of the GTU and DAM.