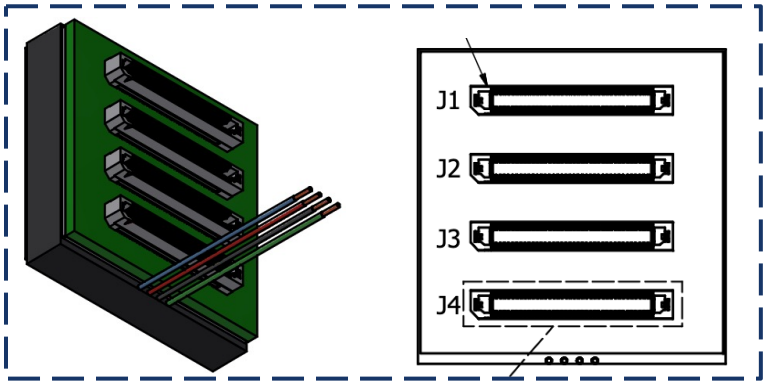
eRD110 FY24 proposal (HRPPDs)

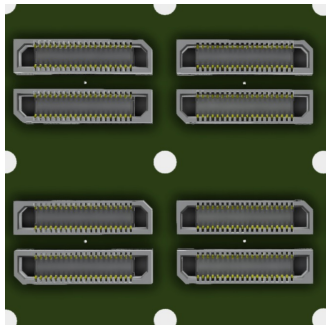
Topic as formulated in V1	V3 (final)	Current status	Prospects
Samtec interposers	Removed (were ordered using FY23 money)		
Passive interface	Moved to Yale PED proposal; partly ordered using FY23 funds	No funding granted for Yale QA station	Order as part of MCP-PMT interfaces
ASIC backplane	Moved to eRD114 (pfRICH)	Defunded	Ask for PED money
B field studies at Argonne	Removed; perform MCP-PMT evaluation instead		Do parasitically with MCP-PMT studies
B field studies at INFN	Removed		Ask for PED funding
Beam test at Fermilab	Reformulated with a focus on hpDIRC application		Need a separate DRS4 backplane?
Ageing studies at INFN	Survived		
QE evaluation at Argonne	Removed, assuming “Yale PED”	No funding	?
PDE evaluation at BNL	Removed, assuming “Yale PED”	No funding	?
Timing upgrade at BNL	Survived		

eRD110 FY24 proposal (MCP-PMTs)

Topic as formulated in V1	V3 (final)	Current status	Prospects
New Photek Auratek	Removed	Ordered by JLab	
New Photonis Planacon	Removed		Try to reanimate the existing one?
Test stand upgrade in Glasgow	Funded in full		
Passive Photek interface	Survived	Being ordered	
Passive Planacon interface	Survived		Needs a bit of a discussion



Auratek stock configuration



HRPPD world

Budget table (v1)

	ANL	INFN	Glasgow	BNL	JLab	USC
B-field maintenance, He consumption	$8.0k					
B-field studies, QE scans (staff effort support)	$18.0k					
B-field studies, QE scans (engineering support)	$15.0k					
B-field studies (travel)		~~$16.0k~~			$4.0k	$4.0k
Consumables for ageing studies		$6.0k				
Postdocs and students		$20.0k				
Beam test travel and freight		$4.0k	$10.0k	$12.0k	$4.0k	
~~Five HRPPD passive integration packages~~				~~$12.0k~~		
~~HRPPD ASIC integration package~~				~~$15.0k~~		
~~Samtec compression interposers~~				~~$16.0k~~		
~~Photek / Photonis MCP-PMT procurement~~						~~$50.0k~~
Photek / Photonis MCP-PMT interface				$4.0k		
Test stand M&S and technical support	~~$2.0k~~		$9.0k	$8.0k		$16.0k
TOTAL	**$43.0k**	**$46.0k**	**$19.0k**	**$67.0k**	**$8.0k**	**$70.0k**

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Budget table (v3)

	ANL	INFN	Glasgow	BNL	JLab	USC
B-field maintenance, He consumption	$8.0k					
B-field studies (staff effort support)	$18.0k					
B-field studies (engineering support)	$15.0k					
B-field studies (travel and freight)				$10.0k	$4.0k	$4.0k
Consumables for ageing studies		$6.0k				
Postdocs and students		$20.0k				
Beam test travel and freight		$4.0k	$10.0k	$12.0k	$4.0k	
Photek / Photonis MCP-PMT interface				$4.0k		
Test stand M&S and technical support			$9.0k	$6.0k		$16.0k
TOTAL	**$41.0k**	**$30.0k**	**$19.0k**	**$32.0k**	**$8.0k**	**$20.0k**

Funded in full as shown

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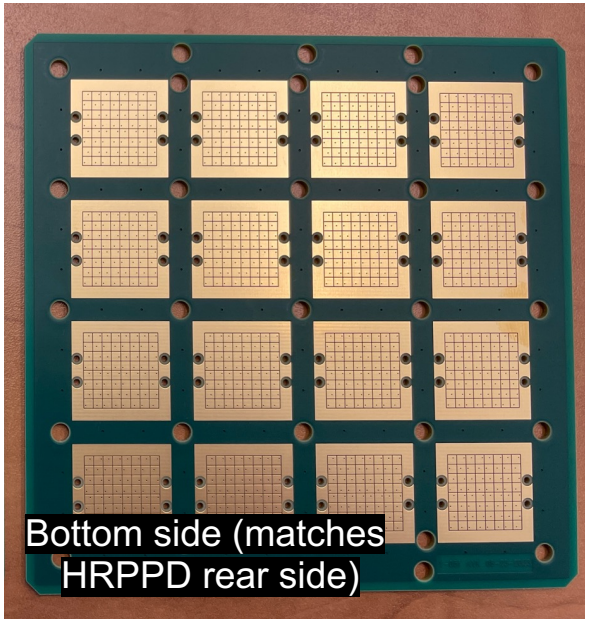
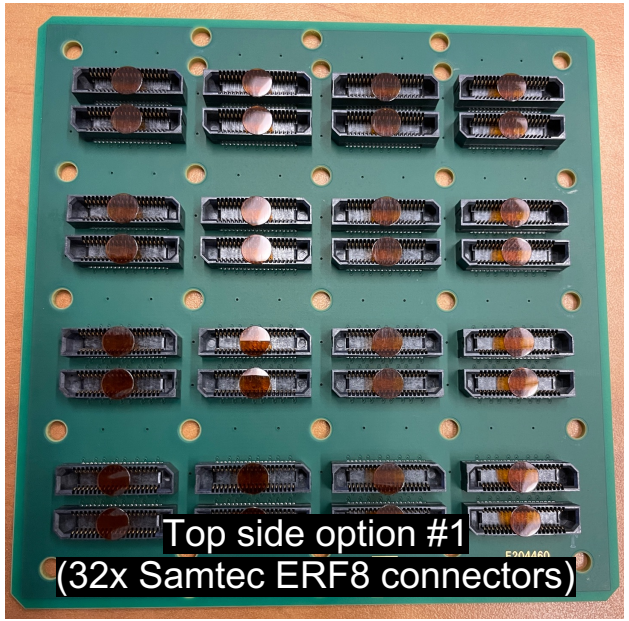
HRPPD order status and expectations

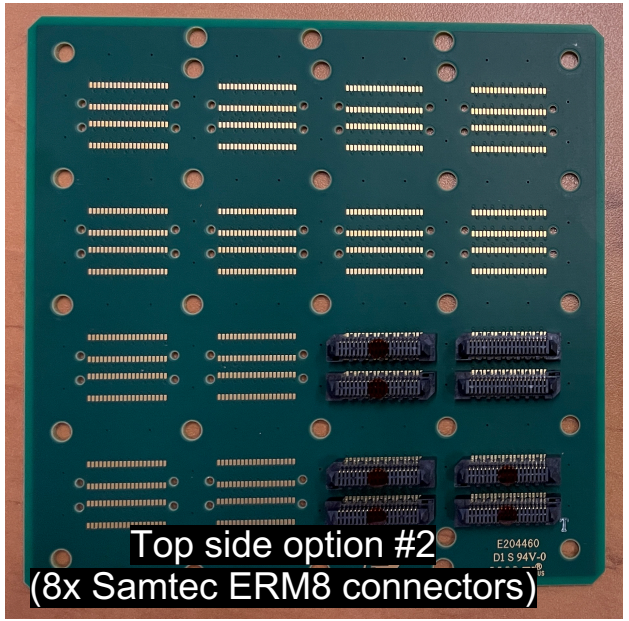
- First five anode base plates are (still) expected from Kyocera on November 15th
- Sapphire windows are not happening in this iteration
- Samtec interposers: the vendor managed to lose both BNL & Incom parts of the PO
  - Production will take ~5 weeks from now
- The five HRPPD production schedule looks like “mid December – mid March”

- QA procedure on our side needs to be discussed / formalized (soon)
- Boundary conditions:
  - No time to ship any of the tiles to Europe and receive them back by pfRICH beam test in May 2024 (?)
    - Any work at INFN & in Glasgow can only start afterwards
  - Realistically, a primary evaluation (in spring 2024) can only happen at BNL (or Jlab? or Yale?)
  - Magnetic field tests at Argonne: summer 2024
  - A YES / NO decision is required to continue any PED activities past first five HRPPD delivery

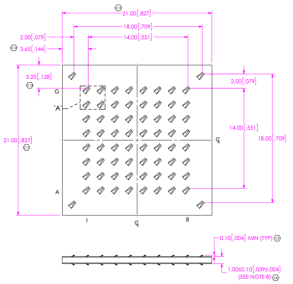
A dummy HRPPD readout board Y05f







Enables ASIC interface to MCP-PMTs

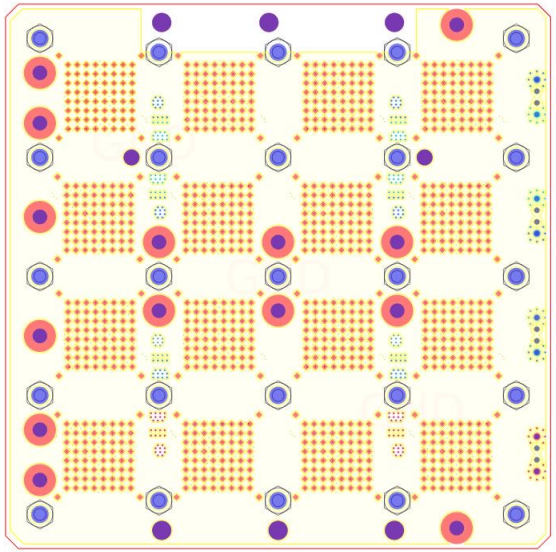


- Got 4 (option #1) + 1 (option #2) sets assembled
- Connectivity for any of the sixteen 8x8 pad fields (PO was not placed yet):
  - A set of [2x Samtec ERM8 -> MMCX] adapters, 32ch (4x8) connected at a time
  - A set of ERM8-based grounding caps for all other 8x8 fields

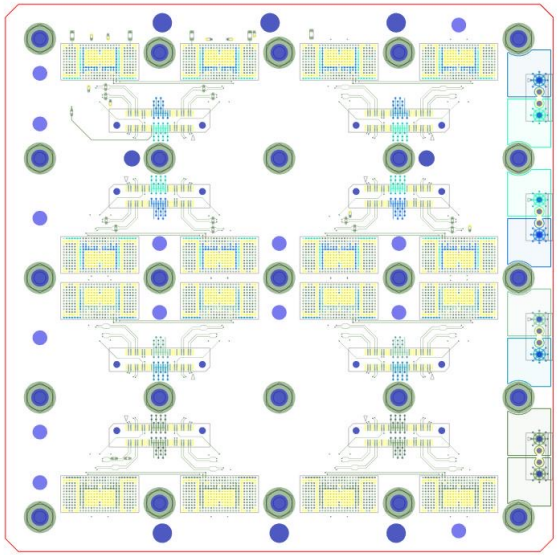
HGCROC3 ASIC / FPGA backplane

IN2P3 (OMEGA), Uni Debrecen, BNL, Oak Ridge

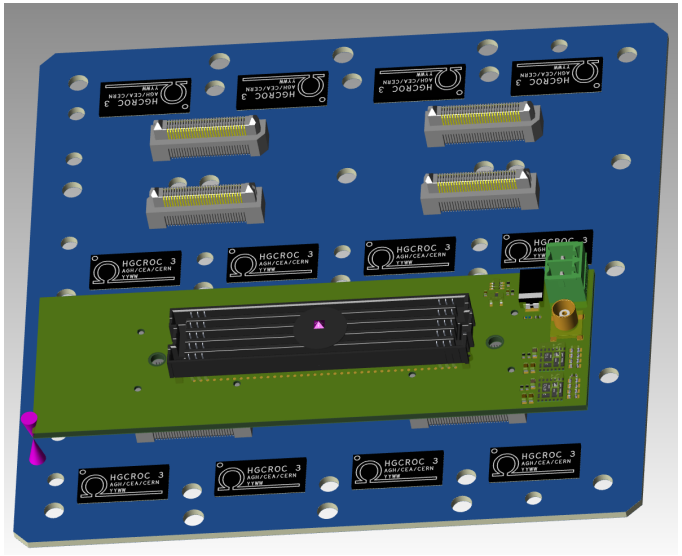
See current version of an interface document here



Bottom (HRPPD) side



Top (ASIC) side



Passive interface to a KCU105 kit

- V0: expect ASIC & passive interface board designs to be finished by November 10
- V0: FPGA board PO will be submitted with a delay of ~2 weeks
- Assume there is still enough time for a second iteration (V1) before May 2024 pfRICH beam test

HGCROC3 ASIC / FPGA backplane schedule