Discrete/COTS waveform readout FEB for backward ECAL

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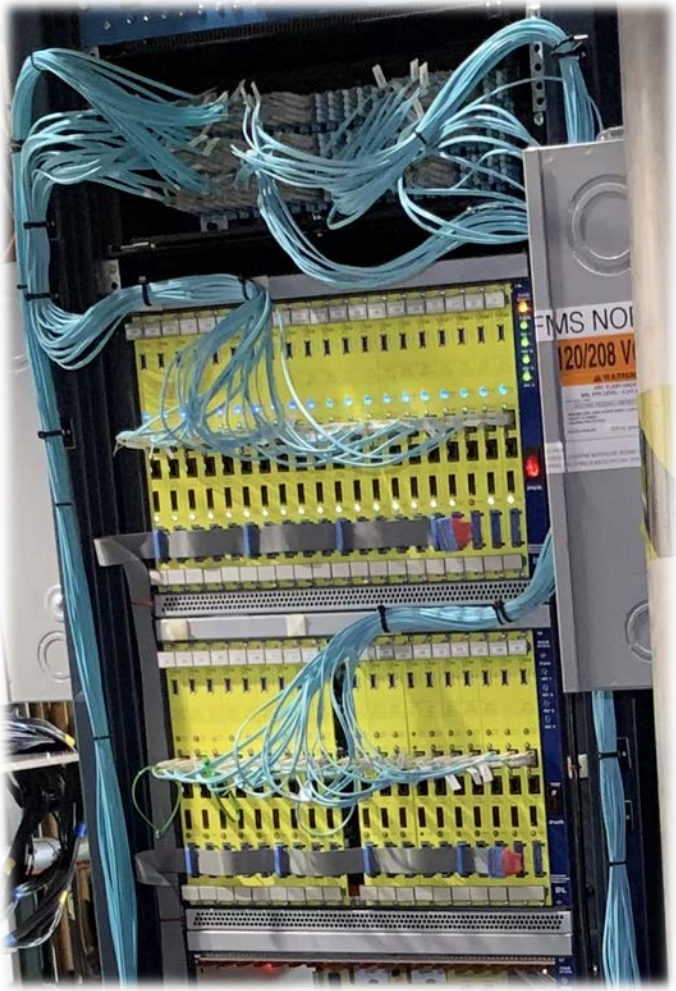


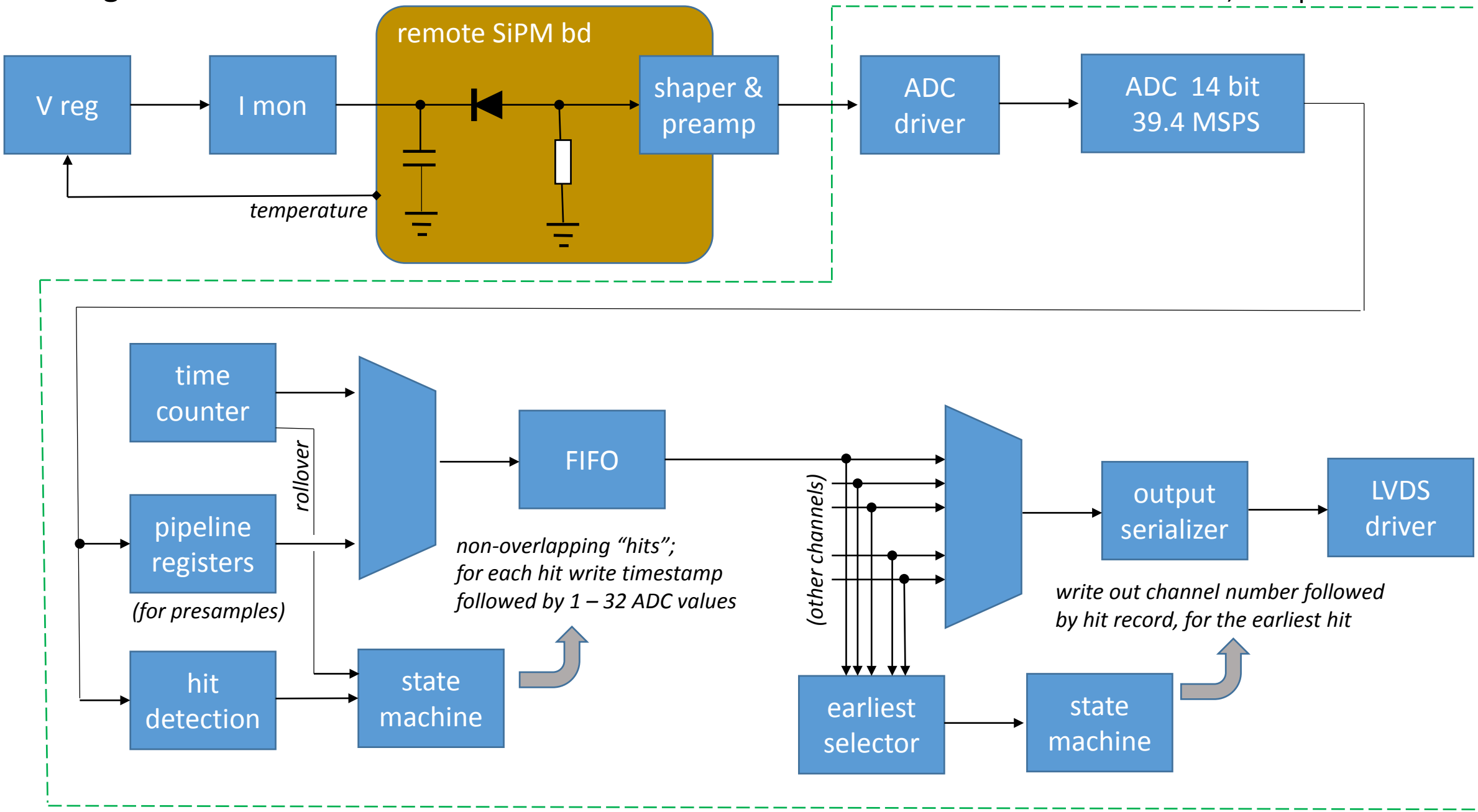
STAR FCS waveform readout (remote preamp/shaper), 32 ch/board

requirements and characteristics – for discussion

see later slide

- 24 channel assembly
- dimensions: < 18 × 12 × 1.5 cm^3
- power: <120 mW/ch (2856 ch: 343 W)
- ADC: 14 bit, 39.4 MSPS (2/5 clock)
- peaking time: 4 – 5 samples
- number of samples taken: 8 (likely; adjustable)
- SiPM: 4× S14160-6010PS (10 nF, gain 1.8 × 10^5, pixel count 1,436,044)
- light yield: 5.5 pixels/MeV (expected, TBC)
- signal range: 5 MeV (threshold) to 20 GeV
  [1.6 pC to 6.3 nC @ highest gain]
- SiPM DCR (after irrad.): TBD
- dark counts in pulse: TBD (roughly peaking × DCR)
- linearity (electronics only): 0.1%
- rate capability: **TBD** (50 kHz/ch ?)
- timestamp size: 24 bit (340 ms rollover)
- rollovers marked in datastream
- total hit data size: 144 bits (or less, w/ feature extraction, perhaps)
- max output (to RDO) data rate: (40 MB/s? TBD)
- data cable: Cat6 or similar, < 25 m
- SiPM bias control: per channel DAC, 33 – 47 V range, <10 mV stability, low noise <1 mV, *fast recovery*
- SiPM bias compensation: per channel thermistor, common slope DAC
- SiPM bias current monitor
- SiPM – FEB cable length: **≤ 60 cm** TBD, micro-coax
- input supply monitor
- on-board LV DC/DC, 10 – 13 VDC input

Block diagram

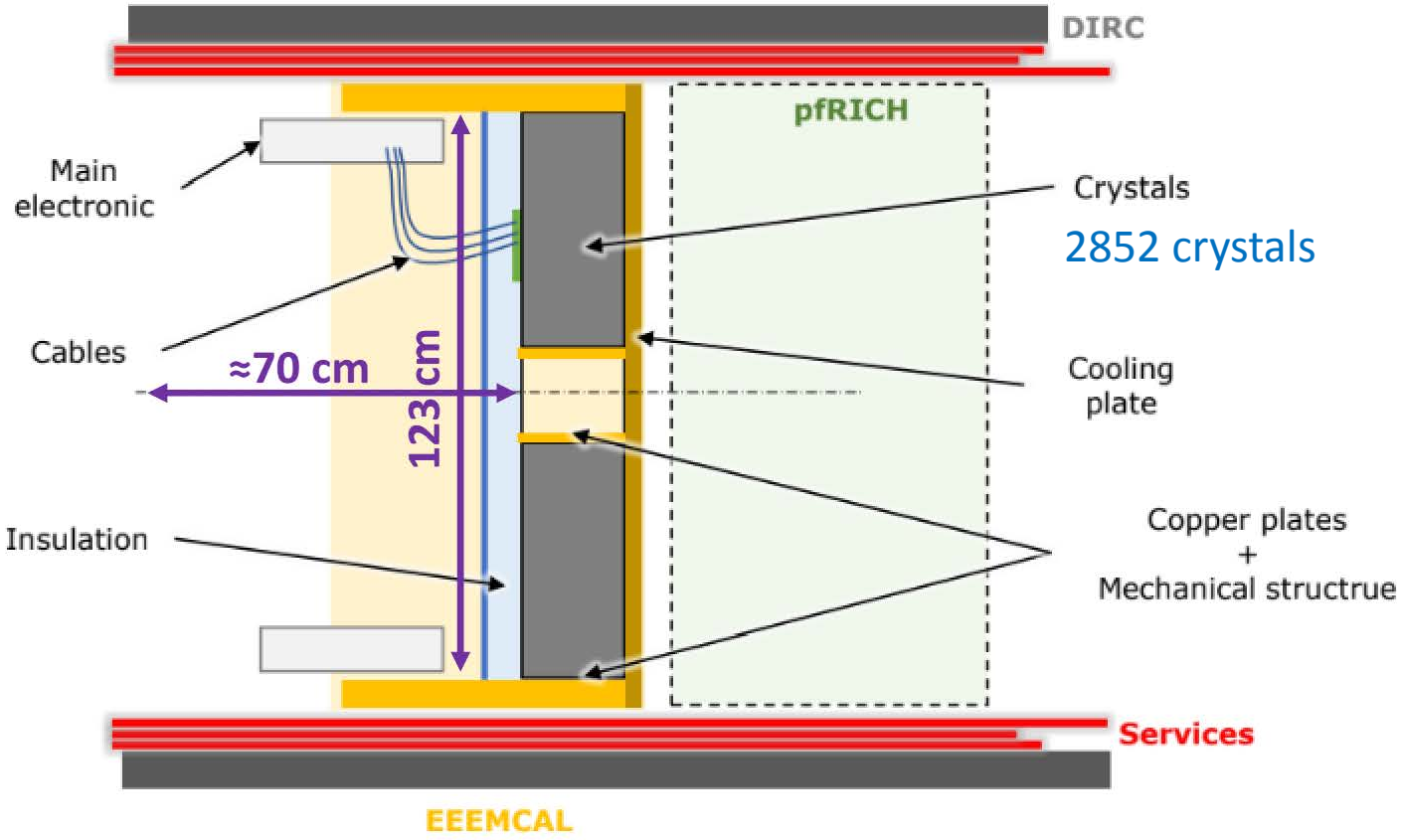


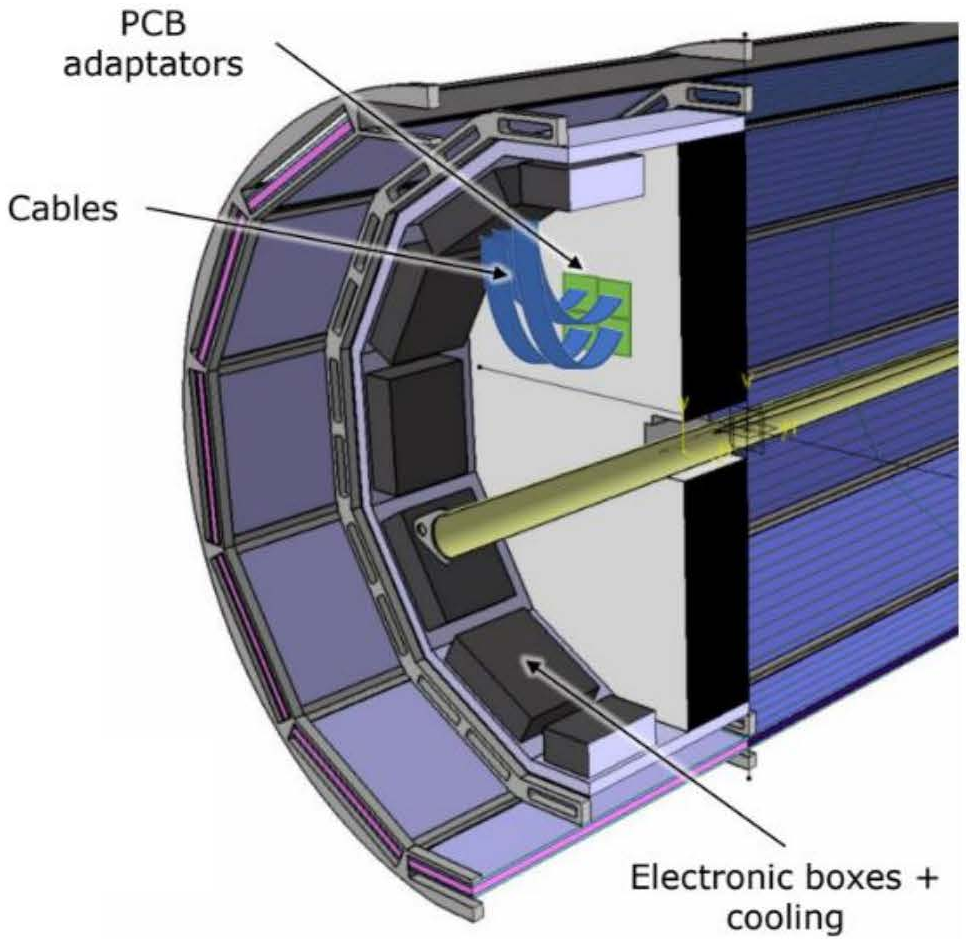
(borrowed slide, slightly trimmed)

EEEMCAL front-end electronics and cooling

There is enough integration space for this electronics.

It will be good to keep most electronics to the periphery, as planned/shown, to minimize radiation damage and to ease cabling.





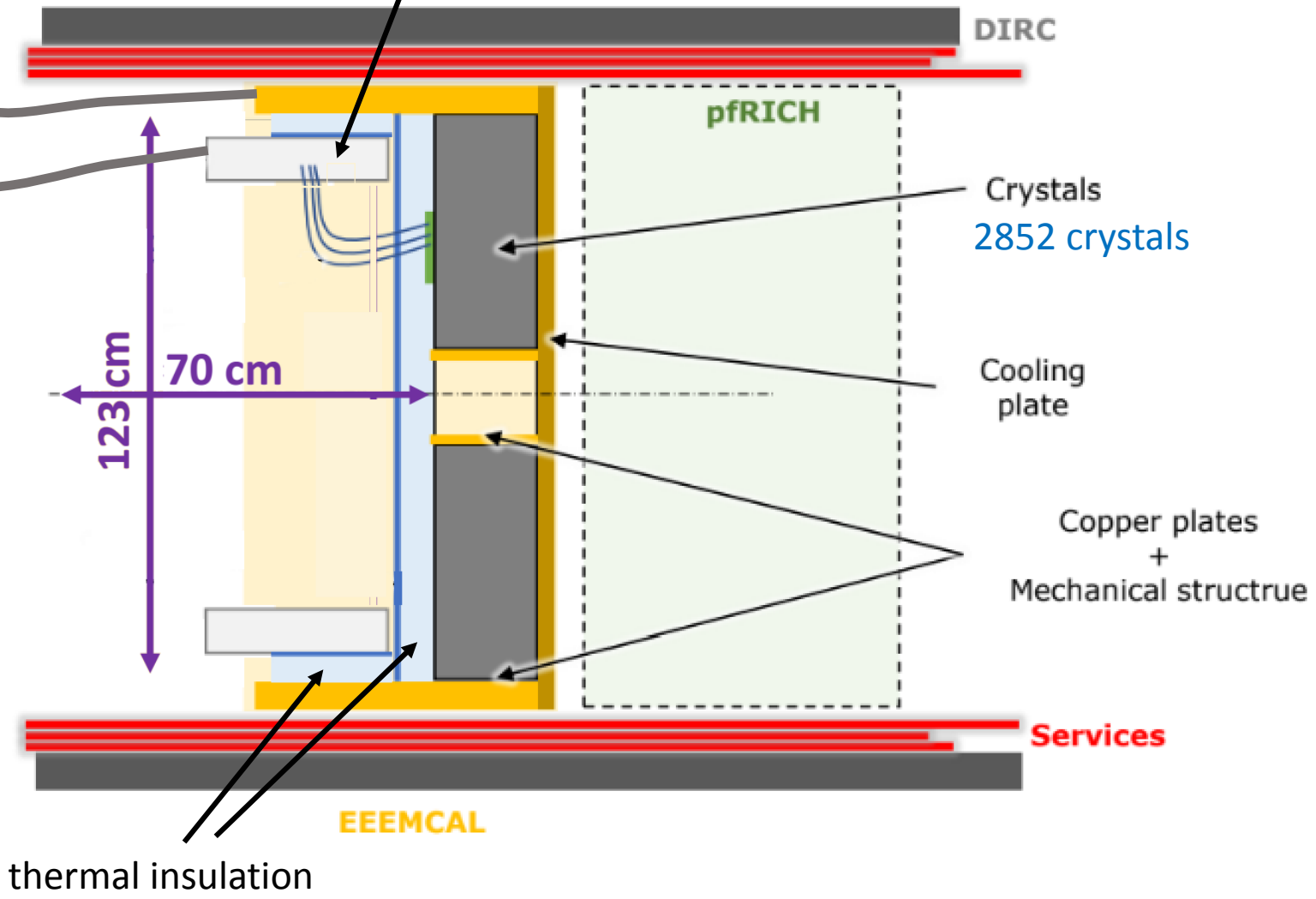
12 electronics assemblies

FEB mechanical & cooling

T control (cooling)
liquid for crystal array

12 × FEB assy, 9 – 10 FEB each (119 FEB total, 2856 ch)
18 × 12 cm in this view (excluding coldplate)

liquid cooling for FEB assy
6 loops, 2 assy in series
57 W per loop



- Thermal insulation *all around* between FEB and crystal support & thermal structure
- **Separate** liquid temperature control loops for crystals & FEB's
- Preamp power on SiPM board should be mimized
  - maybe 0 ?
- But, radiation damaged SiPM's will dissipate some heat:
  - e.g. 98 W @ 200 µA / SiPM…

Further remarks

The preamplifier could either be on the SiPM board or on the FEB. We have to think about this…

- Preamp on SiPM board may be hard to fit. Some shaping is needed before the preamp, IMHO, for linearity concerns.
- With careful design, I think performance can be just as good with the preamp a modest 60 cm distance away. (Using good cable!)
- Preamp power is low (perhaps 5 mW/ch), but of course preferable to avoid that heat on SiPM board
- BUT, radiation damaged SiPM's may be a much more significant heat source (perhaps 35 mW/ch)

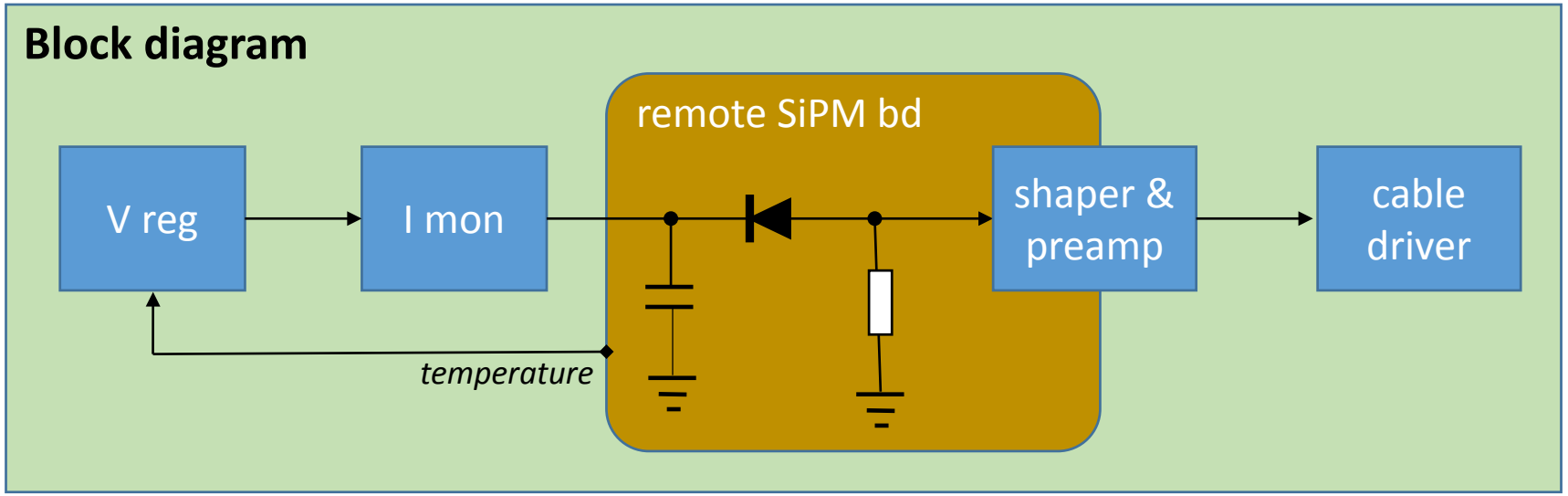
Cost of the above readout: Roughly estimated $36/ch for FEB. (Compared to budget ~$63/ch, if I understand right from Justin. So that seems reasonable.)

In principle, replacement of the COTS ADC and FPGA by an ASIC offering an **equivalent architecture & performance** at lower cost and power would be great. Perhaps it's a possibility (e.g. several SBIR efforts are underway).

External digitizer alternative

Alternative plan, can be discussed:

As with STAR FCS, digitize in racks, 16 or 32 ch digitizer boards. Only bias and preamps on-detector.



Pro's

- Somewhat less power inside (but cable driver takes some power…)
- More of the electronics is outside / serviceable
- "Easier" upgrade?
- Commercial digitizer?

Con's

- Cost of cables
- Cost of more boards, crates, power supplies, development work
- Size of cables in integration
- More connectors! (Less reliable)
- Noise pickup?
- Extra slow controls needed (i.e. at preamps and at ADC's)

fyi

STAR FCS "MDR" cable assemblies
16 channels per cable
diameter 7.2 mm
~128 cables used
60 foot length
performance flawless
cost $262 (May 2020)
NEC type CL2 (safety approved)

My vote at present: Unified FEB, just take care that it is reliable. We can do that!

Sketch of steps to get to production readout design

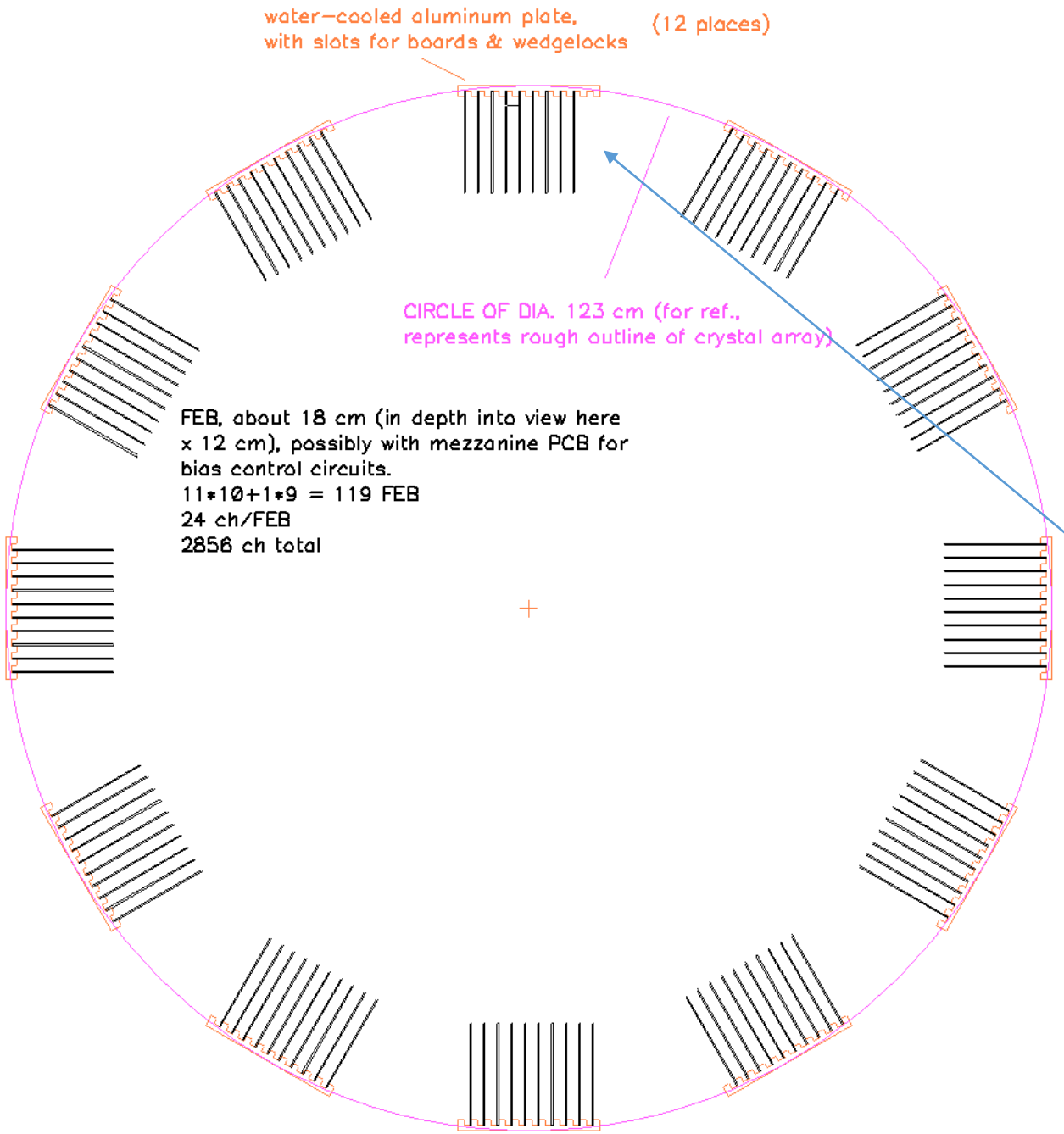
- The forward ECAL readout is now being designed (basically) under eRD109
  - ADC (TI # ADC3442) and FPGA (Microchip # MPF100T-FCVG484E) selected and procured
  - have FPGA eval board, learning to work with PolarFire
  - plan to make a 2-channel signal path prototype to connect to FPGA eval board (next month or two)
  - prototyping in progress for magnetic field tolerant DC/DC and for long data cable to RDO
- Outcome from eRD109 is a proof-of-principle FEB (**qty 3**) but we make every attempt to meet the production FEB requirements, that is the main point of it
- Only minor revisions expected before production, e.g., to take advantage of a better component newly available, or correct a few small issues
- eRD109 FEB will be used for testbeam and other tests for fwd ECAL, *and can be adapted to test bwd ECAL*
- Available early summer 2024
- We need to take that design and restructure it for a production bwd ECAL FEB
  - “long” (60 cm) instead of short connection to SiPM boards
  - perhaps move preamps onto SiPM boards?
  - 24 instead of 32 channels, probably
  - *An early purchase of at least the FPGA’s and ADC’s for bwd ECAL prototyping would be wise*
- *As also in fwd ECAL, we have work to do to understand **rate requirements**, and radiation impact on SiPM’s*

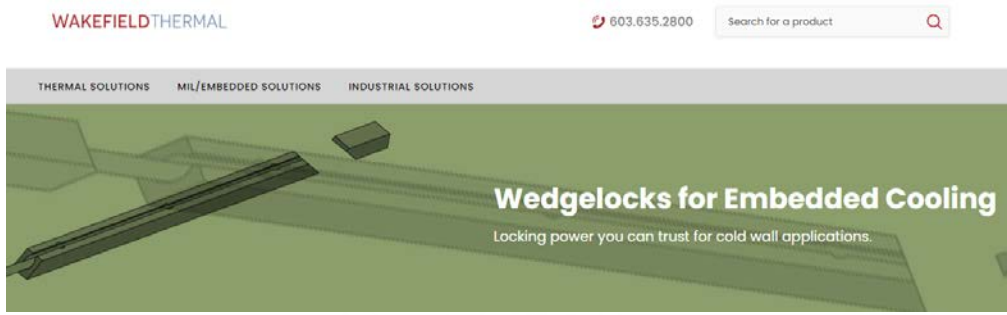
Conclusions

- A straightforward waveform-digitizing streaming readout for the backwards ECAL is feasible
- No concerns about resolution and linearity
- Integration looks feasible, sufficient space and it will be possible to avoid any thermal impact from the readout on the crystals
- Production cost expected to be in line with previous budget estimates
- Indiana University / myself interested to be responsible for this design and production oversight
    - Some funding would be needed (start date in 2024)
- Of course, other engineering resources can also contribute or do this instead – I am still happy to help / share fwd ECAL design info/experience

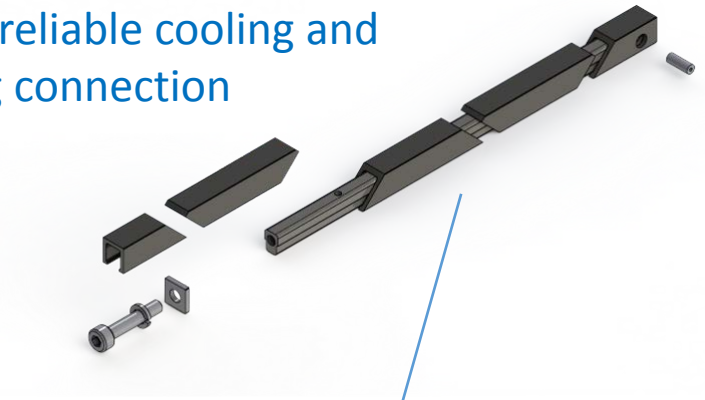
backup

FEB mechanical & cooling

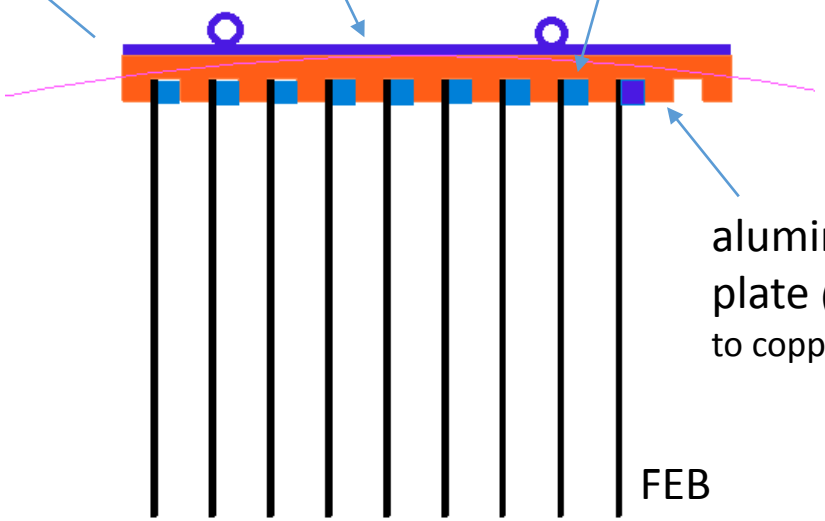




modular, reliable cooling and mounting connection

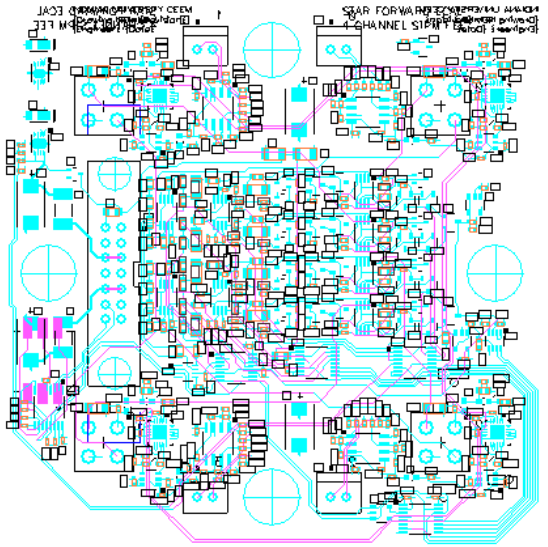


brazed copper heatsink



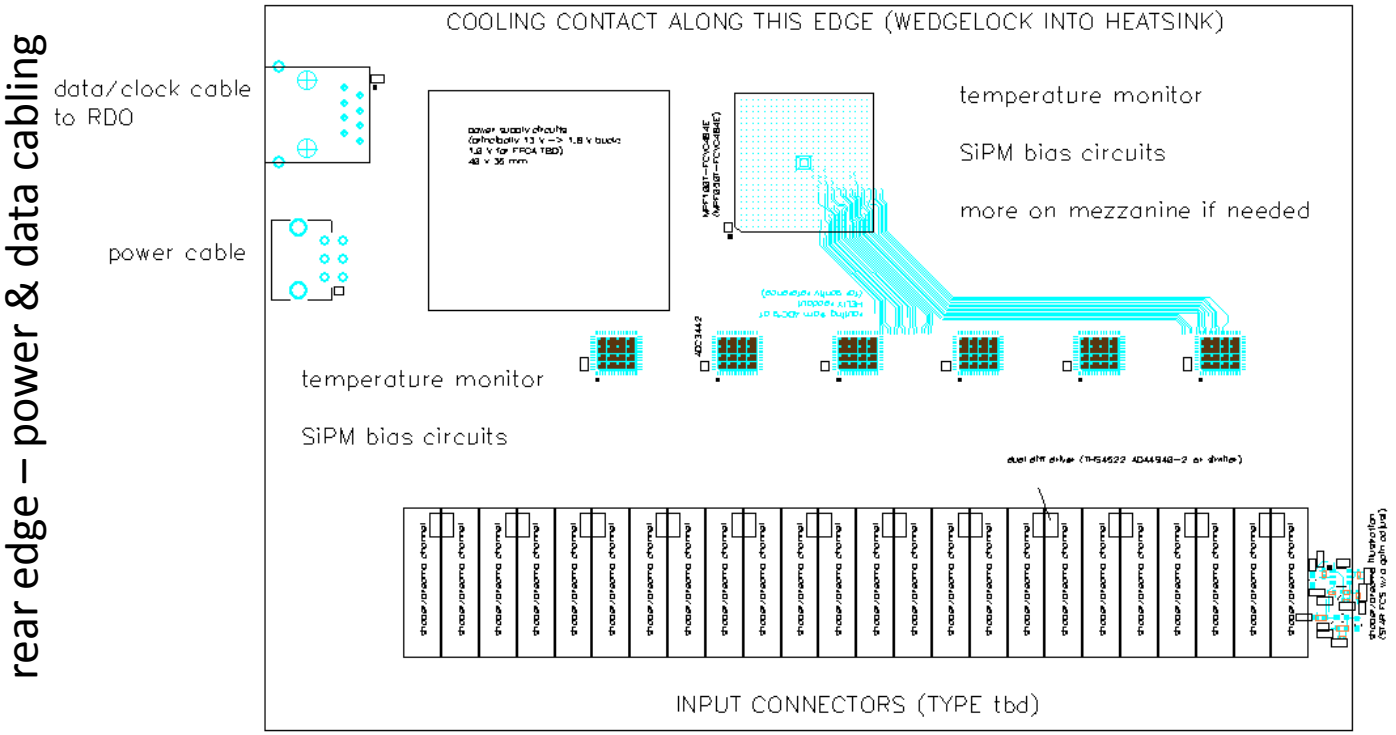
FEB layout sketch

shown with STAR FCS FEB for comparison



ePIC bwd ECAL waveform readout FEB
layout floorplanning sketch G. Visser 8/15/2023

shown with STAR fwd ECAL FEB



rear edge – power & data cabling

1 FPGA (Polarfire)
6 quad ADC's

inside radius edge – cables to SiPM boards