ALCOR ASIC

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INFN Torino

dRICH General Meeting - Readout Electronics
15.11.2023

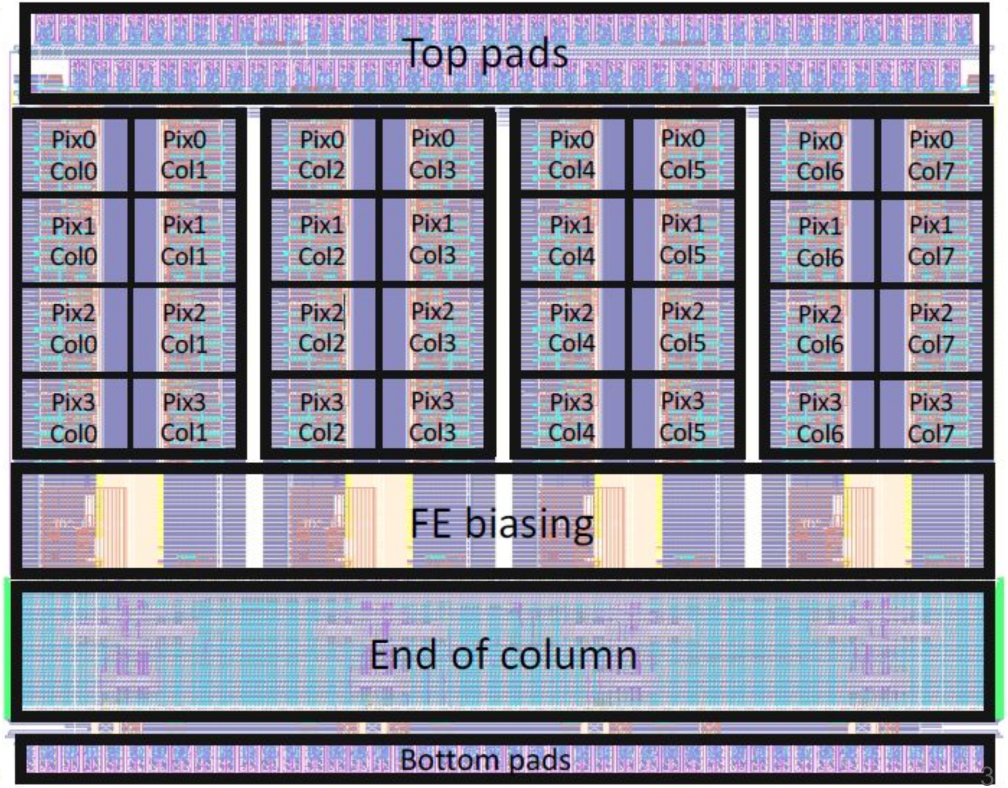
Outline

- ALCOR architecture overview
- ALCOR v2 results
    - October beam test
    - Issues investigation
- ALCOR v3 design status update
    - Internal design upgrades and new features
    - ASIC package

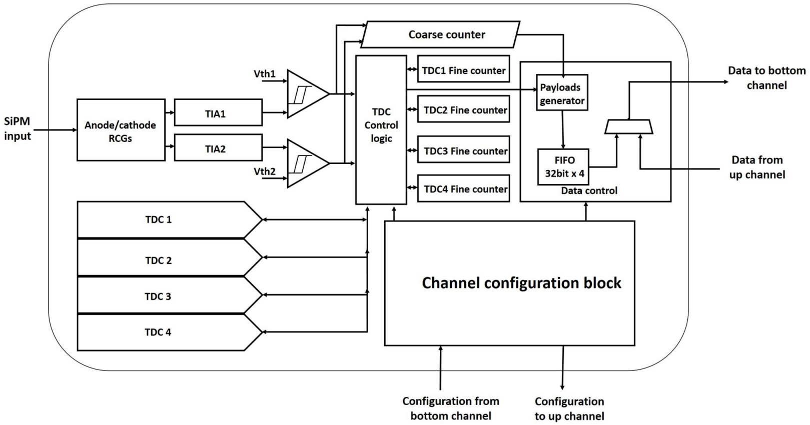
ALCOR (**A** **L**ow Power **C**hip for **O**ptical Sensor **R**eadout)

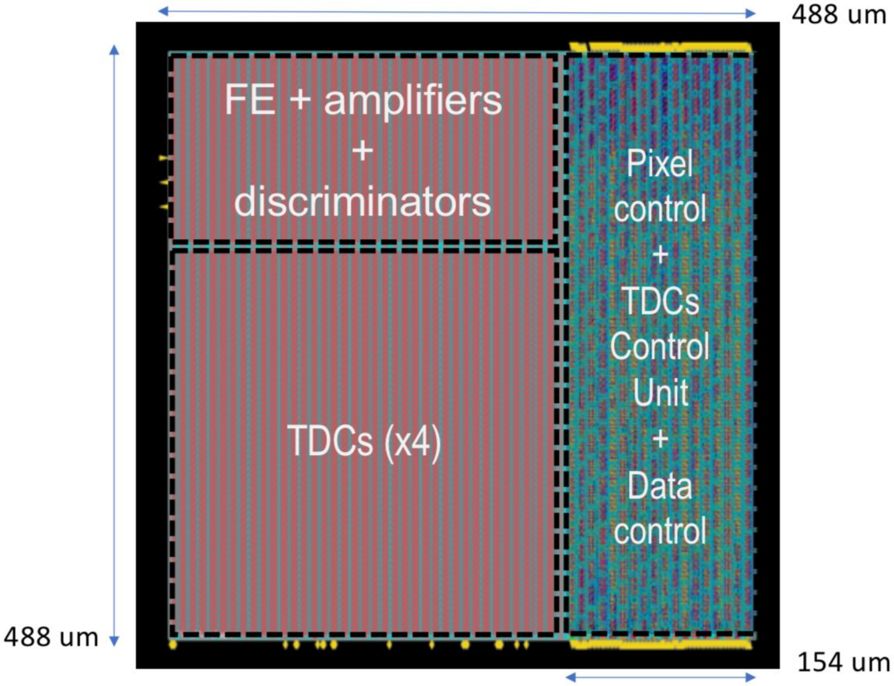
ASIC developed for the readout of the EIC dRICH SiPM sensors

- **32-pixel** matrix (8x4) mixed-signal ASIC
- **SiPM readout**: single-photon time tagging + Time-over-Threshold measurement
- 32-bit (64-bit in ToT mode) event word generated on-pixel and propagated down the column
- **Fully digital output**: 4 LVDS 320 MHz DDR Tx links



Pixel architecture





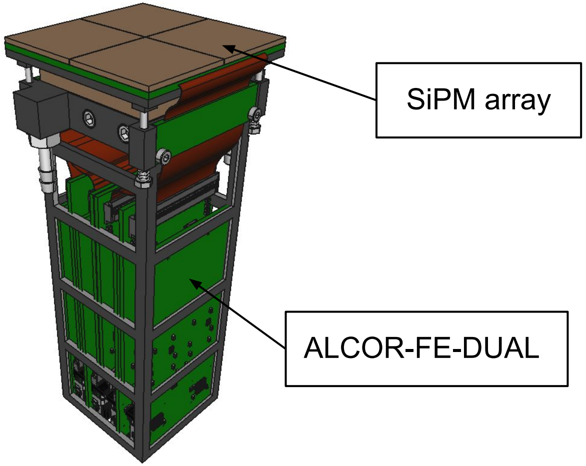
- **TIA amplifier** with RCG input stage
- 2 independent post-amp branches with 4 gain settings
- 2 **leading edge discriminators** with independent (and per pixel) threshold settings (6-bit DAC)
- 4 **TDCs** based on **analogue interpolation** with 25-50 ps time-bin (at 320 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration and data transmission

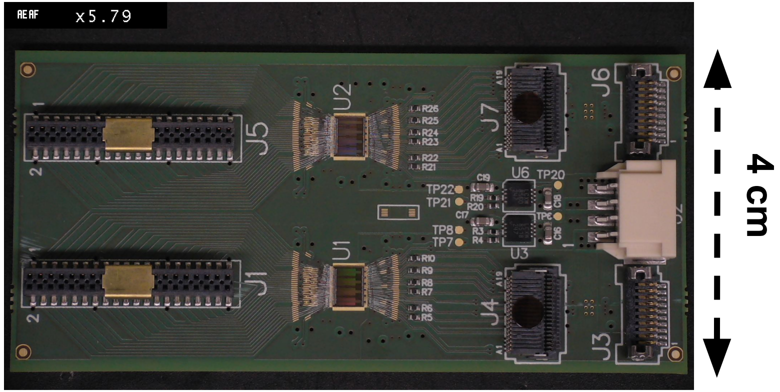
ALCOR 2023 readout system

ALCOR-FE-DUAL

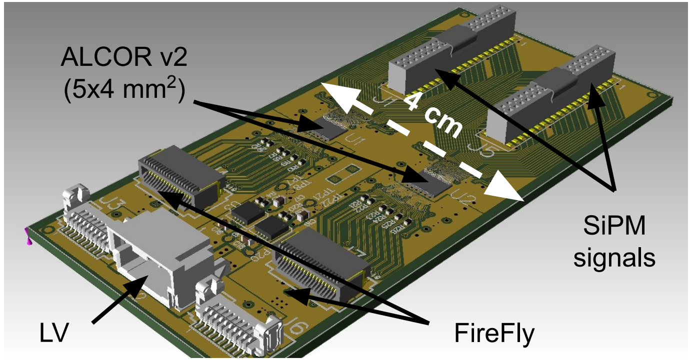
- Two **32-channel** ALCOR v2 ASICs **wire-bonded** on the PCB
- 4 ALCOR-FE-DUAL boards for each PDU
- System used for Oct 2023 beam test

Prototype photodetector unit (PDU)





designed by INFN Torino (Marco Mignone)



ALCOR v2 results

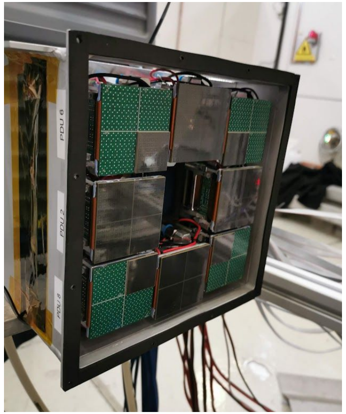
Successful beam test in October 2023, but some issues on few chips/channels…

- **Channels not sending out any data**: issue still to be found in design, recent lab tests show dependence on digital power supply, temperature and configuration settings

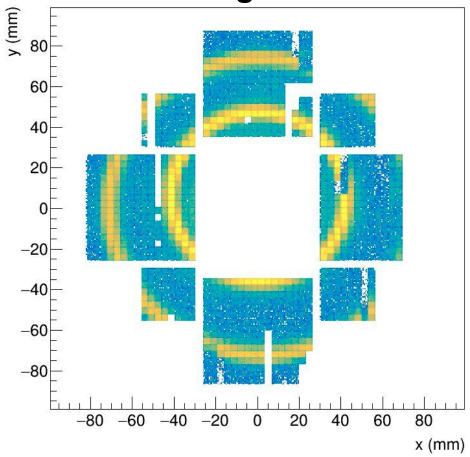
- **Cannot align** ALCOR sector **data link** (8 channels) due to reset glitch (“COUNTER reset” becomes “FULL reset” for the EoC and its ECCR → serializer is disabled): problem understood, lab tests show dependence on temperature

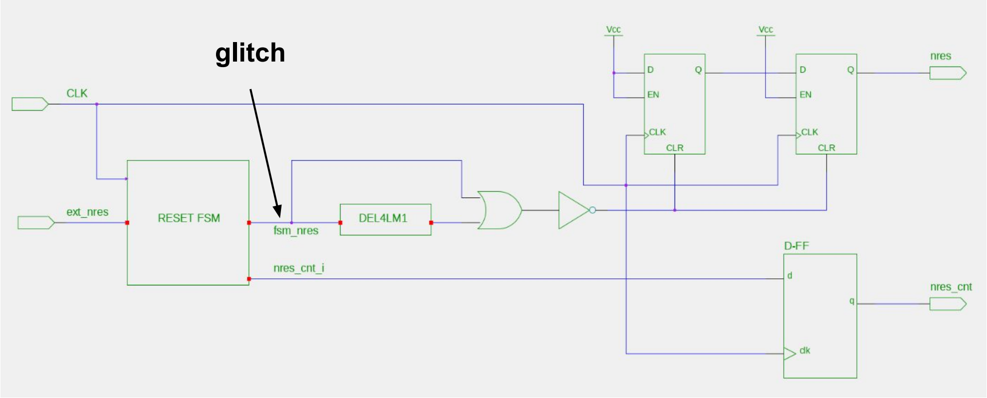
➢ Both issues seem related to PVT variations

20 FE ALCOR DUAL, 40 ALCOR v2 (1280 channels)



R. Preghenella





New tests in Torino

B07, B15, B24 back to Torino at the end of beam test → tested at room temperature

- **B07** (DVDD = 1.196 V)
    - chip 1: ch. 8,10,11, 25,26,27 missing
    - chip 2: ch. 0,1,2 missing

  → increase DVDD (1.25 V) → chip 1: ch. 8,10,11 still missing
  chip 2: ok
  → temperature scan tests

- **B15** (DVDD = 1.197 V) → one chip does not see SiPM signals
    - chip 1: ok with internal test-pulse
    - chip 2: ok with internal test-pulse

  → to be tested again with SiPM

- **B24** (DVDD = 1.197 V)
    - chip 1: soft reset glitch on Tx1 (8 clk), other sectors and pixels are ok
    - chip 2: ok

B17 had similar issues of B07 → solved increasing DVDD to 1.25 V, now in Bologna, to be validated

Climatic chamber tests (B17, DVDD = 1.25 V)

full sector missing
few channels missing
reset glitch

Chip 1 improved but still has some issues

- T = 30° C: ch.8,10,11 missing (ok with “TP TDC mode” on neighbor channels and no “raw data mode”)
- T = 20° C: ch.8 missing (ok with “TP TDC mode” on neighbor channels)
- T = 10° C: ch.8 missing
- T = 0° C: ch.0-7 missing (ok with no “raw data mode”), ch.8 missing
- T = -10° C: Tx1 reset (sometimes), ch.0-7 missing
- T = -20° C: Tx1 reset (sometimes), ch.0-7 missing (ok with no “raw data mode”)
- T = -30° C: Tx1 reset (very often), ch.0-7 missing (ok with no “raw data mode”)

Chip 2 always good

- ➢ Increasing DVDD has solved the issues on chip 2, but not completely on chip 1
- ➢ Soft reset glitch more relevant at lower temperatures (8 clk)
- ➢ Two different effects with opposite behaviors w.r.t operating temperature (i.e. PVT corners)
- ➢ Different operating modes provide different results: “raw data mode” to be avoided ?
- ➢ Need to repeat this temperature scan test for other boards

Towards ALCOR v3

- **64-channel** version with **BGA package** (~256 IO pins)
- Revise **ALCOR FE** design to improve time resolution and rate capability of the SiPM+ALCOR system
  - Studies on SiPMs model and optimal coupling with ALCOR (AC coupling inside ALCOR?)
  - Increase amplifier bandwidth
  - Improve response for afterpulses and re-triggering (hysteresis discriminator)
  - Remove/modify not used features (negative polarity FE, 2nd output stage, ToT2 and SR modes)
- **Digital logic** new features and bug fixes
  - **Digital shutter** for data reduction (EIC bunch crossing: 10 ns → 1-2 ns time window)
  - Operation of ALCOR with multiple of EIC clock frequency (98.52 MHz): **394.08 MHz** (or 295.56 MHz)
  - TDC logic fix to remove orphans due to re-triggering of events very close in time
  - Increase EoC FIFO size to cope with higher data rates

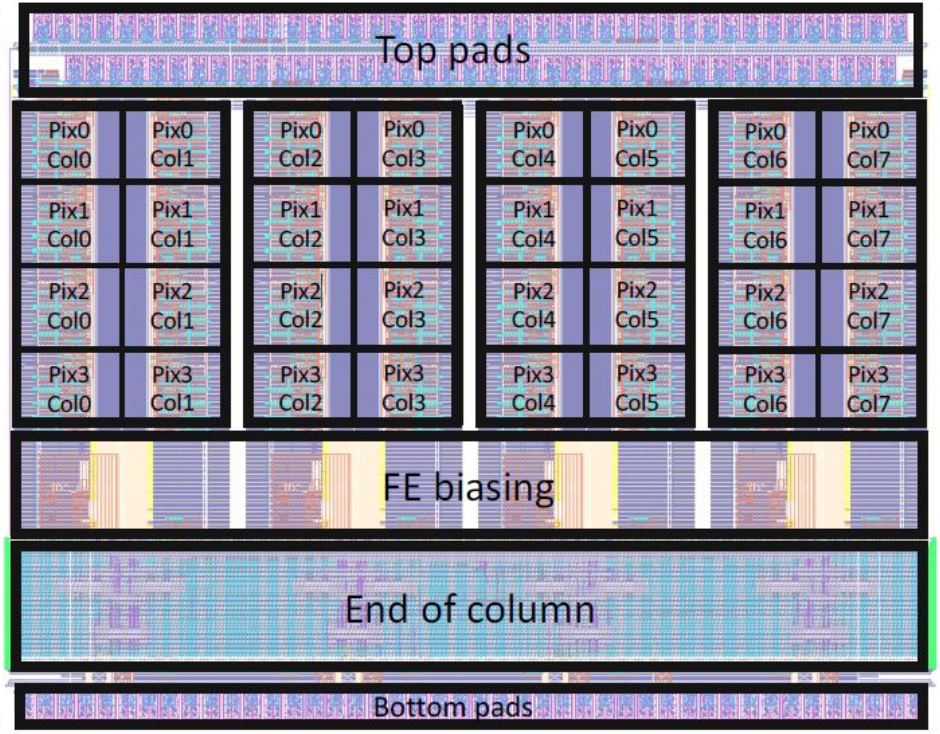
ALCOR-64 packaging

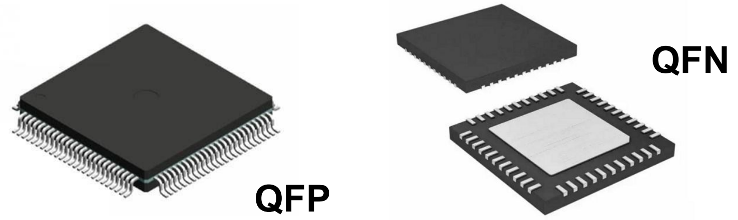
In **ALCOR-32** the space between each sector is used to route the pixels input to the Top pads (SiPMs signal)

ALCOR-64 → 8x8 pixel matrix, ~256 IO pins

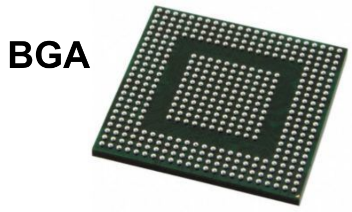
x2 increase of input channels → no space and pads to do routing from the Top pads

Standard packaging (QFP, QFN) is cheap but provides low number of pins and large area, which is not suitable for a good implementation of the 64-channel ALCOR





BGA packaging

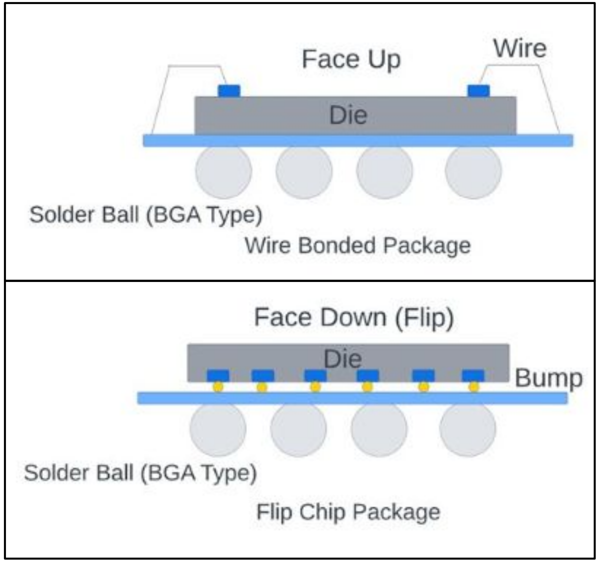


1. **Die**: bare chip which can be connected to the BGA substrate either face-up or face-down
2. **Interconnection matrix**: connects the bare chip to the BGA substrate using *wire-bond* or *flip-chip*
3. **BGA substrate**: miniature multi-layer PCB with an array of solder-bump on the bottom surface (BGA, *ball grid array*)

8x8 pixel matrix → flip-chip BGA package

Inside the package, the chip is **flipped** so that the active side of the device is **bump-bonded** to the BGA substrate

- ➢ The whole bottom surface of the device can be used → more interconnection pins and reduced device area wrt QFP or QFN
- ➢ Shorter interconnections reduce inductance, allow high-speed signals and carry heat better

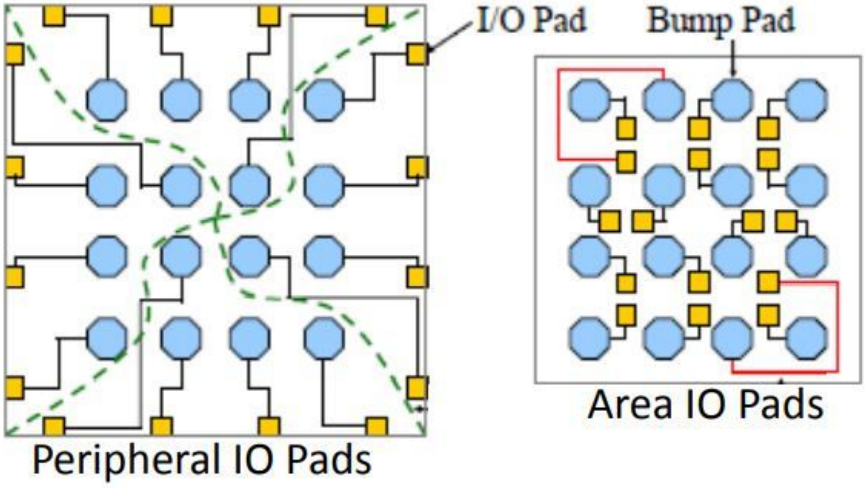


Flip-chip technology

Bump pads: pads to be connected to package interposer, usually placed in a grid pattern

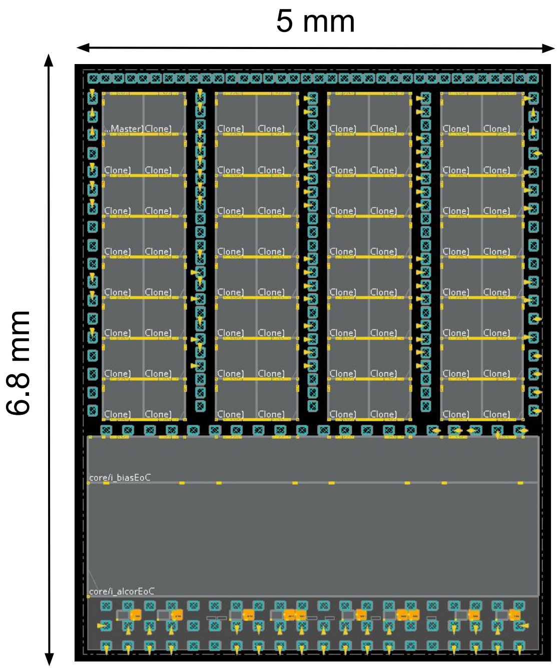
IO pads: pads providing connection to core cells of the chip, provide also ESD protection, geometry can be *peripheral* (wire-bond like) or *area*

RDL (redistribution layer): extra metal layer connecting IO pads and bump pads



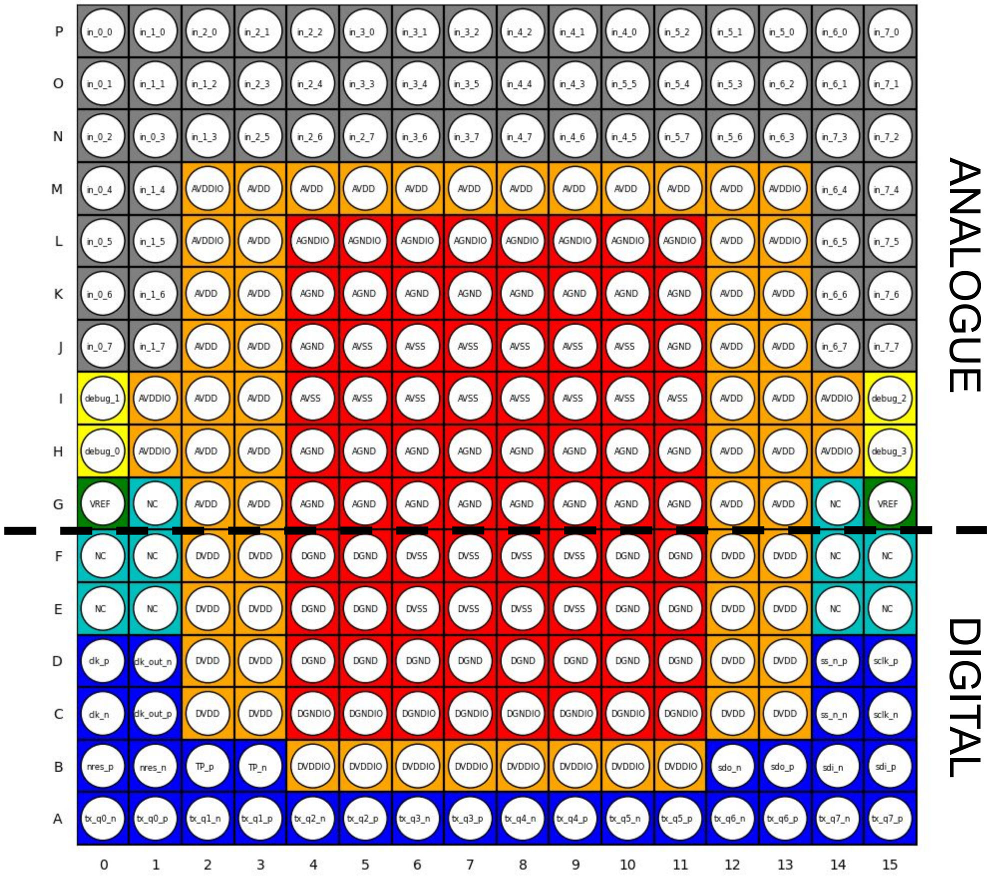
Support to RDL stopped by UMC, only METAL8 can be used to do the redistribution (but not recommended for power integrity) → need to outsource RDL to packaging company (or other company)

ALCOR v3 floorplan



8x8 pixel matrix ASIC (64 channels)

- SiPM inputs bump pads between the pixel sectors
- Digital EoC in the bottom part



256 balls BGA package (size = 12-16 mm)

- Power and ground on inner/mid contacts
- I/O on outer contacts

ALCOR v1 - v2 input stage

PM5: input transistor (common gate, CG)

PM4: CG bias

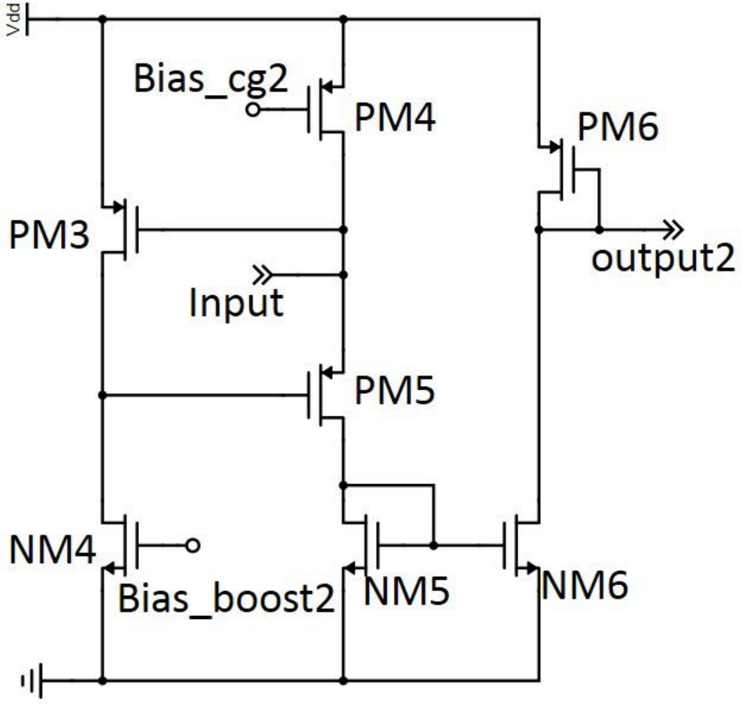
PM3: boost transistor

NM4: boost bias

PM3 + NM4 = common source (CS) amplifier

$A = gm_{PM3} \cdot R_p$

Zin ≃ 1 / (A * gm_{PM5})



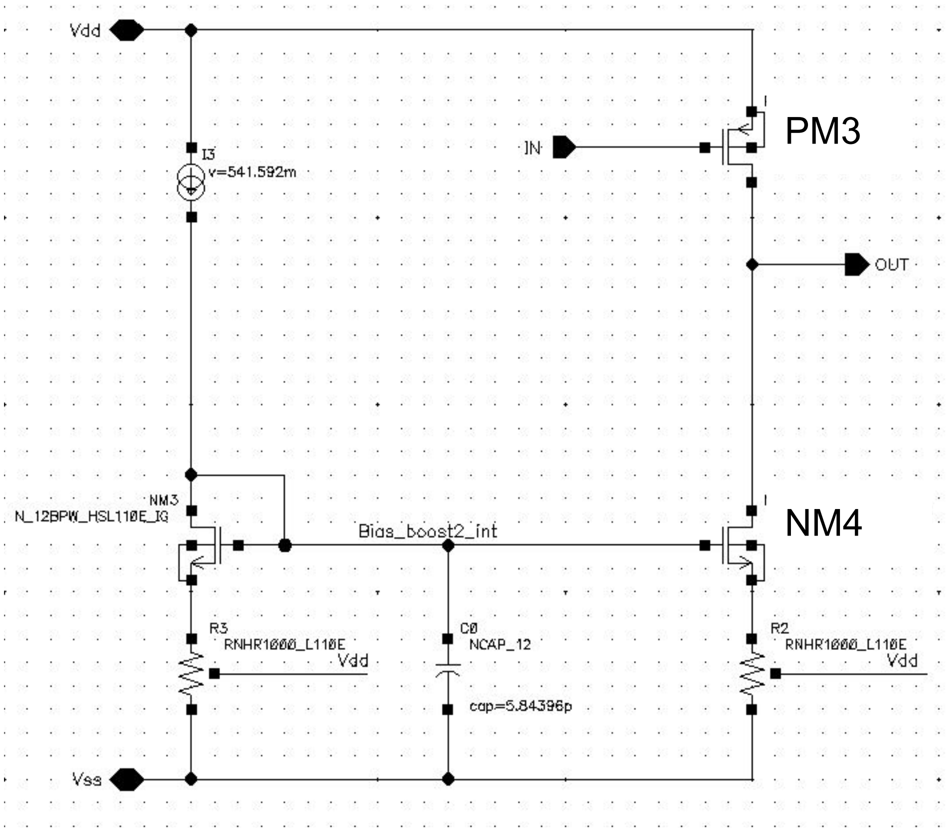
New FE (CS boost stage)

Boost bias transistor (NM4) with source degeneration to reduce its contribution to noise and increase output resistance

$\mathbf{Z_{in} \approx 1 / (A * gm_{PM5})}$

$A = gm_{PM3} \cdot R_p$

Attention must be paid to small mismatches in the resistors and to the decreased voltage headroom

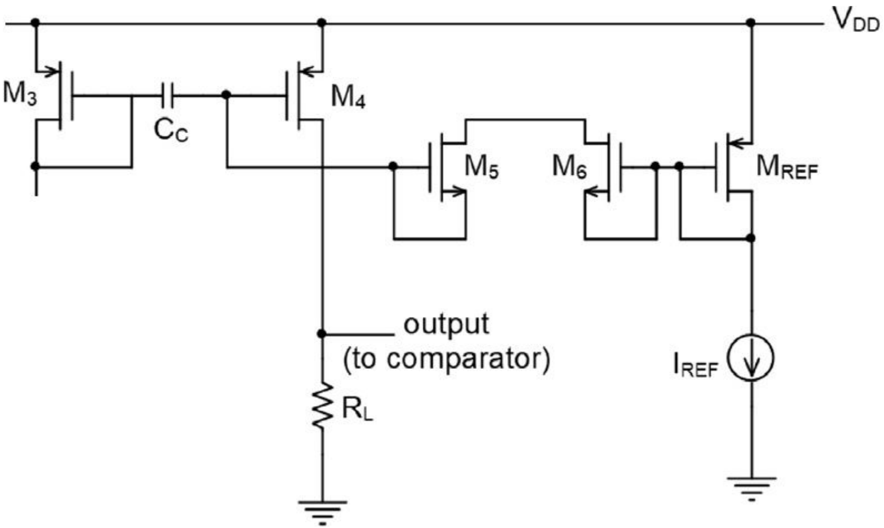


Internal AC-coupling

Input and output stages of ALCOR amplifier are AC-coupled via Cc

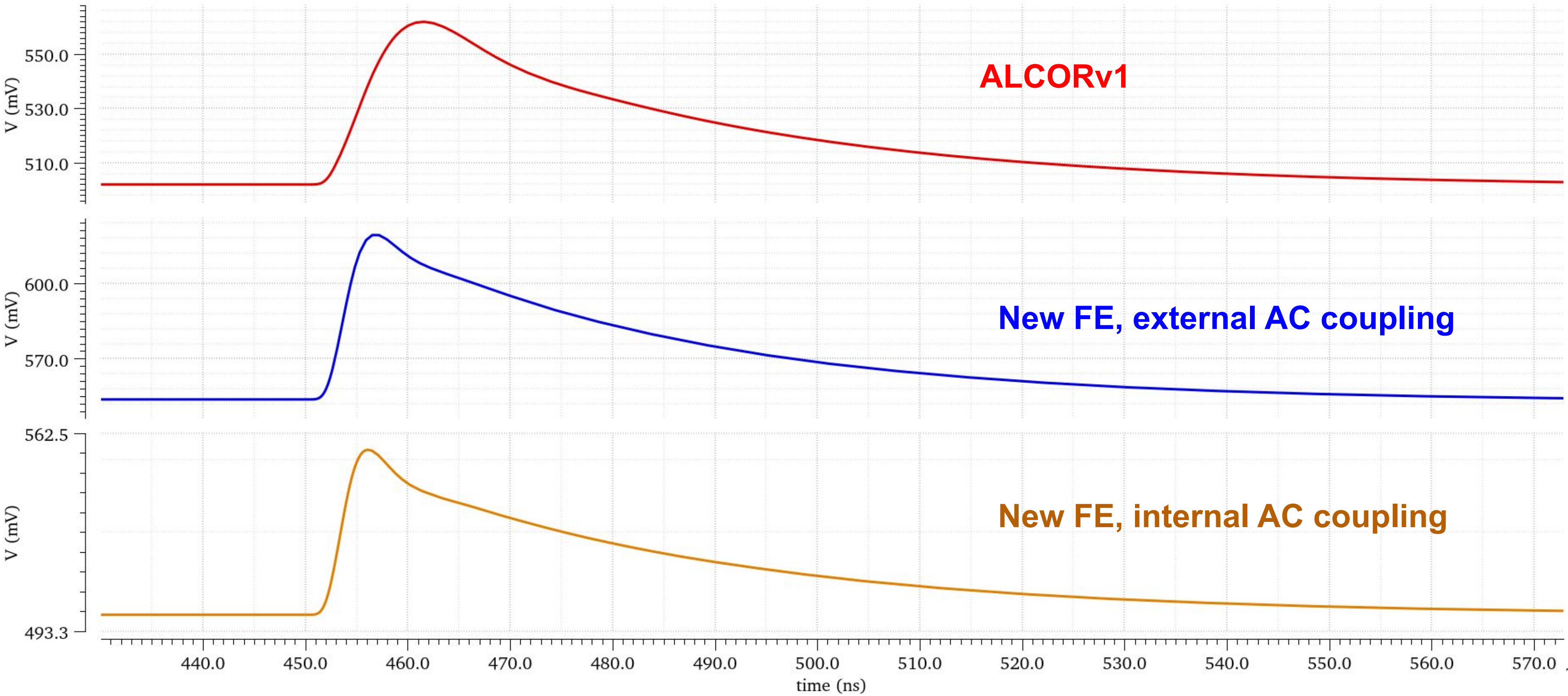
IREF and MREF set DC operating point of M4 via M5 and M6: back-to-back cut-off MOSFETS providing equivalent large resistor (~GΩ)

Baseline can be controlled using I_{REF}, using a simpler architecture w.r.t. the one implemented in ALCOR v1 - v2 with DC-coupled output stage

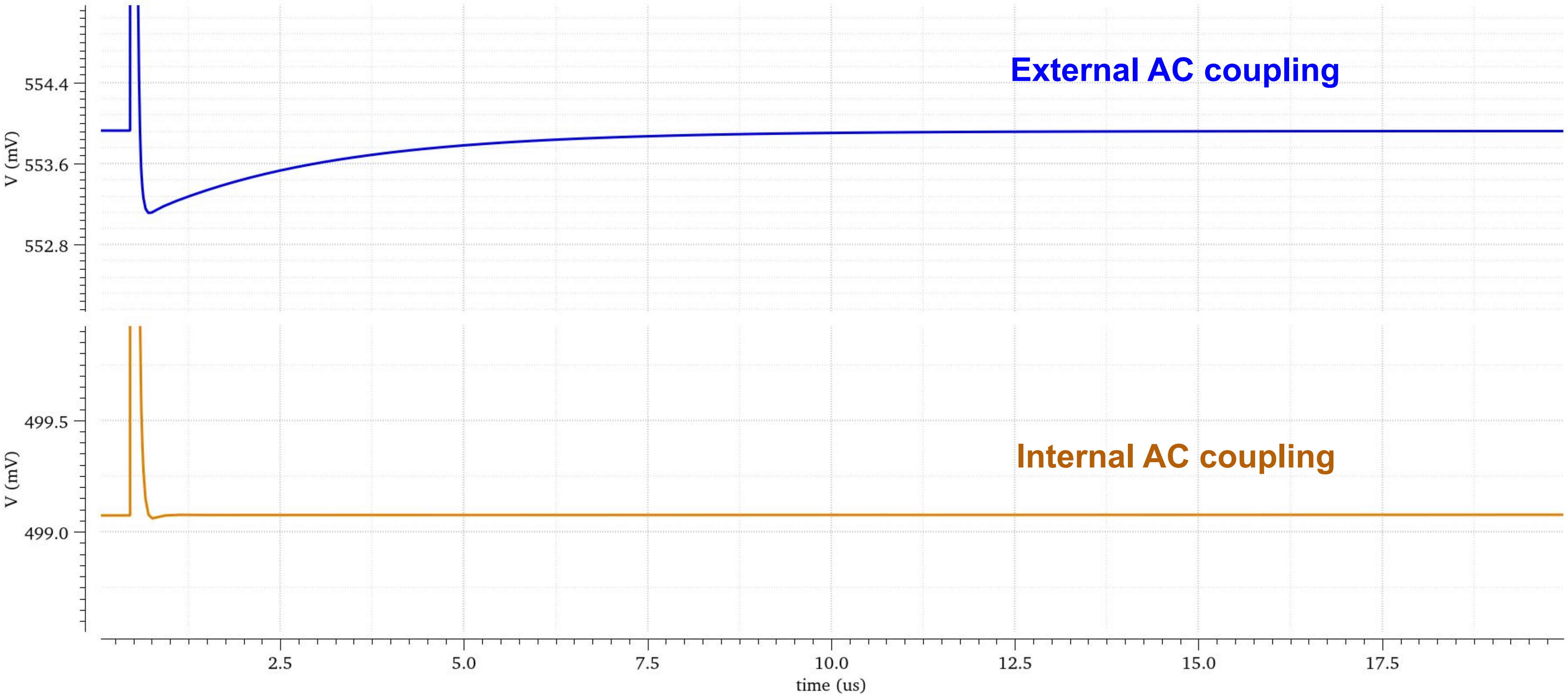


Input stage can be in principle DC-coupled to the SiPM but need to study interplay with annealing MOSFETs and SiPMs HV trim DACs

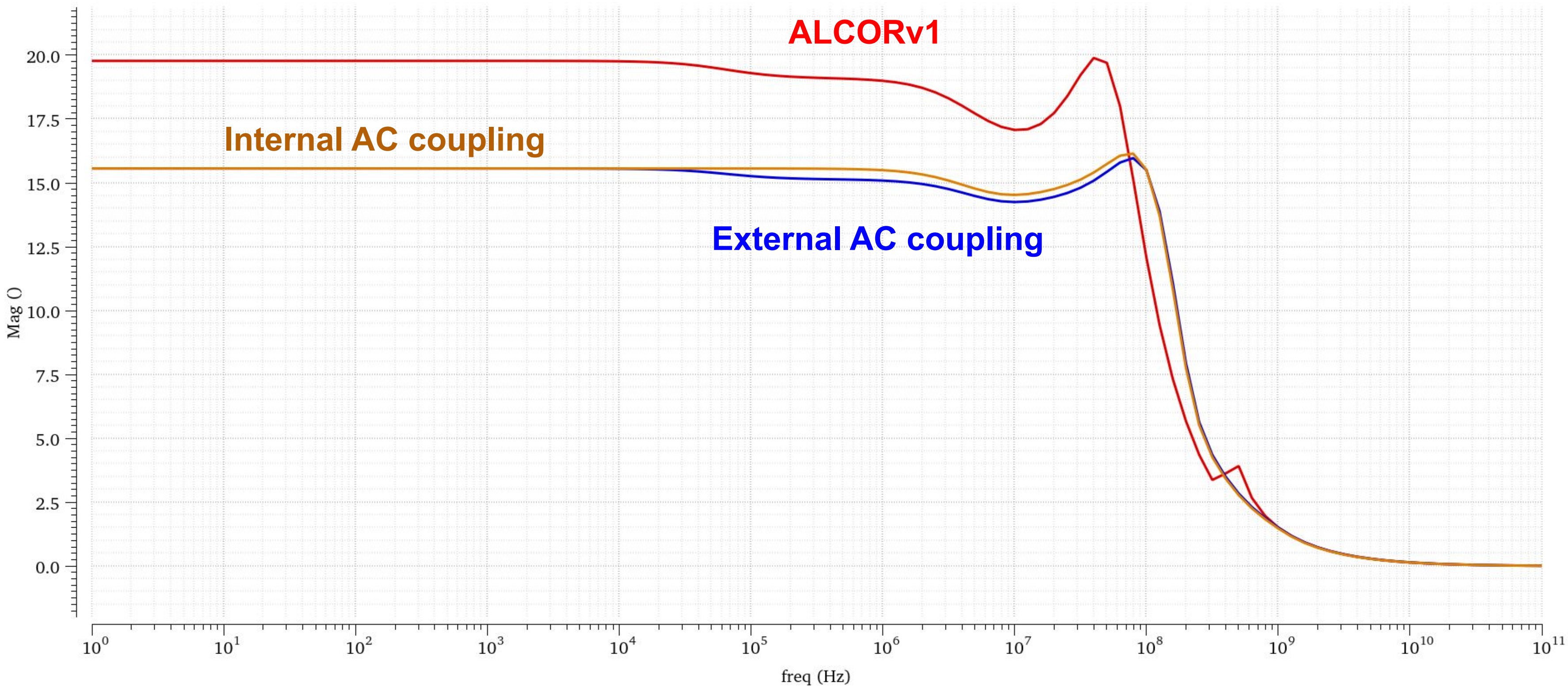
Transient simulation



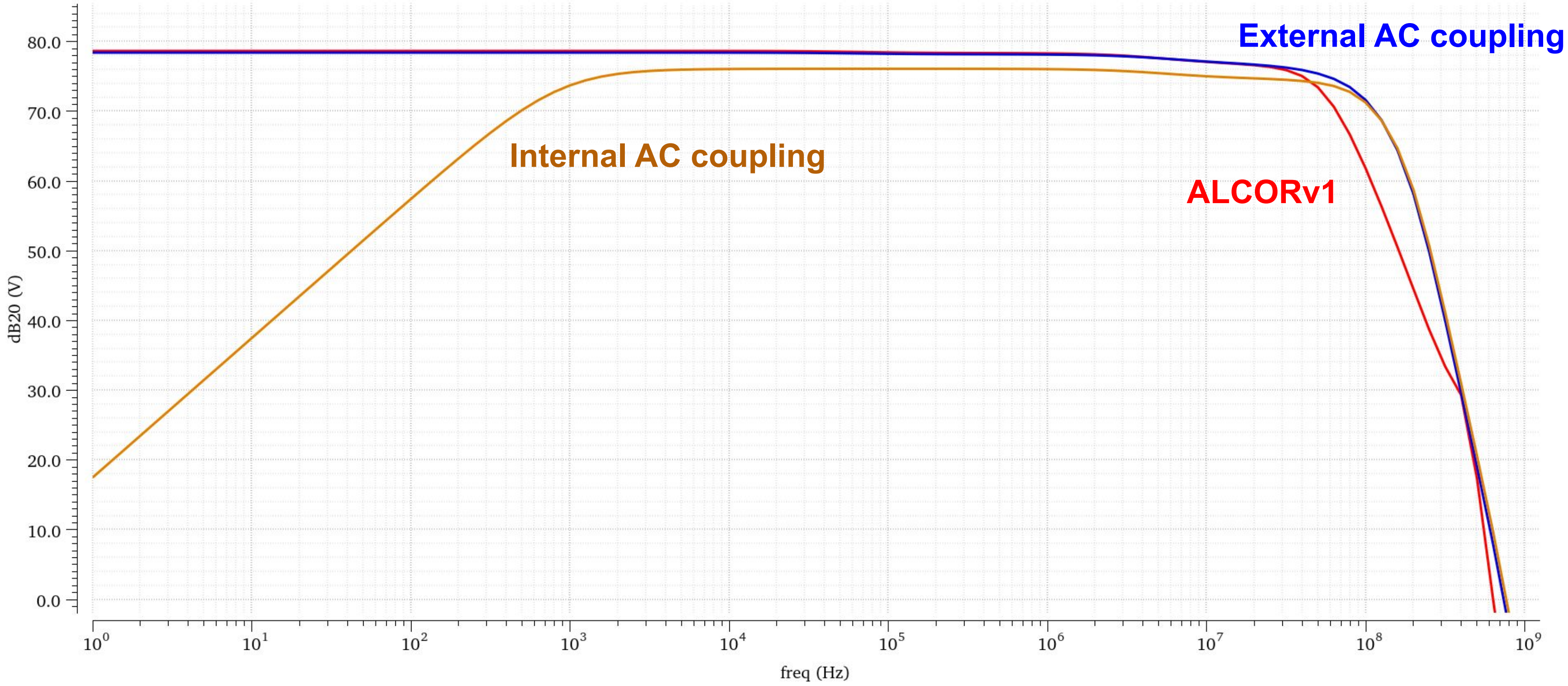
Return to baseline



Input impedance



Frequency response



Specs comparison

Schematic simulations with SiPM model: Hamamatsu S131360-3050, OV = 3 V

ALCORv1

RMSnoise	1.43 mV
SR	9.72 MV/s
jitter	**147 ps**
gain	221.4 mV/pC
SNR	41.9
rise_time	10.4 ns
Zin_DC	19.8 Ω

External AC coupling

RMSnoise	1.65 mV
SR	20 MV/s
jitter	**83 ps**
gain	243.5 mV/pC
SNR	39.7
rise_time	5.61 ns
Zin_DC	15.6 Ω

Internal AC coupling

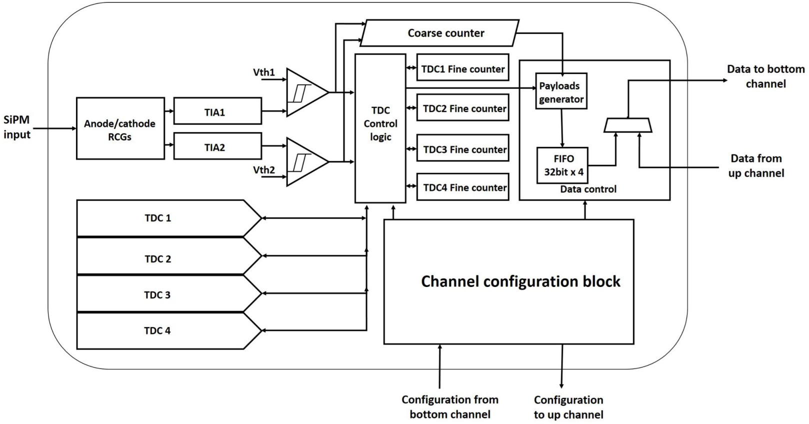
RMSnoise	1.54 mV
SR	19.74 MV/s
jitter	**78 ps**
gain	198.9 mV/pC
SNR	37.5
rise_time	5.17 ns
Zin_DC	15.6 Ω

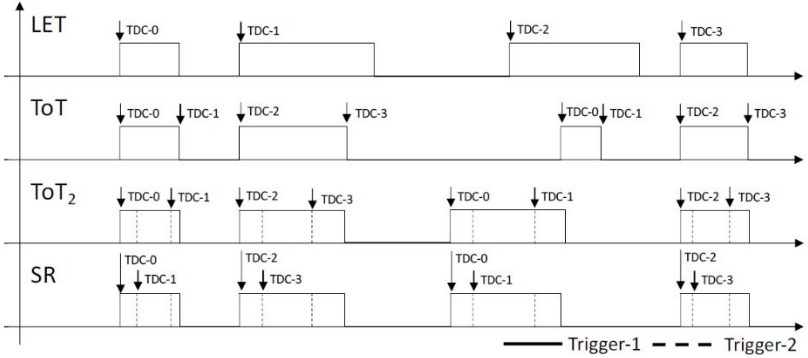
Good improvement in SR and jitter, while SNR slightly decreases

ALCOR v3 (analogue)

- ALCOR front-end supports both **SiPM polarities**, but only positive polarity is required in EIC:
  - ❏ keep as it is
  - ❏ remove negative polarity FE

- ALCOR front-end has two independent **output stages** (TIA) with 4 gain settings, each coupled to a **leading edge discriminator** (LE), but TIA2 and LE2 have not been used in EIC:
  - ❏ keep as it is
  - ❏ remove both TIA2 and LE2
  - ❏ keep only LE2 (coupled to TIA1): to be used for dual-threshold mode (for ToT and SR measurements)





ALCOR v3 (digital)

Definition of ALCOR-64 digital I/Os to match RDO design → **16 LVDS signals**

- 8 DOUT
- 1 CLKIN
- 1 CLKOUT
- 1 TP/SHUTTER
- 1 RESET
- 4 SPI

394.08 MHz clock frequency operation (4 x 98.52 MHz): tested ALCOR v1 at 390 MHz with promising results, more detailed tests and simulations are required, digital implementation must be re-done with new constraints

Digital shutter: “inhibit” pixel digital logic to reduce data throughput (10 ns bunch crossing, 250 ps bunch length, select 1-2 ns → 5-10x data reduction before ALCOR digitization)
→ Asynchronous digital shutter implemented in ALCOR v3 pixel logic

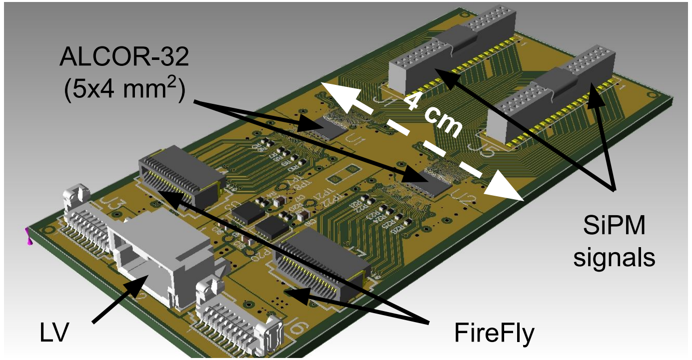
- Programmable delays to guarantee same time window for all the channels across the matrix
- Need to evaluate effect due to time-walk and thresholds dispersion

ALCOR v3 FEB

Start design of the EPIC dRICH Front-End Board (FEB), hosting the ALCOR v3 chip inside the BGA package

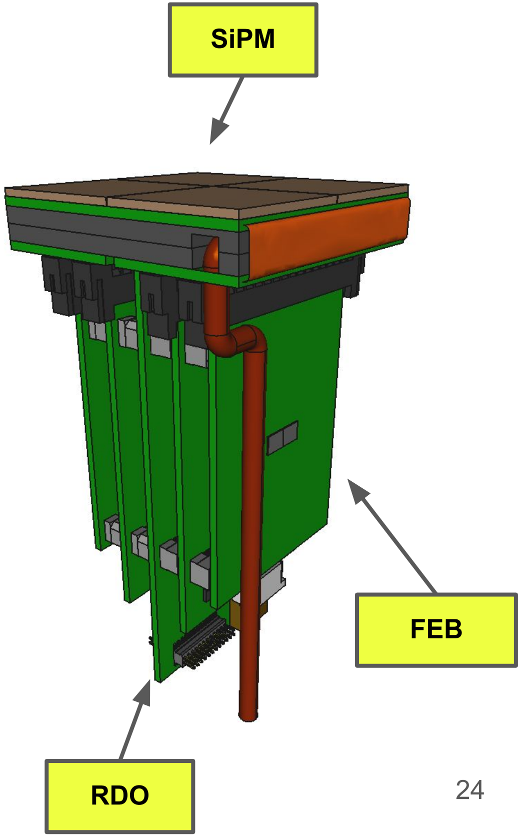
- Two ALCOR v2 (32 channels) replaced by one ALCOR v3 (64 channels)
- Firefly connectors replaced by connectors towards RDO board
- Add annealing Mosfets and HV fine DACs (currently mounted on adapter board)

ALCOR-FE-DUAL (2023-24 version)



Started development of transition board to use current ALCOR-FE-DUAL with new RDO board (2024)

Photodetector unit
(conceptual design of final layout)

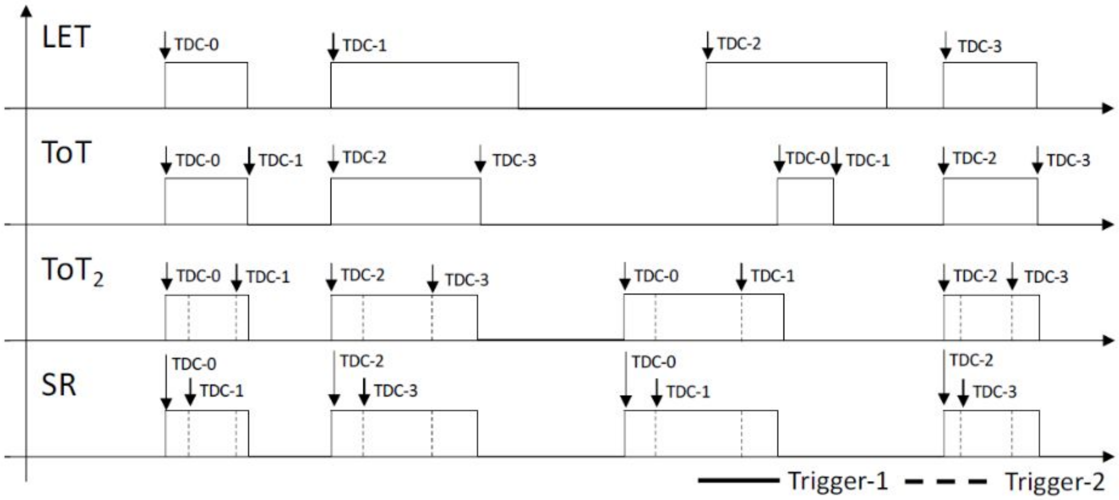


Summary

- **ALCOR v2** (MPW, 60 chips) successfully used during Oct 2023 beam test
  - 20 ALCOR FE DUAL boards: (40 ALCOR v2, 1280 channels)
  - TDC logic error of ALCOR v1 solved → easier operation w.r.t. previous beam tests
  - Some issues on single chips/channels to be investigated and understood
- **ALCOR v2.1** (INFN internal engineering run) wafers received, dicing ongoing
  - Small improvements in TDC logic for better time measurement
  - To be tested for issues found in ALCOR v2
  - Will deliver lots of chips → 20 new ALCOR FE DUAL boards to be produced and assembled for 2024 activities
- Design of **ALCOR v3** and its package ongoing
  - 64-channel MPW version to be submitted before next summer
  - Internal design upgrades providing improved performance and new features
  - Market survey with package manufacturers to define BGA packaging specs and costs

Spare slides

ALCOR pixel operating modes



4 operating modes:

- LET: leading edge measurement
- ToT: Time-over-Threshold measurement using the first discriminator for both edges
- ToT2: Time-over-Threshold measurement using both discriminators
- SR: slew-rate measurement

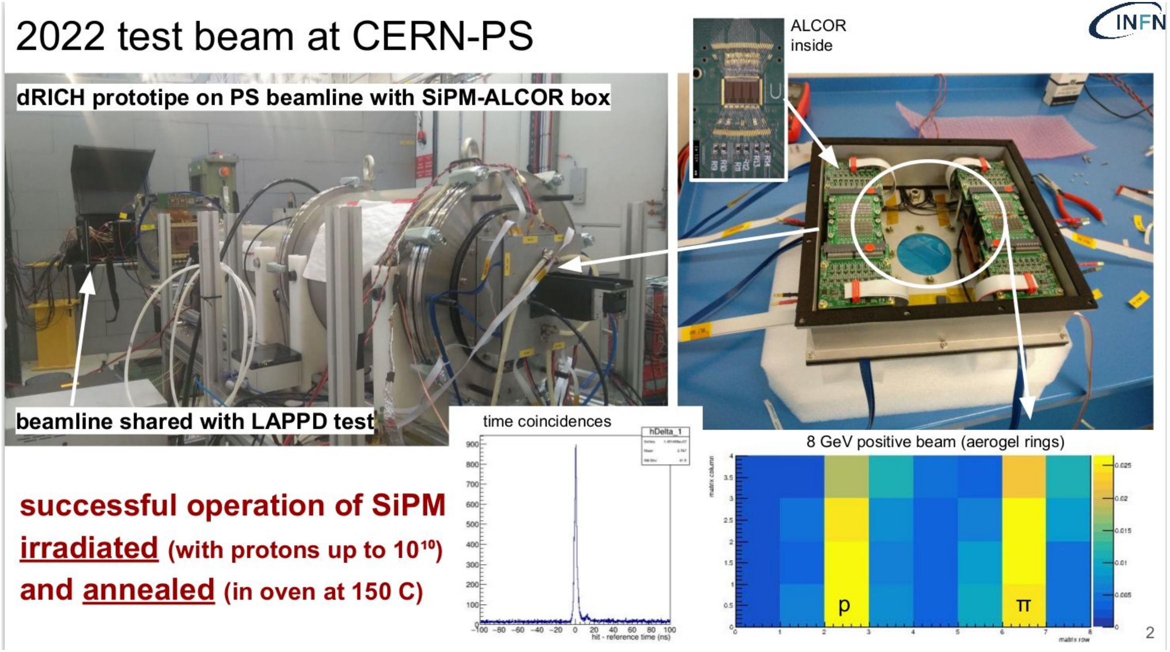
Each mode can be set to:

- FE: normal operation mode
- FE_TP: send test-pulse to analogue front-end
- TDC_TP: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)

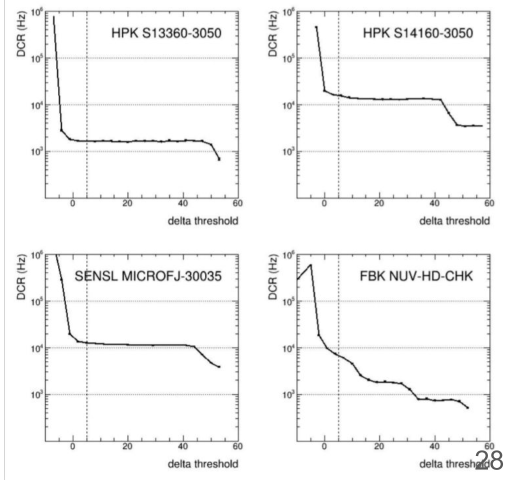
Each pixel can also be disabled

ALCOR v1

- Developed for the readout of SiPMs at 77K, in the framework of Darkside (MPW, Dec 2019)
- Extensively used within the EIC dRICH Collaboration in the last 2 years



Slides from R. Preghenella



ALCOR v2

ALCOR v2

- MPW, submitted in Dec 2022
- 60 chips, received in June, promising results from preliminary tests
  - ✓ TDC logic critical error at high rates solved also for DCR rate at room temperature
  - ✓ New FE gain settings more suited for single photon applications
  - ✓ On-chip test-pulse also for EIC SiPM polarity
  - ✓ Special words from EoC (header, frame, CRC) ok also when status words are disabled

ALCOR v2.1

- INFN internal engineering run
- Submitted in Mar 2023, wafers delivered, dicing ongoing
- High number of chips will be available
- Removed TDC logic bugs (TFine-clock ambiguity, TOT orphans due to fake trigger at very low rates)

ALCOR v2

- ➢ MPW, submitted in Dec 2022
- ➢ **~50-60 chips received mid June 2023, tests started 19th June 2023**

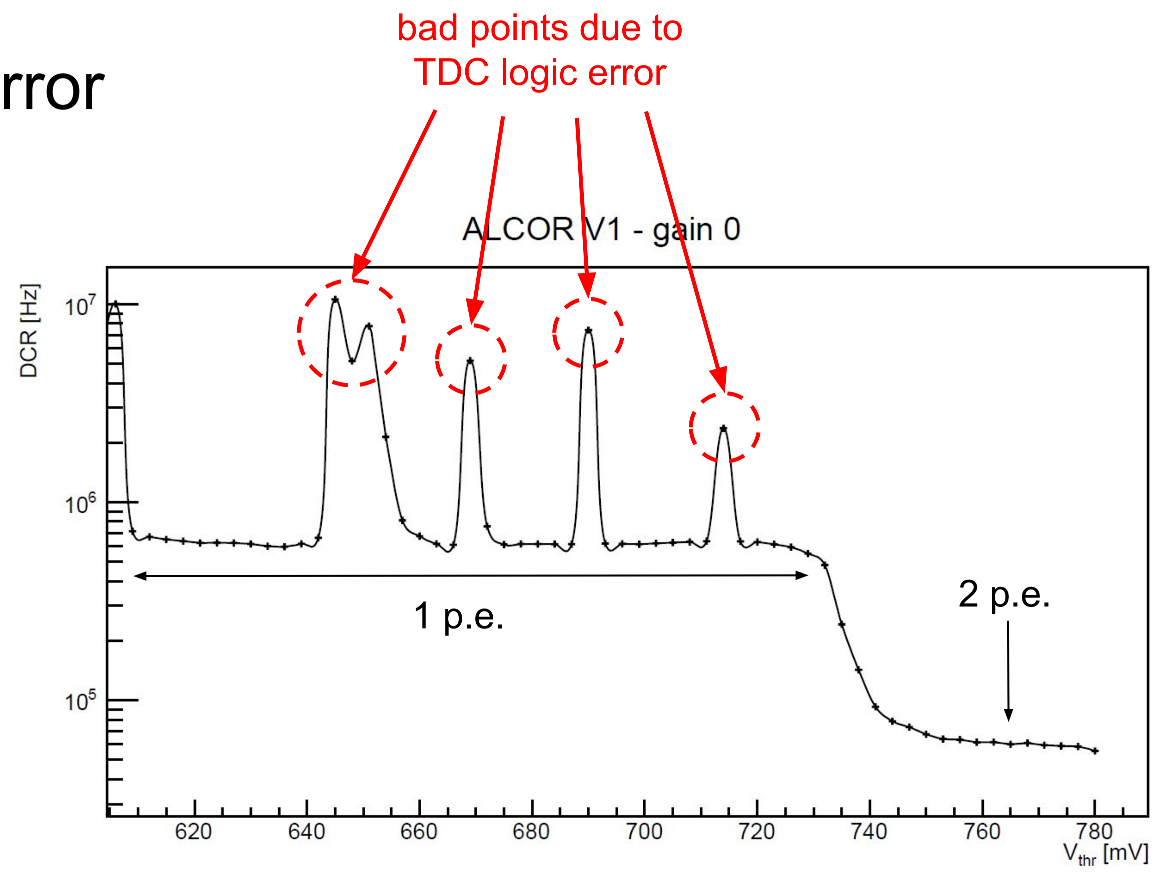
Bug fixes and new features:

1. Solve TDC logic critical error occurring at high rates
2. Generation of special words from EoC (header, frame, CRC) also when status words are disabled
3. New FE gain settings more suited for single photon applications
4. On-chip test-pulse also for EIC SiPMs polarity

1. TDC logic critical error

ALCORv1 TDC logic bug

- occurs at high rates (DCR > 500 kHz)
- generates corrupted data which saturates the ASIC output bandwidth
- requires a full reset to recover



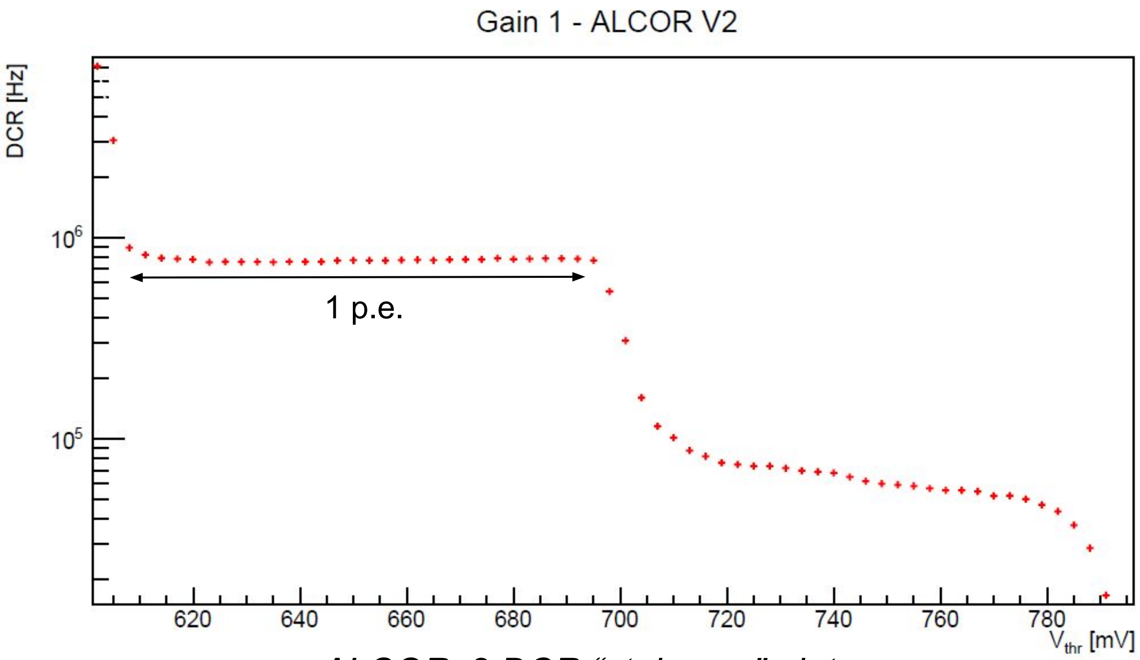
ALCORv1 DCR "staircase" plot

1. TDC logic critical error

ALCORv1 TDC logic bug

- occurs at high rates (DCR > 500 kHz)
- generates corrupted data which saturates the ASIC output bandwidth
- requires a full reset to recover

➢ **Solved in ALCORv2**



ALCORv2 DCR “staircase” plot

2. EoC special words

Header, *frame*, *CRC* and *status* words are added to *event* words to provide information for data clustering, synchronization and verification

ALCORv1 can operate in *raw-data mode* (only event words) or in *full mode* (all special words are included)

- ➢ **ALCORv2** can also operate in an intermediate mode where only ***status* words** are **disabled**
- ➢ This helps to reduce data throughput (status words are >50% of special words)

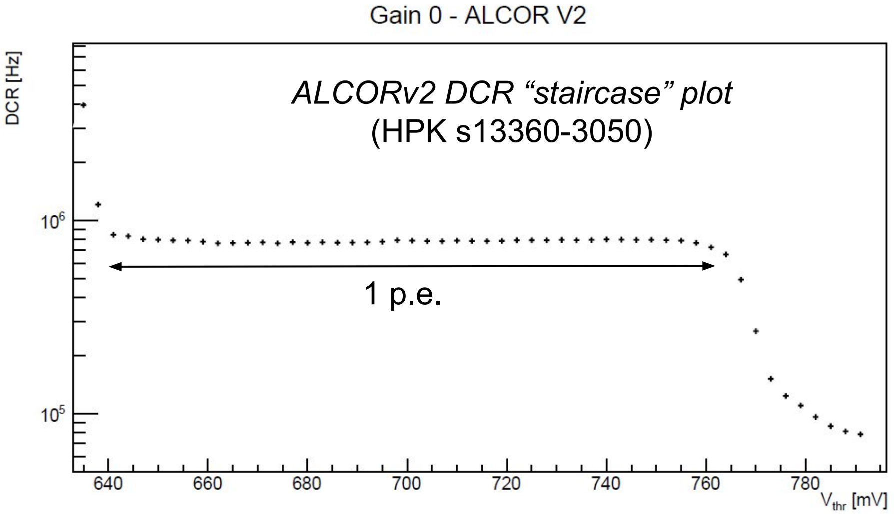
FIFO position	Data
1 (FPGA first received)	K28.0 (Frame header)
2	Frame number (16 bit)
3	Event words Column 0
..	Event words Column 1
n	K28.2 (Coarse Counter Rollover header)
n+1	K28.3 (Status header)
n+2	Status words Column 0 (x4)
n+6	Status words Column 1 (x4)
n+10	End of Column status word
n+11	K28.4 (Checksum header)
n+12	CRC value
n+13	K28.0 (New Frame header)

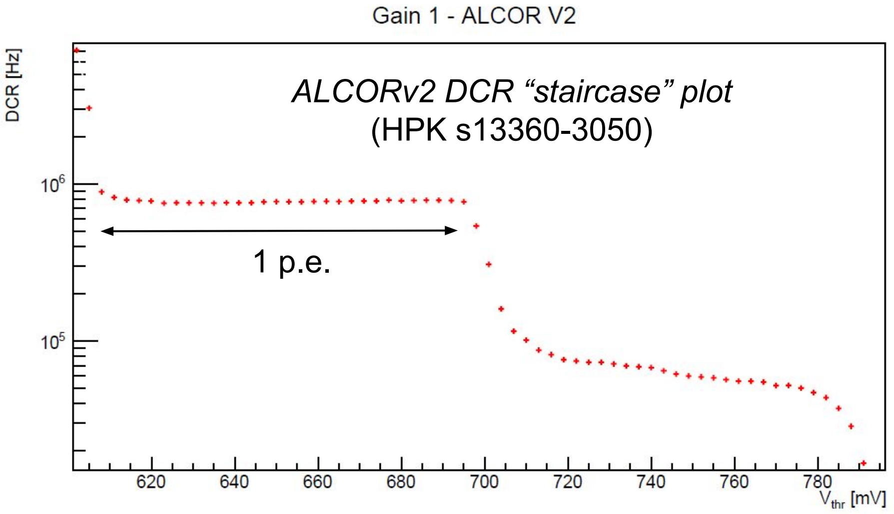
Table 5: Data stream with data events.

3. FE gain settings

ALCORv2 front-end implements two different gain settings best suited for single-photon applications

- ➢ to be tested with different SiPM models currently used within the EIC dRICH framework



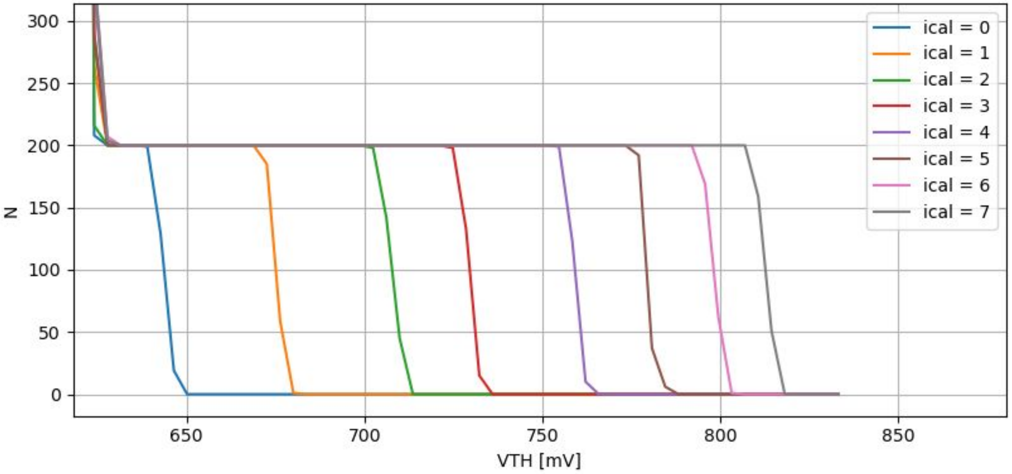


4. On-chip test-pulse

ALCOR can read both input signal polarities, but ALCORv1 internal test-pulse can only inject signals for negative polarity

- ➢ On-chip test-pulse generation included in **ALCORv2** also for EIC SiPMs signal polarity (positive)

VTH scan (200 test-pulse)



On-chip 3-bit DAC calibration circuit to define injected current magnitude